A Universal Level Converter Towards the Realization of Energy Efficient Implantable Drug Delivery Nano-Electro-Mechanical-Systems

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Abstract

Nano-Electro-Mechanical-Systems (NEMS) are a technological solution for building miniature systems which can be beneficial in terms of safety, efficacy, or convenience. Thus investigation is necessary for their usefulness in drug delivery. In order to be an effective and reliable implantable system the DDNEMS (Drug Delivery Nano-Electro-Mechanical-System) should have low power dissipation, fault tolerance, and reconfigurability capabilities. In this paper we introduce a DDNEMS architecture, identify its major components, and propose the design of the crucial component universal (voltage) level converter (ULC). The ULC is a unique component that will reduce dynamic power and leakage of DDNEMS while facilitating its reconfigurability. The ULC is capable of performing level-up and level-down conversions and can block an input signal. We have prototyped a ULC using $32nm$ high-κ/metal-gate nano-CMOS technology with dual-V_{Th} technique. The robustness of the design is tested by carrying out three types of analysis, namely: parametric, load and power. It is observed that the ULC produces a stable output for voltages as low as $0.35V$ and loads varying from $50fF$ to $120fF$. The average power dissipation of the proposed level converter with a $82fF$ capacitive load is $5\mu W$.

Keywords

Drug Delivery Nano-Electro-Mechanical-Systems (DDNEMS), Power Management, DC to DC Level Converter, Low-Power Design, Dual Threshold Voltage, High-κ/Metal-Gate Nano-CMOS, Optimization

1 Introduction, Motivations, and Contributions

Tremendous interest in improving the quality of human life has led to research in the area of self-health management. Most of the conventional drug delivery schemes suffer from drawbacks that can seriously limit their effectiveness. NEMS are a technological solution for building miniature systems which can be beneficial in terms of safety, efficacy, or convenience [12, 11]. The goal of NEMS based drug delivery is to administer drugs to pre-determined targets in the body through implantable chips which are controlled or programmed externally through a radio frequency interface. In order to be an effective and reliable implantable system the DDNEMS should have the following attributes: (1) low power consumption, (2) fault tolerance, and (3) reconfigurability and field upgradability.

High power dissipation is the primary bottleneck for the growth of implantable systems. It has many side effects, such as reduction in battery life time, increase in operating temperature of the system which will then require a heat transfer mechanism, affecting the portion of the body where it is implanted. Thus, there is need for devising integrated power management methods to reduce power consumption in DDNEMS. When the DDNEMS is realized using nano-CMOS technology, the major components of total power dissipation are: gate-oxide leakage, subthreshold leakage, and dynamic power [7]. These power dissipation sources depend on supply voltage, either linearly or quadratically. Dynamic power management techniques with variable V_{DD}) are used for system level power reduction and multiple supply voltage (multi-V_{DD}) is a static solution for switching power reduction in ASICs.

DDNEMS can be realized as system-on-chip (SoC) while supplied with power from a single battery source. In this paper we propose a special type of level converter, called ULC, suitable for power management and field programmability of DDNEMS. Efficient design of ULC is critical to reduce the overhead on the circuits that they are designed to serve. In this paper we consider using cutting-edge technology, high-κ/ metal-gate nano-CMOS at $32nm$ for the design of the ULC. Thus, while high-κ would be used to contain the gate leakage this will be assisted by the use of dual-V_{Th} technology to contain the subthreshold leakage. The use of high-κ serves the dual purpose of scaling of the device as well as reducing of gate leakage. Hence high-κ/ metal-gate transistors serve as a good alternative to classical transistors at nanoscale technologies [2, 3].

The novel contributions of this paper are as follows:

1. We introduce a novel implantable system called DDNEMS, which can be realized as a multicore analog/mixed-signal SoC (AMS-SoC) along with non-

electrical components for programmable drug delivery.

2. We identify the key components as well as challenges of DDNEMS design.

3. In order to serve the most pressing challenge, the power dissipation, we introduce the universal voltage-level converter (ULC).

4. A novel design flow for energy efficient design of a ULC circuit is proposed.

5. A $32nm$ high-κ/ metal-gate (HKMG) CMOS ULC has been implemented and thoroughly characterized.

6. An algorithm is presented for the simultaneous power, leakage, and delay optimization of the $32nm$ ULC.

7. A dual$-V_{Th}$ technique has been applied to this HKMG ULC for power and delay optimization.

The rest of the paper is organized as follows: Section 2 introduces the architecture of DDNEMS and the concept of ULC. Section 3 discusses the design of the ULC using HKMG nano-CMOS. Section 4 presents an optimization algorithm used in this design. Section 5 highlights the functional simulation and characterization of the ULC. Section 6 presents conclusions and directions for future research.

2 The Proposed Drug Delivery Nano-Electro-Mechanical Systems (DDNEMS)

2.1 The Proposed Architecture for DDNEMS

Fig. 1 presents an architecture for the DDNEMS, the typical components of which are presented below.

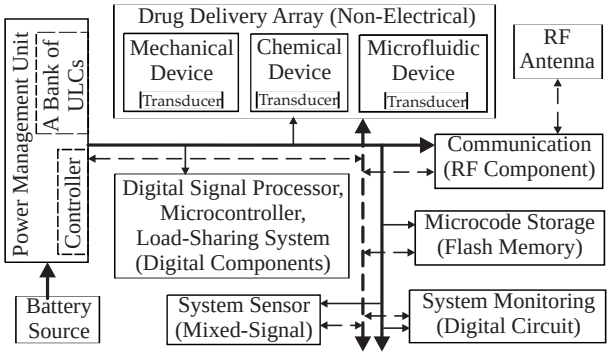


Figure 1. The proposed architecture for DDNEMS. The solid-line represents the power bus and the dotted line the data and control buses. The modules may be digital, mixed-signal, RF or non-electrical, as shown.

Power Management Unit (PMU): PMU is one of the most important components of the entire DDNEMS. Under the control of the digital signal processor (DSP) and the stored microcode, it manages the power distribution to the various subsystems to optimize energy consumption. It has built-in timers that put the system to "sleep" or "wake-up" mode and can be induced to activate the system via external signals received by the RF subsystem (to force an emergency drug delivery, for example). *The heart of PMU is a bank of ULCs*. ULC sends different operating voltages to various subsystems of DDNEMS each of which operate at different voltages from a *single battery* and facilitates reconfigurability.

Drug Delivery Array (DDA): The key component of the DDNEMS is the drug delivery subsystem, which is typically non-electrical in nature. To allow for redundancy, fault tolerance, load sharing and multiple drugs, the subsystem itself needs to be designed as an array. The array could be homogeneous (all elements of the same kind) or heterogeneous. Array elements to be considered and modeled during the design phase include micropumps, microfluidic devices, stents, and microneedles. The array elements need to have appropriate transducers to allow their control and interfacing to the electronic portion of the DDNEMS.

Electrical Components (DSP, Sensors, Memory, etc.): The data processing, controlling and interfacing aspects of the DDNEMS are handled by electrical subsystems, which are analog, digital or mixed-signal in nature. The monitoring and control of the drug array elements is performed by the sensor subsystem which receives information from, and sends control signals to the transducers. Its front-end (transducer side) is analog but the back-end, interfacing to the DSP is digital. The DSP subsystem analyzes the on-line data generated by the sensors and, under the control of the program stored in the flash memory subsystem, generates control signals to control drug delivery, facilitate fault tolerance, load sharing, and drug mixing. The system monitoring subsystem continually polls the various electrical subsystems and transducers to obtain a snapshot of the overall system's health. Upon the discovery of faults or errors, it alerts the DSP for appropriate action.

Radio Frequency Components (RF): The RF subsystem, comprising of an antenna and transmitter/receiver, can be built using RFID principles for the shape and placement of the antenna and communication protocol. Its function is to allow non-invasive maintenance of the system (modification of the microcode stored in the flash memory, for example), remote collection of data (such as amount of drug remaining in the reservoir, drug array element failures, battery status etc.), and emergency drug delivery or system deactivation.

2.2 The Universal Voltage-Level Converter

Fig. 2 shows the high level representation of the ULC. It has an input voltage signal called V_{in}, two control signals $S1$ and $S0$, two supply voltages V_{DDl}, V_{DDh}, and an output voltage signal V_{out}. The control signals decide which functionality is to be performed and depending on that, the input voltage V_{in} is transformed to the output voltage V_{out}. Table 1 presents the truth table which defines the functionality of the ULC.

A ULC is capable of performing three types of operations on the voltage signal: (1) level-up conversion, (2) level-down

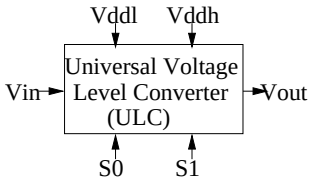


Figure 2. High-level view of the Universal Level Converter.

Table 1. Selection signals for programmability

Select Signal (S1, S0)		Type of Operation
0	0	Blocking
0	1	Level-down
1	0	Level-Up

conversion, and (3) blocking as needed for power management in DDNEMS. Level-down conversion is used to provide supply to the blocks of the sub-systems which operate at lower than battery voltage. Level-up conversion is applied as an interface where V_{DDl} (lower supply voltage) cells are driving V_{DDh} (higher supply voltage) cells or to provide supply to sub-systems operating at higher than the battery voltage. The blocking feature of the ULC is used to shut off the unused blocks of a circuit in the standby mode, thereby reducing standby leakage. The ULC can be programmed according to different requirements. For example, DDNEMS may use level-up conversion with blocking features to reduce short-circuit power and leakage power. DDNEMS may also use level-down conversion with the blocking features to minimize switching power, in addition to standby leakage.

3 Design of Universal Level Converter using High-κ/Metal-Gate Nano-CMOS Technology

3.1 Models for Power, and Delay Calculation of the ULC

3.1.1 Power and Leakage Models

The total power of a nano-CMOS circuit can be calculated as the summation of major components, like dynamic power, subthreshold leakage, and gate leakage. The use of HKMG transistors as technology for our design eliminates gate leakage. Thus, the power dissipation of the ULC circuit is calculated by the following expression:

$$P_{ULC} = P_{dynamic} + P_{subthreshold}. \quad (1)$$

The dynamic power dissipation of the circuit, which depends on loading conditions, can be calculated as [8]:

$$P_{dynamic} = \alpha C_L V_{dd}^2 f. \quad (2)$$

The subthreshold leakage of a nano-CMOS device is [10]:

$$I_{sub} = \mu_0 \left(\frac{\epsilon_{ox} W}{T_{ox} L_{eff}}\right) v_{therm}^2 e^{1.8} \times \exp\left(\frac{V_{gs} - V_{Th}}{S v_{therm}}\right) \times \left(1 - \exp\left(\frac{-V_{ds}}{v_{therm}}\right)\right). \quad (3)$$

This leakage current is exponentially dependent on V_{Th}, and increasing V_{Th} will decrease the leakage current substantially.

3.1.2 Delay Model

The delay of a CMOS device is [10]:

$$Delay \propto \left(\frac{C_L V_{dd}}{\mu\left(\frac{\epsilon_{ox}}{T_{ox}}\right)\left(\frac{W_{eff}}{L_{eff}}\right)(V_{dd} - V_{Th})^{\alpha}}\right). \quad (4)$$

In a ULC we have both up converters and down converters. Thus, the average delay of the ULC circuit is defined as:

$$Delay_{ULC} = \left(\frac{Delay_{up} + Delay_{down}}{2}\right). \quad (5)$$

The delay of the level converter is calculated from the 50% level of the input swing to 50% level of the output swing.

3.2 HKMG CMOS Modeling

We used the $32nm$ HKMG CMOS Predictive Technology Model (PTM) [14]. The PTM is well established and is able to predict the general trend of device attributes. In the absence of published data and other device models, PTM provides a timely and effective analysis approach. The simulation results obtained are highly accurate and the calculated data are of comparable accuracy to TCAD simulations which are typically time and computation intensive. For PTM based on BSIM4 models, two modes are adopted: (1) The model parameter in the model card that denotes relative permittivity (EPSROX) is changed, and (2) The equivalent oxide thickness (EOT) for the dielectric under consideration is calculated. The EOT is calculated so as to keep the ratio of relative permittivity over dielectric thickness constant using:

$$T_{ox}^{*} = \left(\frac{\kappa_{\mathrm{SiO_2}}}{\kappa_{gate}}\right) \times T_{gate}, \quad (6)$$

where κ_{gate} is the relative permittivity and T_{gate} is the thickness of the gate dielectric material other than SiO_2, while $\kappa_{\mathrm{SiO_2}}$ is the dielectric constant of $SiO_2 (= 3.9)$. For our design, we have taken $\kappa_{gate} = 21$ to emulate a HfO_2 based dielectric. The EOT is calculated to be $5nm$.

3.3 The Design Flow Using Dual-V_{Th} Based High-κ Technology

We followed the following design flow for optimal design of ULC using using dual-V_{Th} based HKMG technology. It may be noted that in SiO_2 based nano-CMOS technologies, gate-oxide leakage is a major contributor to power during ON, OFF,

and transient states of a circuit [7]. This may be overcome using the dual oxide technique, as proposed in [4]. This is a viable solution at the $45nm$ node technology. However, at sub-$45nm$ technologies (e.g., $32nm$ in this paper), this technique is not viable, and hence bulk-CMOS must be replaced by HKMG CMOS. This motivates us to use the HKMG nano-CMOS for the design of the ULC to completely eliminate gate leakage.

The second issue of power is subthreshold leakage. A dual-V_{Th} is adopted to reduce subthreshold leakage [1]. A higher V_{Th} in a transistor leads to lower subthreshold current. Hence we propose a dual-V_{Th} technique for the minimization of the subthreshold leakage in the ULC circuit. The power-hungry transistors are assigned a higher-V_{Th} value in this technique.

The power (including leakage) and delay of the entire ULC circuit are optimized using the optimization methodology; an algorithm is presented in Section 4. Hence, as the end result of this design flow, we obtain a thorough optimization of the ULC circuit for use in a multi-V_{DD} environment.

3.4 Circuit-Level Design of the ULC

For level-up conversion, we employ a cross coupled level converter, shown in Fig. 3. In this circuit, there are two cross-coupled PMOS transistors to form the circuit load. The cross-coupled PMOS transistors act as a differential pair [5]. Thus, when the output at one side is pulled low, the opposite PMOS transistor will be turned on and the output on that side will be pulled high. Below the PMOS load, there are two NMOS transistors that are controlled by the input signal V_{in} [8].

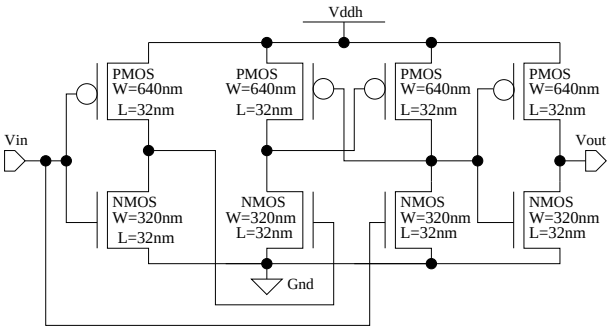


Figure 3. Circuit for up conversion.

We employ a differential input level converter for level-down voltage conversion. It has a differential input, which enables a stable operation at low voltage and high speed use [6]. The differential input also offers immunity against power supply bouncing. The circuit diagram is shown in Fig. 4.

Fig. 5 shows the transistor level circuit realization of the proposed ULC. This is achieved by stitching the individual sub-circuits together. The switches designed using transmission gates provide programmability. They are controlled by the control signals S1 and S0. In the baseline design we chose $W = 320nm, L = 32nm$ for NMOS and $W = 640nm, L = 32nm$ for the PMOS devices, respectively to achieve correct functionality. Each of the above sub-circuits of the ULC are thoroughly characterized through parametric, load, and power analysis, presented in Section 5.

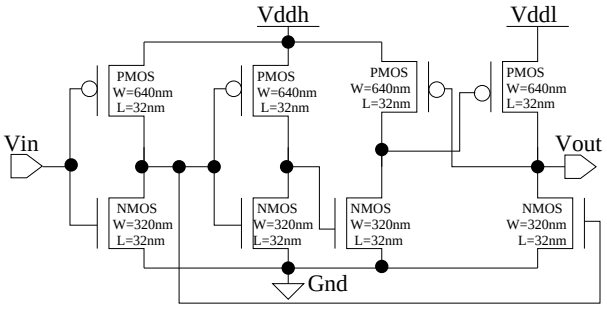


Figure 4. Circuit for down conversion.

4 The Proposed Optimization Approach

In the ULC, the power-hungry transistors are identified and are assigned higher V_{Th} values. Power-hungry NMOS are assigned 20% higher V_{Th} and power hungry PMOS are assigned 50% higher V_{Th} as compared to the nominal values specified for the technology node. We used Algorithm 1 for the power, leakage, and delay optimization of the ULC circuit. The inputs to the algorithm comprise of the circuit netlist, the objective set F ($P_{ULC}, Delay_{ULC}$) with its stopping criteria S (e. g., $S = 2\%$), and the design variable set D with its lower constraint C_{lower} and upper design constraint C_{upper}. The design variable set D comprises of the following: (1) W_{PMOSup}: width of PMOS transistors in level-up converter, (2) W_{NMOSup}: width of NMOS transistors in level-up converter, (3) $W_{PMOSdown}$: width of PMOS transistors in level-down converter, and (4) $W_{NMOSdown}$: width of NMOS transistors in level-down converter. The outputs of the algorithm are the optimized objective set $F_{optimal}$ satisfying the stopping criteria S and the optimal values of the design variable set $D_{optimal}$ within C_{lower} and C_{upper}.

Algorithm 1 Proposed optimization algorithm for ULC design

1: **Input:** Circuit netlist, Objective set $F = [f_1, f_2....f_n]$, Stopping criteria S, design variable set $D = [d_1, d_2....d_n]$, Lower/Upper design constraint C_{lower}, C_{upper}.
2: **Output:** $F_{optimal}, D_{optimal}$ for $S = \pm\sigma$. {where $1\% \leq \sigma \leq 5\%$}
3: Run initial simulation in order to obtain feasible values of design variables for the given Objective set.
4: **while** ($C_{lower} < D < C_{upper}$) **do**
5: Use finite difference perturbation to generate new set of design variables $D' = D + \delta D$.
6: Compute $F(D')$ = [P_{ULC}, $Delay_{ULC}$].
7: **if** ($S == \pm\sigma$) **then**
8: **return** $D_{optimal} = D'$, where $D' = [W_{PMOSdown}, W_{PMOSup}, W_{NMOSdown}, W_{NMOSup}]$.
9: **end if**
10: **end while**
11: Obtain optimal values for design variable set $D_{optimal}$.
12: Compute optimized Objective set $F_{optimal}$ for the ULC.

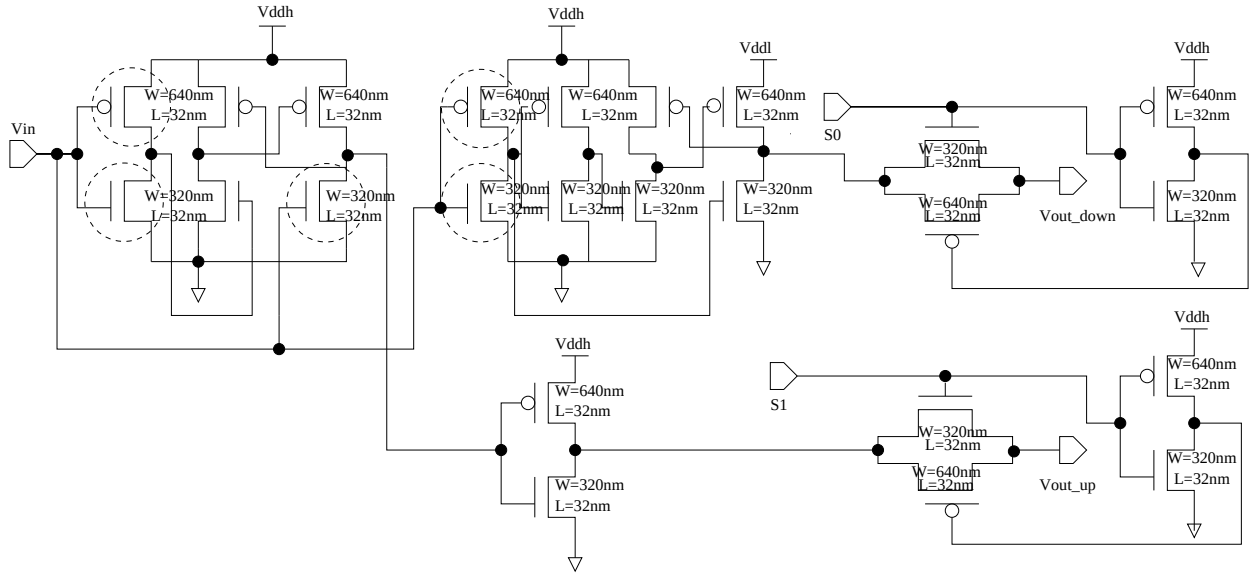


Figure 5. Transistor level circuit realization of the ULC. The circled transistors are identified as power-hungry and subjected to dual-V_{Th} technique.

During optimization, a simulation is run using the initial values of D, and the value of F is calculated, to determine whether the initial values are feasible for the given $F_{optimal}$. In the next iteration, the design variable set (D) values are changed accordingly, to achieve the required $F_{optimal}$. This is called *finite difference perturbation*. The circuit is simulated again using this new design variable set. This process continues till $F_{optimal}$ meets with stopping criteria S. This algorithm is based upon the Feasible Sequential Quadratic Programming algorithm. The optimized objective set $F_{optimal}$ is presented in Table 2, and the $D_{optimal}$ values are presented in Table 3.

Table 2. Optimized values of objective set $F_{optimal}$

Objective	Value
P_{ULC}	$5\mu W$
$Delay_{ULC}$	$1.6ns$

Table 3. Design variable values for optimal power and delay

D	C_{lower}	C_{upper}	$D_{optimal}$
W_{PMOSup}	$64nm$	$640nm$	$64nm$
W_{NMOSup}	$64nm$	$640nm$	$640nm$
$W_{PMOSdown}$	$64nm$	$640nm$	$64nm$
$W_{NMOSdown}$	$64nm$	$640nm$	$640nm$

5 Characterization of the ULC

5.1 Functional Simulation

The functional simulation of the ULC is shown in Fig. 6. When the control signals $S1$ and $S0$ are in the "10" state, V_{in} is $0.595V$ ($V_{ddl} = 85\%$ of V_{dd}), and V_{out} is $0.7V$(V_{dd}), i.e., level-up conversion is being performed. When the control signals $S1$ and $S0$ are in the "01" state, V_{in} is $0.7V$ (V_{dd}), and V_{out} is $0.595V$ (V_{ddl}), i.e., level-down conversion of the input signal is being performed. When $S1$ and $S0$ are "00", the input signal V_{in} is blocked. We observe that the 3 functions level-up conversion, level-down conversion and blocking are performed depending on values of $S1$ and $S0$. This can be verified from Table 1. Thus, the proposed converter can also be programmed by external stimuli through the RF interface of DDNEMS.

5.2 Characterization

We have characterized the ULC using 3 types of analysis: parametric analysis, load analysis and power analysis to check the robustness of the design. It was found that the design is stable under varying operating conditions.

5.2.1 Parametric Analysis

The parametric analysis involves testing of the up-conversion and down-conversion of the proposed ULC. For the up-conversion, V_{in} is varied from $0.1V$ to $0.595V$ in steps of $0.05V$ and the output of ULC is observed. As shown in Fig. 7(a), a stable up-conversion is performed for voltages as

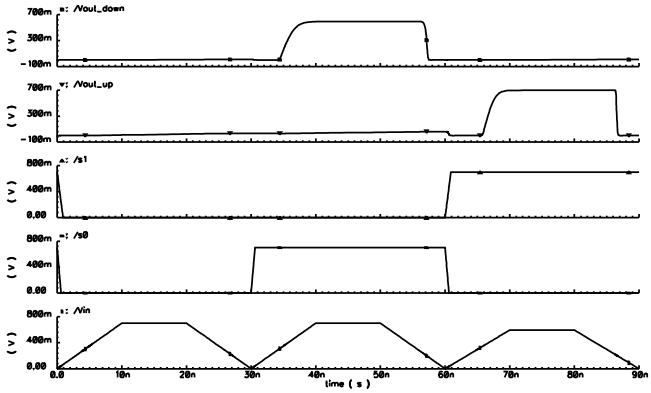


Figure 6. Functional simulation of the ULC. It verifies the truth table given in Table 1, demonstrating its programmability capability. The bottom-most curve is the input, the 2 top-most curves are the outputs, and the middle 2 signals are control signals. The sequence of operations is block, step-down, and step-up.

low as $0.35V$ (50% of V_{DD}). For the down-conversion, V_{in} is varied from $0.1V$ to $0.7V$ in steps of $0.05V$. The output in Fig. 7(b) shows that stable down-conversion is performed for voltages greater than $0.35V$.

5.2.2 Load Analysis

Load analysis is used to determine the excess load the ULC can drive. The value of nominal load capacitance (C_{Load}) is taken as 10 times the gate capacitance of the PMOS transistors (C_{gg}) in the ULC. Thus we have the following expression:

$$C_{Load} = 10 \times \left(\frac{\kappa \times W_{pmos} \times L_{pmos}}{T_{gate}} \right). \qquad (7)$$

The nominal value of C_{Load} is calculated as $82fF$. For the load analysis, the load capacitance is varied from $50fF$ to $120fF$ in steps of $10fF$. These values of load capacitance represent realistic loads [13]. The results as shown in Fig. 8(a) and Fig. 8(b) demonstrates that the circuit produces a stable and expected output voltage under varying load conditions.

5.2.3 Power Analysis

The power analysis of the ULC is performed at a capacitive load of $50fF, 82ffF$ and $120fF$. Table 4 shows the values obtained. The input rise/fall times and switching frequency are also recorded. It is evident that there is not much difference in the power consumption with varying loads. The power measurement includes the dynamic power and subthreshold leakage in the ULC circuit, as the gate-oxide leakage is measured to be negligible.

Table 4. Power consumption of the ULC

Input Rise/Fall Time (ns)	Input Switching Freq. (MHz)	Capacitive Load (fF)	Avg. Power Consumption (μW)
10	33.33	50	4.988
10	33.33	82	5
10	33.33	120	5.8

6 Summary, Conclusions, and Future Research

In this paper, we proposed a novel design called ULC for DDNEMS architecture. The ULC is capable of performing three types of distinct level converting operations on the input signal: up-conversion, down-conversion and blocking. This makes the proposed ULC highly suitable for use in the context of dynamic power management in a multi-V_{dd} environment.

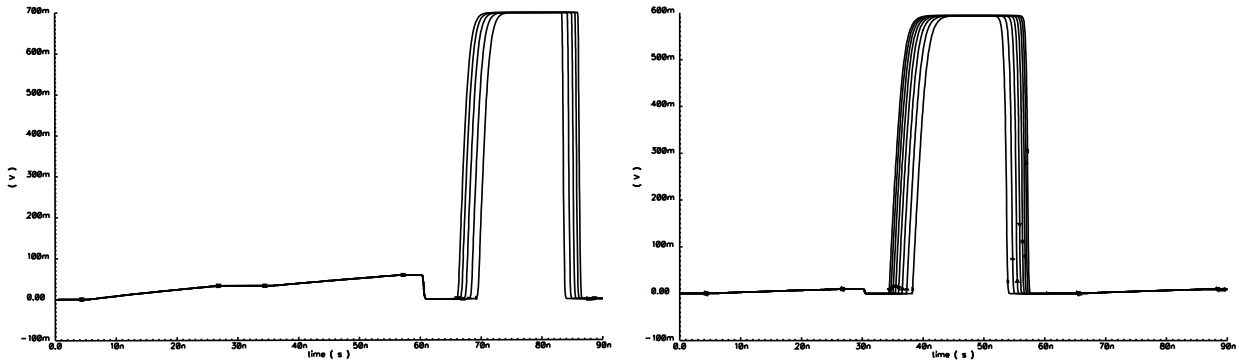
An HKMG design of the ULC is presented. This ULC is subjected to further power minimization by applying a dual-V_{Th} technique. Finally, an algorithm is discussed and adapted for the power and delay optimization of the entire ULC circuit. The robustness of the ULC is tested using parametric, load and power analysis.

The average power consumption of the level converter is $5\mu W$ making it the lowest power design reported. There are several works on level converter design available in the literature. A comparative perspective is presented in Table 5. It is evident that this is the first ever reported level converter implemented using $32nm$ HKMG nano-CMOS. The proposed ULC consumes the least power compared to other level converters presented. It can also be seen from the table that existing circuits perform a specific task, either up or down conversion, and are not programmable, unlike the ULC which can perform multiple tasks.

Table 5. Comparative perspective of related research

Reference	Technology	Power	Delay	Conversion
Ishihara [5]	$Bulk\ 130nm$	–	$127ps$	Up and down
Yu [13]	$Bulk\ 350nm$	$220.57\mu W$	–	Level-up
Sadeghi [9]	$Bulk\ 100nm$	$10\mu W$	$1ns$	Level-up
Kanno [6]	$Bulk\ 140nm$	–	$5ns$	Level-down
This Work	High-κ $32nm$	$5\mu W$	$1.6ns$	Up/Down/Block

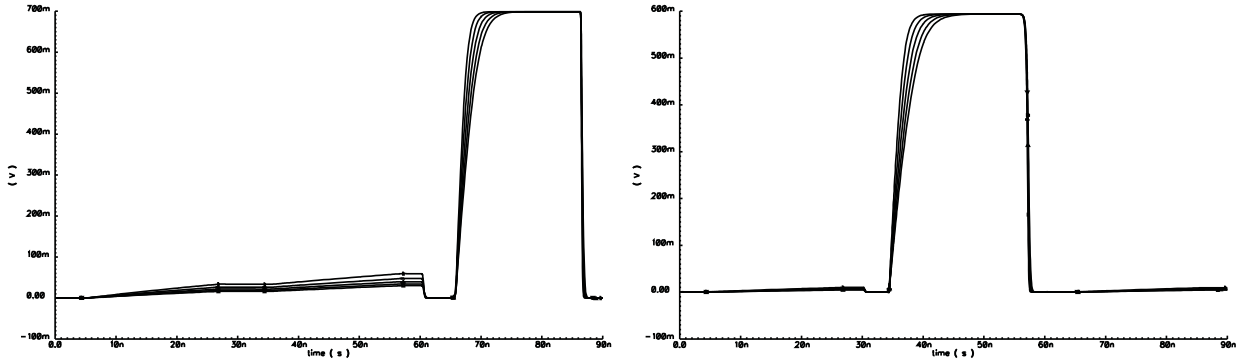
Future work will include considering gate-induced junction leakage (GIDL) in the optimization process. As part of future work, we plan to design the ULC using other nanoscale technologies, such as double gate FET (DGFET), Carbon Nano-Tube FET (CNTFET), etc., and analyze the effects on the performance metrics.



(a) For level-up conversion

(b) For level-down conversion

Figure 7. Parametric analysis showing the output (V_{out}) waveforms.



(a) For level-up conversion

(b) For level-down conversion

Figure 8. Output under varying load conditions ($C_L = 50fF$ to $120fF$). ULC provides stable output voltage even though the loading condition changes.

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