A PVT Aware Accurate Statistical Logic Library for High-κ Metal-Gate Nano-CMOS

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Abstract

The semiconductor industry is headed towards a new era of scaling and uncertainty with new key building blocks for the next-generation chips, the high-κ metal-gate transistor. There is a need for statistical characterization of high-κ metal-gate digital gates as a function of process parameter variations to make them available for designers. In this paper, we present a methodology for PVT aware high-κ metal-gate logic library creation while considering the variability effect in 15 parameters. First, statistical models for GIDL current ($\hat{I}_{GIDL}$), off-current ($\hat{I}_{OFF}$) and drive current ($\hat{I}_{ON}$) are presented at the device level. This is followed by statistical characterization of logic cells at room temperature. Data for subthreshold current ($\hat{I}_{sub}$), $\hat{I}_{GIDL}$, dynamic current ($\hat{I}_{dyn}$) and delay is presented. This is followed by results for PVT aware characterization of logic cells. To the best of the authors' knowledge, this is the first research which provides a PVT aware statistical characterization for high-κ metal-gate nano-CMOS based logic gates.

Keywords

Nanoscale CMOS, High-κ metal-gate technology, Monte Carlo, Gate Induced Drain Leakage (GIDL), Subthreshold Leakage, Dynamic Power

1 Introduction and Contributions

The success of the semiconductor industry relies on the continuous improvement of integrated circuit performance which is achieved by device scaling. The superior properties of SiO_2 allow the fabrication of properly working devices with SiO_2 layers as thin as $1.5nm$. However, further scaling of SiO_2 layer thickness leads to tunneling gate leakage [2, 14]. The solution to this problem is to use a gate insulator with a higher dielectric constant κ than that of SiO_2 ($= 3.9$) and metal gate [9]. This reduces the gate leakage and improves the reliability of the gate. In this paper, we refer to this non-classical nano-CMOS structure as high-κ metal-gate (HKMG) nano-CMOS. However, the use of HKMG causes a significant gate-induced drain leakage (GIDL) current (I_{GIDL}) in addition to subthreshold leakage (I_{sub}) [12]. I_{GIDL} is high mainly due to two reasons:

(1) The metal gate introduces a high gate effective work function which leads to high electric field and a high GIDL current [16].

(2) The high-κ gate dielectric and SiO_2 spacers meet at the surface of the drain region, causing a high electric field leading to a high GIDL current [8].

It is widely recognized that the uncontrollable statistical variability in device characteristics represents major challenges to scaling and integration for present and next generation nano-CMOS transistors and circuits. This in turn demands revolutionary changes in the way in which future integrated circuits and systems are designed. Strong links must be established between circuit design, system design and fundamental device technology to allow circuits and systems to accommodate the increasing variability. The major sources of variability are: process variation (P), supply voltage (V), and operating temperature (T) which may be due to the environment, through self-heating effects or a combination of the two.

Unfortunately, PVT variability makes it hard to achieve "safe" integrated circuit designs in nanometer technologies. This is because PVT variability causes fluctuation in timing as well as power for System-on-Chip (SoC) designs [7]. Till now very few efforts have been made at addressing the effect of PVT variability on power, leakage and delay estimation. It is necessary to express each of these factors as a function of process, voltage and temperature (PVT):

$$\hat{Y} = f(P, V, T), \tag{1}$$

where $\hat{Y}$ is power, leakage or delay. Also, for nano-CMOS, a shift from deterministic to probabilistic design is required to accommodate the effects of device variability, which involves extensive use of statistical techniques. The challenges for such modeling are several:

(1) There is a need for realistic evaluation of circuit delay and power variability, considering processes variation and correlations between them.

(2) There is a need to directly relate variability in circuit parameters to variability in process parameters.

(3) There is a need to migrate from corner-based timing to statistical timing for accuracy.

To address these challenges, we propose a Monte Carlo based technique to create a PVT aware library, which has the following advantages:

(1) Accurate estimation of power, leakage and delay in emerging non-classical CMOS structures is possible.

(2) A closed form function relating the output to input is not required, which otherwise would have been cumbersome for the large number of parameters considered in this paper.

(3) Parameters take on more realistic or practical extreme values resulting in densely designed, reliable, manufacturable circuits.

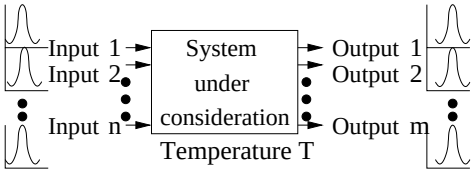


Figure 1. Logic level modeling for PVT aware statistical library.

Figure 1 shows the logic level modeling for a system under consideration for which a PVT aware library is to be created. The inputs to the system are probability density functions (PDFs) of the sources of variability. In this paper, the system under consideration is logic gates, as the goal is a logic library creation. The input PDFs are denoted as $\hat{X}_j$, where $j = 1 \rightarrow n$. The logic gate is then subjected to Monte Carlo simulations. The output of the system are the PDFs for outputs as functions of the inputs, which are process parameters (P) and voltage (V), at a specific temperature (T). The output PDFs are denoted as $\hat{Y}_i$, where $i = 1 \rightarrow m$. These simulations run for different temperatures and a PVT aware library is obtained.

The novel contributions of this paper are as follows:

(1) A methodology for HKMG logic library creation is presented.

(2) The effect of process variations has been considered during logic library creation.

(3) Device level characterization of HKMG NMOS and PMOS transistors is presented.

(4) An HKMG logic library with statistical characterization at room temperature (27°C) is presented.

(5) A PVT aware HKMG statistical logic library is presented.

The rest of the paper is organized as follows: Section 2 discusses related research. The proposed methodology for logic library creation is discussed in section 3 highlighting the various sources of variability. The power, leakage and delay models used in this paper are presented in section 4. Section 5 presents the statistical characterization of HKMG NMOS and PMOS devices. Section 6 presents the statistical characterization of the HKMG logic library at room temperature. PVT characterization results are presented in section 7. Section 8 discusses applications of the statistical logic library. The paper concludes in section 9.

2 Related Prior Research

Logic libraries are required for fast design exploration. Statistical characterization of logic gates as a function of process and environment parameter variations is required [22, 14, 20]. To minimize power consumption and maximize timing performance, design teams require rapid library characterization and accurate modeling for specific operating conditions [18]. A large number of logic libraries are available in the market today for standard CMOS [3, 6]. However, as the industry moves away from classical CMOS, characterized standard cells for non-classical technologies will be required. This paper is a futuristic effort in this direction.

3 The Proposed Methodology For Logic Library

3.1 Sources of Variation and Nature of Variability

In this paper, we have considered 15 different parameters for variation. The parameters for variability are as follows: (1) V_{dd}: supply voltage (V), (2) V_{Thn}: NMOS threshold voltage (V), (3) V_{Thp}: PMOS threshold voltage (V), (4) t_{gaten}: NMOS gate dielectric thickness (nm), (5) t_{gatep}: PMOS gate dielectric thickness (nm), (6) L_{effn}: NMOS channel length (nm), (7) L_{effp}: PMOS channel length (nm), (8) W_{effn}: NMOS channel width (nm), (9) W_{effp}: PMOS channel width (nm), (10) N_{gaten}: NMOS gate doping concentration (cm^{-3}), (11) N_{gatep}: PMOS gate doping concentration (cm^{-3}), (12) N_{chn}: NMOS channel doping concentration (cm^{-3}), (13) N_{chp}: PMOS channel doping concentration (cm^{-3}), (14) N_{sdn}: NMOS source/ drain doping concentration (cm^{-3}), (15) N_{sdp}: NMOS source/ drain doping concentration (cm^{-3}). These parameters are not necessarily independent. The statistical variability in most of these parameters can be modeled as Gaussian distributions [13].

3.2 Statistical Logic Library Characterization Flow

We present the proposed methodology followed in this paper for a PVT aware HKMG logic library creation, shown in figure 2. The input to the design flow is a $32nm$ HKMG model

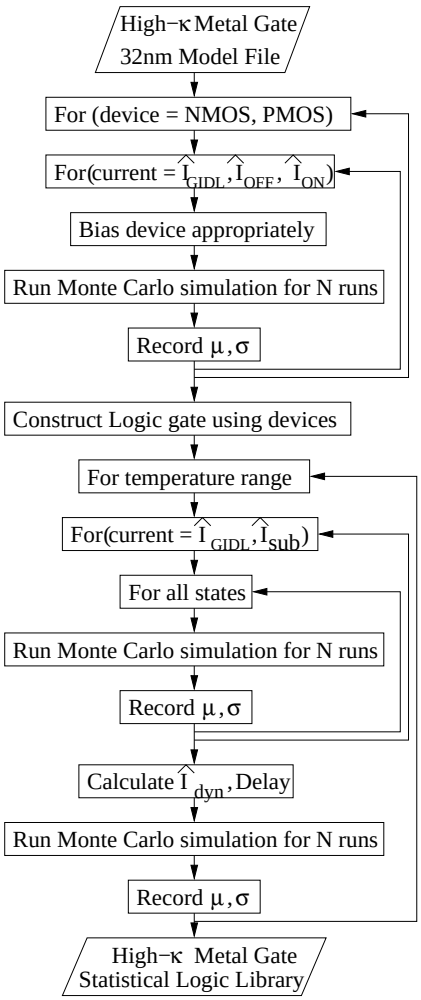


Figure 2. The proposed methodology for PVT aware statistical logic library.

file. The first step in the flow involves the statistical characterization at device level i.e. NMOS and PMOS for $\hat{I}_{GIDL}$, $\hat{I}_{OFF}$ and $\hat{I}_{ON}$. For measurement of each current, the device has to be biased appropriately. The biasing conditions are discussed in detail in section 5. Monte Carlo simulations are run on the device to obtain statistical data (mean μ, variance σ^2) for each device. The second step in the flow involves PVT aware characterization of logic gates. At a given temperature, the logic gate under consideration is biased for each state and Monte Carlo simulations are performed to obtain the statistical data. We present state dependent data for $\hat{I}_{GIDL}$ and $\hat{I}_{sub}$. This is followed by measurement of $\hat{I}_{dyn}$ and delay.

4 Power, Leakage, and Delay Models

4.1 Gate Induced Drain Leakage (GIDL)

GIDL is caused by the existence of a high electric field at the drain junction of MOS transistors [8]. In NMOS transistors, GIDL takes place when the gate is at a lower potential than the drain. This causes significant band bending in the drain, allowing electron-hole pair generation through avalanche multiplication and band to band tunneling. GIDL has a strong impact in HKMG transistors. Equation 2 shows the BSIM4 expression used for calculating GIDL [1]:

$$I_{GIDL} = A \times W_{effCJ} \times N_f \times \left(\frac{V_{ds} - V_{gs} - E}{3 \times T_{gate}}\right) \times \exp\left(\frac{-3 \times T_{gate} \times B}{-V_{ds} - V_{gs} - E}\right) \times \left(\frac{V_{db}^3}{C + V_{db}^3}\right), \quad (2)$$

where V_{db} is the drain to body voltage, V_{ds} is the drain to source voltage, V_{gs} is the effective gate voltage, W_{effCJ} is the effective width of the drain diffusions, N_f is the number of fingers of the transistor and A, B, C and E are all BSIM4 GIDL leakage-based parameters which have been fitted to existing data [16, 8, 12].

4.2 Subthreshold Leakage

The subthreshold leakage through a CMOS device is modeled as follows [1, 17]:

$$I_{sub} = I_0 \times \left(1 - \exp\left(\frac{-V_{ds}}{v_{therm}}\right)\right) \times \exp\left(\frac{V_{gs} - V_{Th} - V_{off}}{S \times v_{therm}}\right), \quad (3)$$

where I_0 is a constant dependent upon device parameters for a given technology, v_{therm} is the thermal voltage, V_{Th} is the threshold voltage, V_{off} is the offset voltage which determines the channel current at V_{gs} = 0, S is the subthreshold swing factor, V_{gs} is gate-to-source voltage, and V_{ds} is the drain-to-source voltage.

In a nano-CMOS device, the threshold voltage V_{Th} is scaled along with the supply voltage in order to maintain performance. However, the systematic reduction in V_{Th} causes the subthreshold current to increase exponentially, as can be seen from equation 3.

4.3 Dynamic Current

The dynamic power consumption of a circuit is expressed as follows [4]:

$$P_{dyn} = s \times C_L \times V_{dd}^2 \times f, \quad (4)$$

where the activity factor s captures how many devices are active on any particular clock cycle, C_L is the total switched capacitive load, V_{dd} is the supply voltage and f is the frequency of the clock. This power dissipation depends on loading condition and not the device features. The current associated with P_{dyn} is I_{dyn} and is calculated as the average of the current through the load capacitance C_L, given as:

$$I_{dyn} = \lim_{T \to \infty} \frac{1}{T} \int_0^T I_c(t) \times dt, \quad (5)$$

where $I_c(t)$ is the current through the load capacitance C_L.

4.4 Propagation Delay

The propagation delay (T_{PD}) of a device is approximately calculated as follows [19]:

$$T_{PD} = \beta \times \left(\frac{C_L V_{dd}}{\mu \left(\frac{\kappa_{gate}}{T_{gate}}\right) \left(\frac{W_{eff}}{L_{eff}}\right) (V_{dd} - V_{Th})^{\alpha}} \right), \quad (6)$$

where β = a technology dependant constant , μ = electron surface mobility and α is the velocity saturation index. The delay of logic cells is calculated as:

$$Delay = \left(\frac{T_{PDLH} + T_{PDHL}}{2} \right), \quad (7)$$

where, T_{PDLH} refers to the low to high transition, and T_{PDHL} refers to the high to low transition of the output.

4.5 Method to Model high-κ at Device Level

A $32nm$ Predictive Technology Model (PTM) available at [24] is used for modeling HKMG transistors. PTM provides a timely and effective analysis in the absence of published data and other device models. For high-κ dielectric modeling using PTM, two methods are used: (1) The model parameter in the model card that denotes relative permittivity (EPSROX) is changed or (2) The equivalent oxide thickness (EOT) for the dielectric under consideration is calculated. The EOT is calculated by:

$$EOT = \left(\frac{\kappa_{\mathrm{SiO_2}}}{\kappa_{gate}} \right) \times t_{gate}, \quad (8)$$

where κ_{gate} is the relative permittivity and t_{gate} is the thickness of the gate dielectric material other than SiO_2, while κ_{SiO_2} is the dielectric constant of SiO_2 $(= 3.9)$. We have taken $\kappa_{gate} = 21$ and $t_{gate} = 5nm$ to emulate a HfO_2 based dielectric. EOT is calculated to be $0.9nm$.

5 Variation Aware Device Level Characterization

Different biasing conditions have been used for device level characterization of the currents discussed in section 4. For reference, we have: (1) $V(D)$ = voltage across drain, (2) $V(G)$ = voltage across gate, (3) $V(S)$ = voltage across source, (4) $V(B)$ = voltage across bulk. For the NMOS device, for measuring I_{GIDL} and I_{OFF}, $V(D)$ = $0.7V$, $V(G)$= $0V$, $V(S)$ = $0V$ and $V(B)$ = $0V$. For measuring I_{ON}, $V(D)$ = $0.7V$, $V(G)$= $0.7V$, $V(S)$ = $0V$ and $V(B)$ = $0V$. For the PMOS device, for measuring I_{GIDL} and I_{OFF}, $V(D)$ = $0V$, $V(G)$= $0.7V$, $V(S)$ = $0.7V$ and $V(B)$ = $0.7V$. For measuring I_{ON}, $V(D)$ = $0V$, $V(G)$= $0V$, $V(S)$ = $0.7V$ and $V(B)$ = $0.7V$.

A Monte Carlo analysis with N =1000 runs has been run, with all the process parameters from section 3.1. Each of these process parameters is assumed to have a Gaussian distribution [10] with mean taken as the nominal values specified in the PTM [24] and standard deviation as 10% of the mean [21, 23]. $\hat{I}_{GIDL}$, $\hat{I}_{OFF}$ and $\hat{I}_{ON}$ exhibit lognormal distribution (figures 3(a), 3(b), and 3(c). Only the results for the NMOS transistors is shown. The PMOS data follow the same trends. The mean and standard deviation values for both transistor types are recorded in Table 1.

Table 1. Statistical data for HKMG devices

PDF of Currents		NMOS Device	PMOS Device
$\hat{I}_{GIDL}$	μ	-10.5637	-10.1050
	σ	1.6211	0.9927
$\hat{I}_{OFF}$	μ	-7.6789	-7.4682
	σ	0.9203	1.1446
$\hat{I}_{ON}$	μ	-4.1247	-4.1694
	σ	0.1206	0.1632

6 Variation Aware State Dependent Logic Level Characterization

In this section we present the results for HKMG logic cells at room temperature ($27°C$). The results are presented for inverter and NAND gates for brevity. We present state dependent data for $\hat{I}_{GIDL}$ and $\hat{I}_{sub}$ as they lead to accurate leakage estimation. As I_{dyn} depends primarily on the switching of the logic gates, we present average data for $\hat{I}_{dyn}$ as per equation 5. C_L is taken as 10 times C_{gg} (gate capacitance of PMOS).

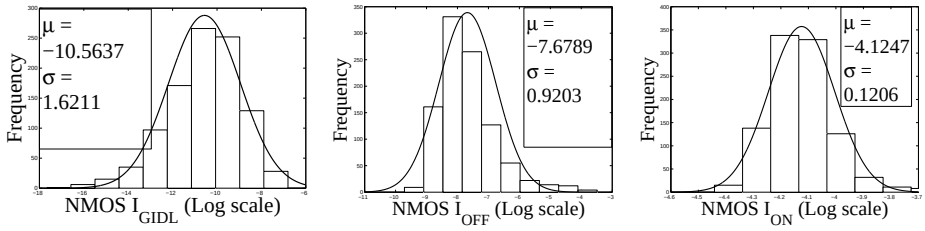
Tables 2 and 3 summarize the statistical data for the various currents measured in an inverter and a NAND gate. Results for only two gates are shown for brevity but the entire library is characterized following the same procedure. The direction of various currents in the NAND gate for each state are shown in figures 4(a), 4(b), 4(c), 4(d) and the distribution plots for these currents are shown in figures 5(a) to 6(j).

7 PVT Aware Logic Level Characterization

This section presents the results for PVT aware logic library. Simulations at 0°C, +50°C, +100°C, +125°C are considered. It can be seen that $\hat{I}_{GIDL}$ does not show strong dependence on temperature (figure 7(a)), while $\hat{I}_{sub}$ shows an increase in the mean (μ) value with increasing temperature (figure 7(b)). This is due to dependence of $\hat{I}_{sub}$ on V_{Th}, which depends strongly upon temperature. Delay also shows an increasing trend with temperature (figure 7(d). $\hat{I}_{dyn}$ is measured over one cycle of operation, as per equation 5. $\hat{I}_{dyn}$ remains almost constant with temperature, because for one cycle theoretically, $\hat{I}_{dyn}$ does not depend on frequency [11]. The statistical results are summarized in Table 4. For brevity, the results for NAND gate are presented. $\hat{I}_{GIDL}$ and $\hat{I}_{sub}$ data are presented for state "00".

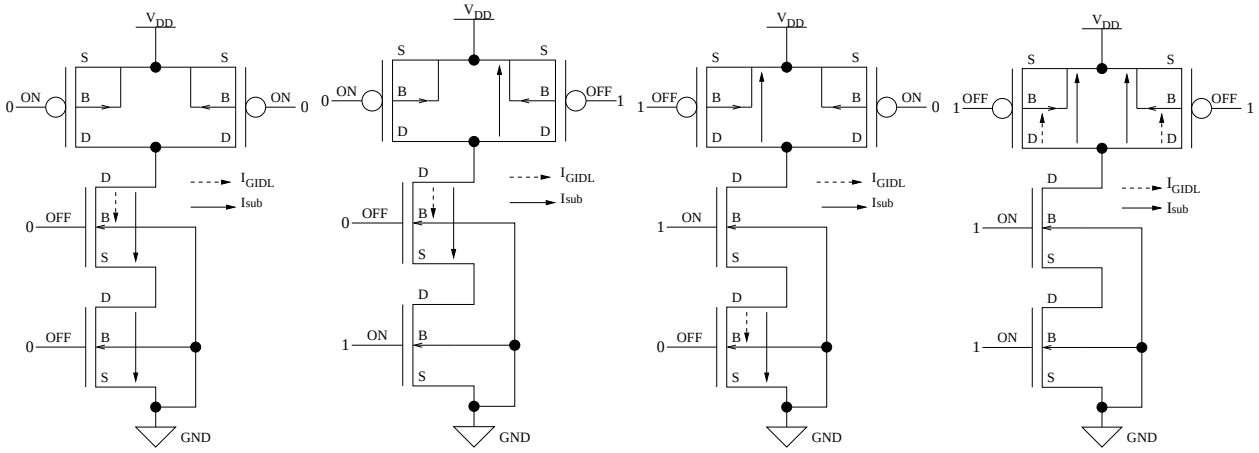
8 Applications For The Statistical Logic Library

Current circuit design methodologies, which depend on the existence of deterministic and uniform devices with no consid-



(a) GIDL current (b) OFF current (c) ON current

Figure 3. Distribution of $\hat{I}_{GIDL}$, $\hat{I}_{OFF}$, and $\hat{I}_{ON}$ for HKMG NMOS.



(a) State "00" (b) State "01" (c) State "10" (d) State "11"

Figure 4. Flow of I_{sub} and I_{GIDL} for a high-κ NAND gate for different states. The dotted line shows I_{GIDL} and the solid line represents I_{sub} flow. I_{GIDL} flows from drain to bulk, whereas I_{sub} flows from drain to source.

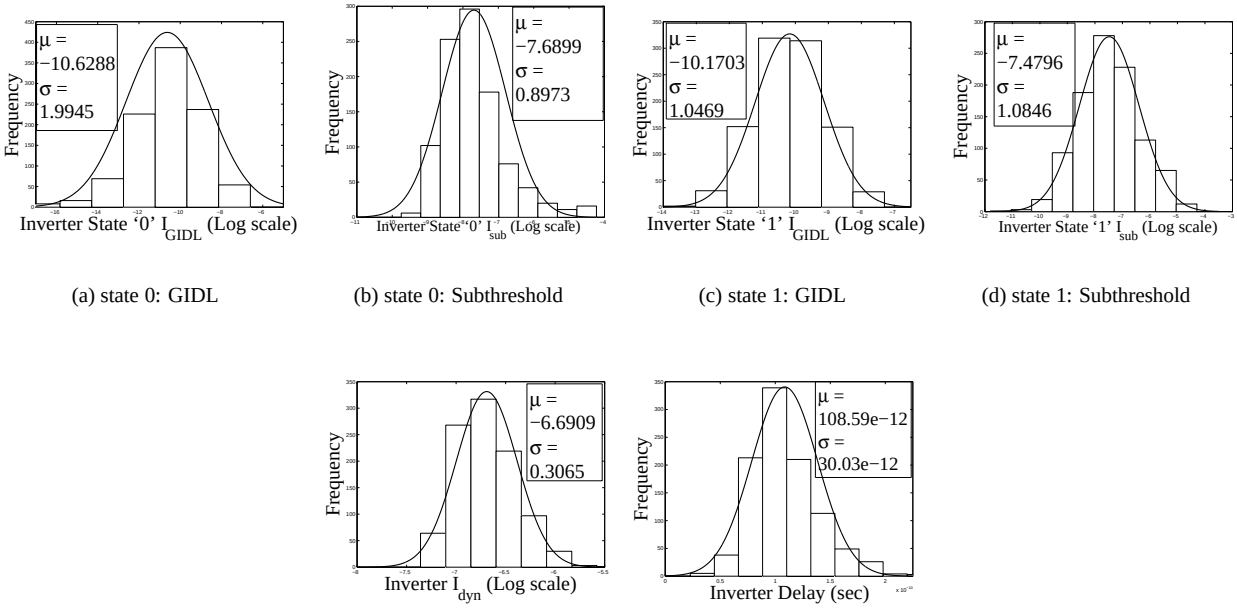
Table 2. Statistical state dependent data for an inverter.

PDF of Currents / Delay		'0'	'1'
$\hat{I}_{GIDL}$	μ	-10.6288	-10.1703
	σ	1.9945	1.0469
$\hat{I}_{sub}$	μ	-7.6899	-7.4796
	σ	0.8973	1.0846
$\hat{I}_{dyn}$	μ	-6.6909	
	σ	0.3065	
Delay	μ	108.59ps	
	σ	30.03ps	

Table 3. Statistical state dependent data for a NAND.

PDF of Currents / Delay		"00"	"01"	"10"	"11"
$\hat{I}_{GIDL}$	μ	-10.5409	-10.5779	-13.3605	-10.0153
	σ	1.6280	1.6377	1.6670	1.6247
$\hat{I}_{sub}$	μ	-8.4793	-7.6933	-7.9148	-7.8814
	σ	0.6193	0.8815	0.7913	1.0967
$\hat{I}_{dyn}$	μ	-6.5458			
	σ	0.2203			
Delay	μ	126.37ps			
	σ	29.72ps			

eration for either power consumption or probabilistic behavior, will no longer be sufficient to design robust circuits. This paper provides statistical state dependent characterization data for logic cells. The issue of providing characterization data for systems built using these logic cells is not in the scope of this paper. However, the data provided in this paper will be useful at the system level when a probabilistic analysis is carried out. In [15], the authors characterize datapath components using a structural HDL. The data presented in this paper can also be useful for probabilistic-CMOS [5] where the analysis is done using probability distribution functions (PDFs), instead of working with actual values.



(a) state 0: GIDL (b) state 0: Subthreshold (c) state 1: GIDL (d) state 1: Subthreshold

(e) Avg. : I_{dyn} (f) Delay

Figure 5. Distributions of GIDL ($\hat{I}_{GIDL}$), subthreshold ($\hat{I}_{sub}$), and dynamic ($\hat{I}_{dyn}$) current, and delay for HKMG an inverter.

Table 4. PVT aware statistical data for HKMG a NAND logic cell.

Temp	PDF of $\hat{I}_{GIDL}$			PDF of $\hat{I}_{sub}$			PDF of $\hat{I}_{dyn}$			PDF of Delay		
(° C)	μ	σ	$\frac{\sigma}{\mu}$ %	μ	σ	$\frac{\sigma}{\mu}$ %	μ	σ	$\frac{\sigma}{\mu}$ %	μ	σ	$\frac{\sigma}{\mu}$ %
0	-10.5398	1.6230	15.4	-8.9032	0.6763	7.6	-6.5504	0.2184	3.3	126.41 ps	29.61 ps	23.42
50	-10.5418	1.6325	15.5	-8.1738	0.5784	7.1	-6.5442	0.2210	3.4	127.19 ps	30.12 ps	23.68
100	-10.5443	1.6432	15.6	-7.6394	0.5070	6.6	-6.5441	0.2205	3.4	131.55 ps	31.52 ps	23.96
125	-10.5457	1.6490	15.6	-7.4228	0.4781	6.4	-6.5439	0.2197	3.4	134.8 ps	32.32 ps	23.98

9 Conclusions and Future Directions of This Research

We have presented a methodology for a PVT aware HKMG standard cell library creation while considering the effect of process variations, in this paper. Device level characterization for HKMG NMOS and PMOS transistors for drive current ($\hat{I}_{ON}$), off-current ($\hat{I}_{OFF}$) and GIDL current ($\hat{I}_{GIDL}$) has been done, modeled using $32nm$ PTM models. This is followed by PVT aware statistical characterization of standard cells. The state dependent data for $\hat{I}_{sub}$, $\hat{I}_{GIDL}$ and dynamic current ($\hat{I}_{dyn}$) are presented. As part of future work, we plan to implement similar logic libraries for other non-classical CMOS technologies such as double gate FET and Carbon Nanotubes and analyze their performance.

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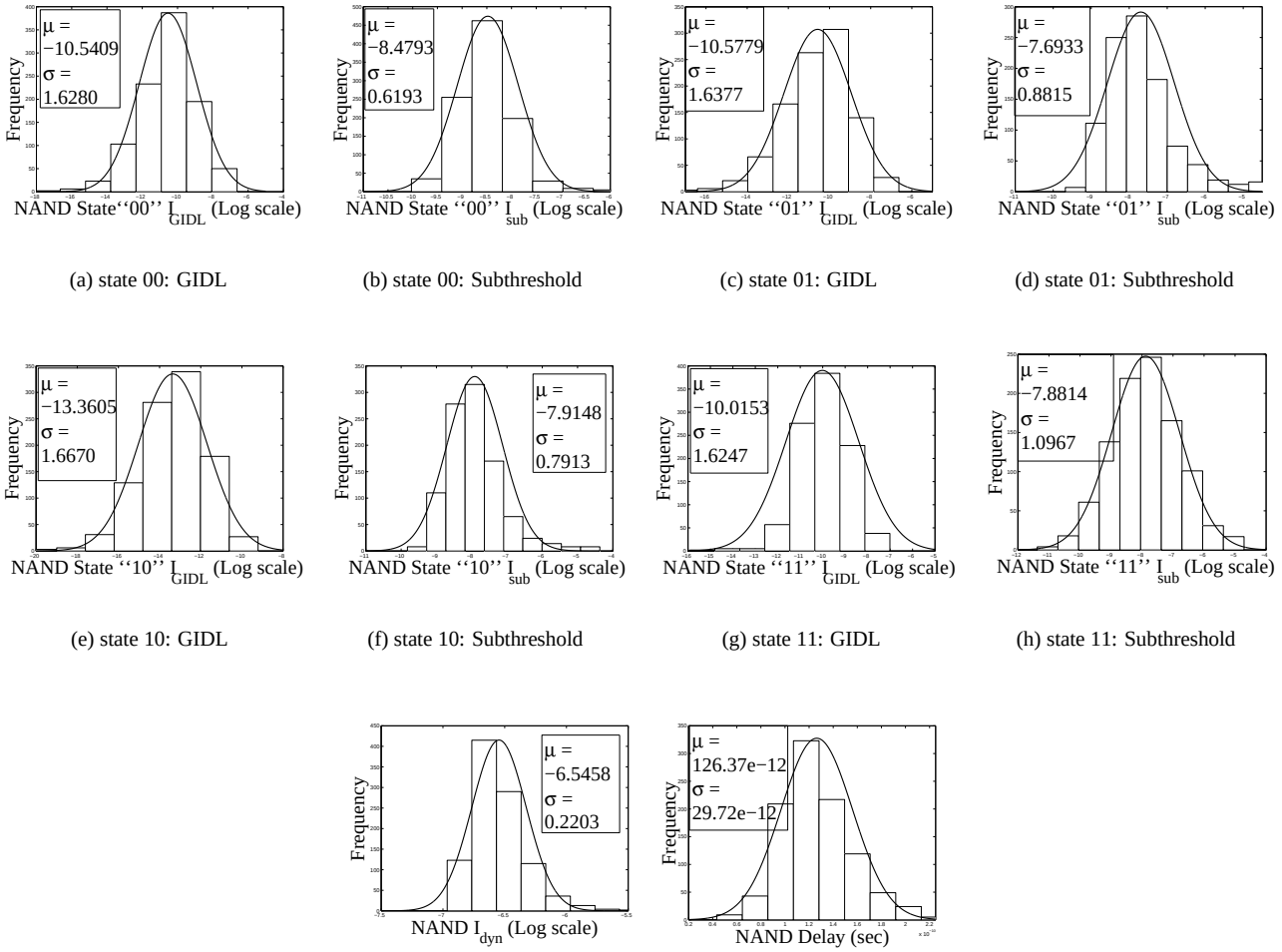

(a) state 00: GIDL (b) state 00: Subthreshold (c) state 01: GIDL (d) state 01: Subthreshold

(e) state 10: GIDL (f) state 10: Subthreshold (g) state 11: GIDL (h) state 11: Subthreshold

(i) Avg. : I_{dyn} (j) Avg. : Delay

Figure 6. Distributions of GIDL ($\hat{I}_{GIDL}$), subthreshold ($\hat{I}_{sub}$), and dynamic ($\hat{I}_{dyn}$) current, and delay for a HKMG NAND.

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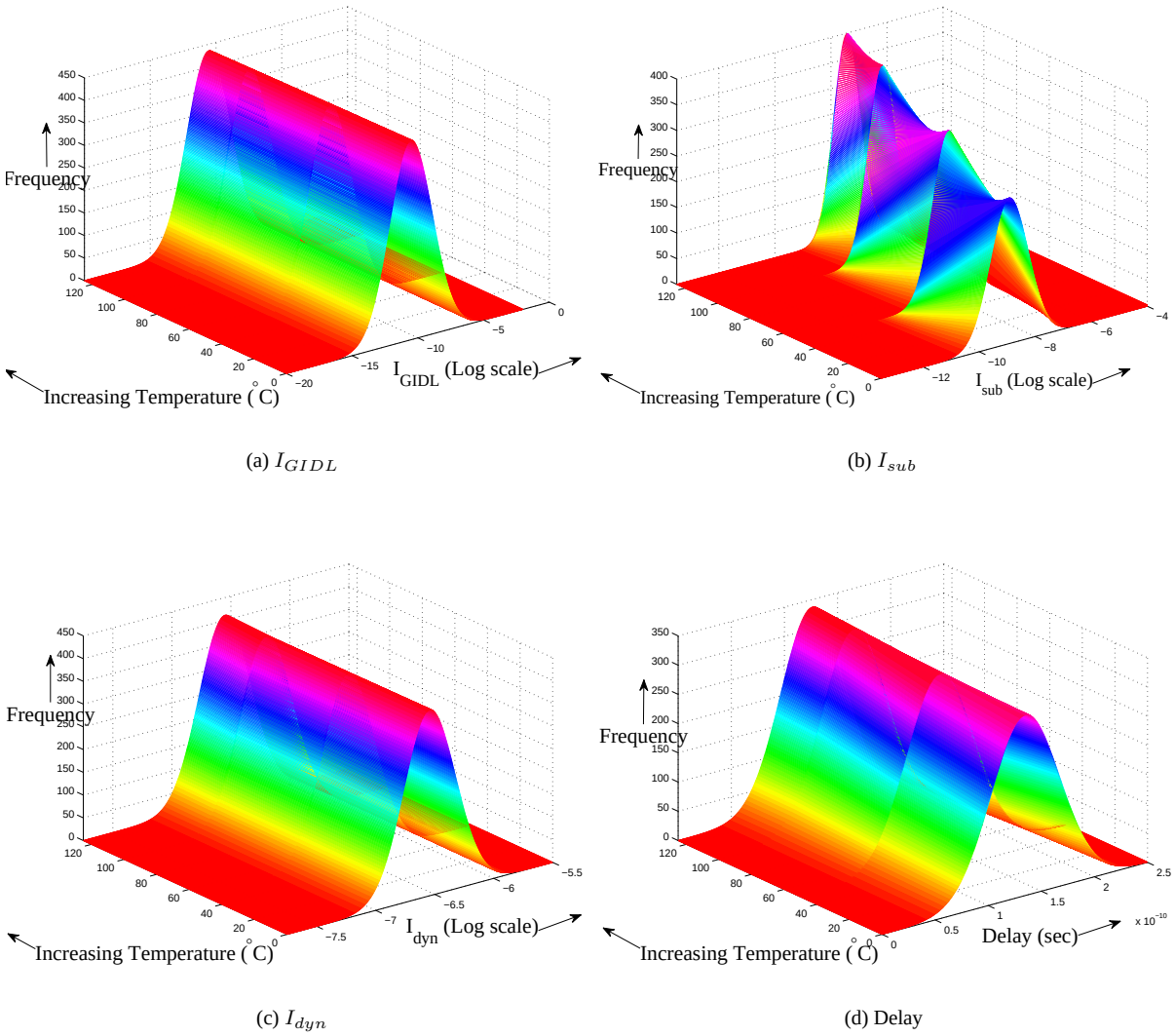

(a) I_{GIDL} (b) I_{sub}

(c) I_{dyn} (d) Delay

Figure 7. PVT plots for GIDL ($\hat{I}_{GIDL}$), subthreshold ($\hat{I}_{sub}$), and dynamic (I_{dyn}) current, and delay for a HKMG NAND.

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