Variability-Aware Optimization of Nano-CMOS Active Pixel Sensors using Design and Analysis of Monte Carlo Experiments

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Abstract

We propose a novel design flow for mismatch and process-variation aware optimization of nanoscale CMOS Active Pixel Sensor (APS) arrays. As a case study, an 8×8 APS array is designed using the proposed methodology for $32nm$ CMOS technology. Performance metrics such as power, output voltage swing, dynamic range (DR) and capture time (delay) have been measured. The baseline results show a power consumption of $16.32\mu W$, output voltage swing of $428mV$, dynamic range (DR) of $59.47dB$ and a capture time of $5.65\mu s$. The baseline APS array is subjected to 5% "intra-pixel" mismatch and 10% "inter-pixel" process variation and the effect on power and output voltage swing has been observed. The APS array is subjected to a design and analysis of Monte Carlo experiments based optimization. Using this approach, we have been able to achieve 21% reduction in power (including leakage). To the best of our knowledge, this is the first ever nano-CMOS implementation of an APS array optimized to be mismatch and process variation tolerant.

Keywords

Nanoscale CMOS, Design of experiments (DOE), Monte Carlo, Active Pixel Sensor (APS), Optimization, Gate Oxide Leakage, Subthreshold Leakage, Dynamic Power

1 Introduction

The advent of nano-CMOS technology has brought about significant challenges for analog and digital circuit design due to process variation and mismatch [1, 6]. Process variation describes the die-to-die, wafer-to-wafer, or lot-to-lot variability in which the same variation is assumed for the devices in a particular circuit. Mismatch describes die or wafer-level variability, in which devices in the same circuit may have different variations. For analog circuits, not only process variation but also mismatch influences the circuit behavior. According to the inverse square root law [3], mismatch becomes more severe when transistor gate size decreases. *To accurately predict analog circuit behavior, a combination of mismatch and process variation analysis is necessary*.

The emergence of complex System-on-Chip (SoC) technologies for consumer-electronics applications has been driven by the evolution of CMOS to nanoscale. These SoCs are mixed-signal designs, embedding analog blocks along with complex digital circuitry (i.e., multicores, logic blocks, memory, DSP). The growth of portable applications increases the need for low-cost, low-power, high-performance solutions. As an example, consider a typical digital camera SoC shown in figure 1 [11]. The design of the primary components, i.e. the APS array, has not taken advantage of nano-CMOS technology, and hence we address variability aware design of nano-CMOS APS in this paper to advance the state-of-the-art of analog/mixed signal SoC (AMS-SoC).

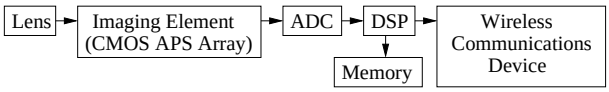


Figure 1. A typical CMOS sensor based digital camera in a mobile phone

The novel contributions of this paper are the following:

(1) A novel flow is proposed for variability tolerant design and optimization of nanoscale CMOS APS array.

(2) Two different mismatch and process variation concepts, "intra-array mismatch" and "inter-array variation" are introduced in the context of nano-CMOS APS circuits.

(3) A design and analysis of Monte Carlo experiments based algorithm is proposed for mismatch and process-variation aware design of an APS array. While a Monte Carlo approach gives a designer an idea about the circuit's yield, the DOE (Design of Experiments) approach allows dramatic reduction of the number of required simulations while providing a near-optimal design.

(4) As a case study a $32nm$ 8×8 CMOS APS array has been implemented, tested successfully, and thoroughly characterized. The APS array is subjected to simultaneous 5% "intra-array" mismatch and 10% "inter-array" process variation for robust design of the APS.

The rest of the paper is organized as follows: Section 2 discusses related research. The design and characterization of the baseline APS array is discussed in Section 3. The variability optimization methodology is presented in Section 4. The paper concludes in Section 5.

2 Related Previous Research in APS

In [10], the authors have examined mismatch in photodetectors at $2\mu m/1.2\mu m$ CMOS processes. In [7], the authors have analyzed pixel mismatch. In [5, 15], low voltage APS are proposed. In [12], the authors have analyzed the effect of technology scaling on readout time. A multiple-resolution APS is presented in [2]. It is evident that the existing research in APS does not consider all design challenges posed by nanoscale CMOS technology, such as leakage current, variability, and transistor reliability. *The APS proposed in this paper is variability tolerant, designed using the smallest CMOS technology, has the lowest power dissipation, and operates at the lowest voltage* (refer Table 1). Our APS incorporates the nano-CMOS challenges and is most suitable for target AMS-SoCs.

Table 1. Comparative perspective of selected existing APS arrays.

Works	Node	Supply	Power	Swing	Range
Weng [14]	$250\ nm$	$1.8\ V$	–	$0.5\ V$	–
Cho [4]	$350\ nm$	$1.5\ V$	$550\ \mu W$	–	–
Ours	$32\ nm$	$0.9\ V$	$16.32\ \mu W$	$0.428\ V$	$59.47\ V$

3 Proposed Flow for Variability-Aware Design and Optimization of Nano-CMOS APS

3.1 The Proposed Design Flow

We propose a novel design flow presented for variability-aware optimization of a nano-CMOS APS array in figure 2. The first step in the design flow is the design of a baseline array for a specific nano-CMOS technology node. Then the baseline $M \times N$ array is simulated for functional correctness. This step is followed by measuring the baseline values of the various figures of merit, such as power, leakage, voltage swing, capture time, etc. The target figures of merit which need to be optimized are identified. As nanoscale circuits suffer from high leakage, we have chosen to optimize average power (P_{APS}), with minimum degradation in output voltage swing (V_{swing}). These metrics are defined in Section 3.3. In the next step, the parameters to be used for process variation are identified. The array is then subjected to simultaneous "intra-array" mismatch and "inter-array" process variation. The "intra-array" mismatch can also be interpreted as pixel-to-pixel variation. This enables designers to take into account the trade-off between matched transistor size and yield when designing their circuits. Once the process variation results are analyzed, the design flow proceeds to the optimization. In the optimization, the parameters which are to be used as design variables are identified. The end product is an $M \times N$ APS array optimized for nanoscale process variations.

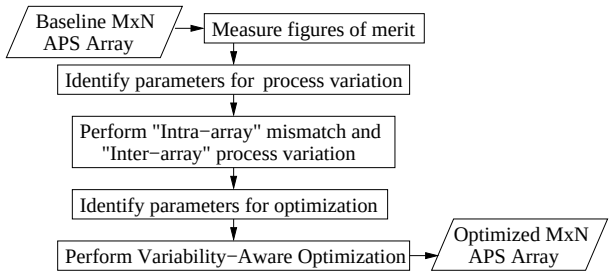


Figure 2. The proposed design flow for optimal design of nano-CMOS APS.

3.2 Single Pixel Design Using $32nm$ CMOS

An active-pixel sensor (APS) is an image sensor consisting of an integrated circuit containing an array of pixel sensors, each pixel containing a photodetector and an active amplifier. There are many types of active pixel sensors including the CMOS APS used most commonly in cell phone cameras, web cameras and in some DSLRs (digital single-lens reflex) cameras. Such an image sensor is produced by a CMOS process (and is hence also known as a CMOS sensor), and has emerged as an alternative to charge-coupled device (CCD) image sensors.

The design of a 3-transistor single pixel is presented as shown in figure 3. The three transistors of the circuit are as follows: (i) M1: reset transistor, (ii) M2: source follower transistor, and (iii) M3: access transistor.

A PMOS transistor ($M1$) has been employed as the reset transistor, as this results in a higher output voltage swing as compared to a conventional APS [5]. Transistor sizes are chosen carefully for enough current, source follower gain, and isolation of source follower output from the pixel output. In addition, the transistor sizes should be as small as possible for the maximum photodiode/pixel ratio ("fill factor"), when considering the physical design in silicon. Table 2 shows the sizes chosen for the transistors of the APS.

Table 2. Transistor sizes of the APS.

Transistor name	size ($W : L$) for $32nm$ CMOS
$M1$	$160nm : 32nm$
$M2$	$320nm : 32nm$
$M3$	$240nm : 32nm$

The most important component of the APS, the photodiode is modeled as a pulsed current source representing the photocurrent ($I_{photo} = 100nA$ to $350nA$) in parallel with a capacitor representing the diode capacitance ($C_{diode} = 20fF$) and a DC current source representing the dark current ($I_{dark} = 2fA$) [16]. $I_{bias} = 500nA$ and $C_{bias} = 1pF$ are assigned to

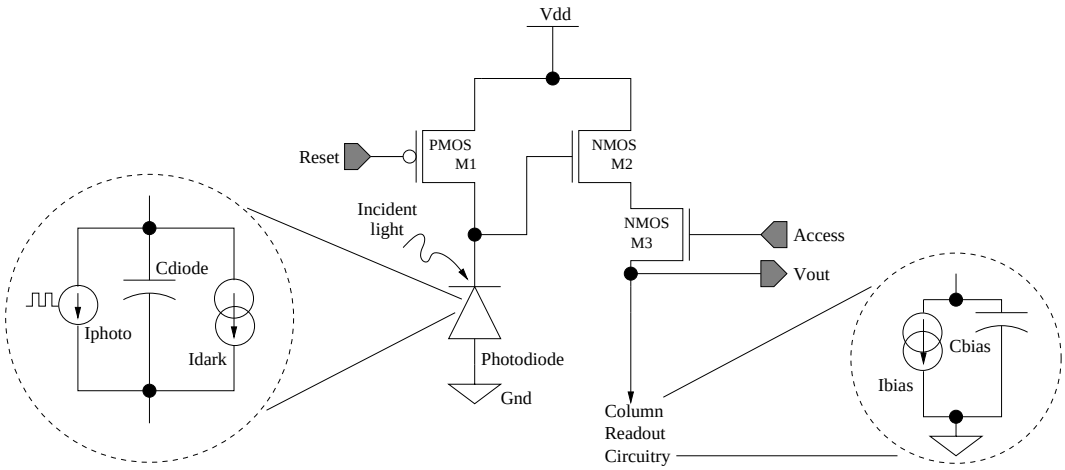


Figure 3. Circuit diagram of an active pixel sensor (APS).

the biasing circuitry. The values are selected to be consistent with the $32nm$ technology node. Higher bias current (I_{bias}) ensures a smaller readout time.

A typical two-dimensional array of $M \times N$ pixels is organized into M rows and N columns. Pixels in a given row share reset lines, so that a whole row is reset at a time. The row select lines of each pixel in a row are tied together as well. The outputs of each pixel in any given column are tied together. Since only one row is selected at a given time, no competition for the output line occurs. Further amplifier circuitry is typically on a column basis. Figure 4 shows the block diagram of an 8×8 APS array implemented using 64 single pixels of the type shown in figure 3. The array is accessed pixel-wise. The functional simulation results of the array are shown in figure 5 for high illumination photocurrent. We observe an output voltage swing of $428mV$. The result is obtained from transient analysis of the APS array.

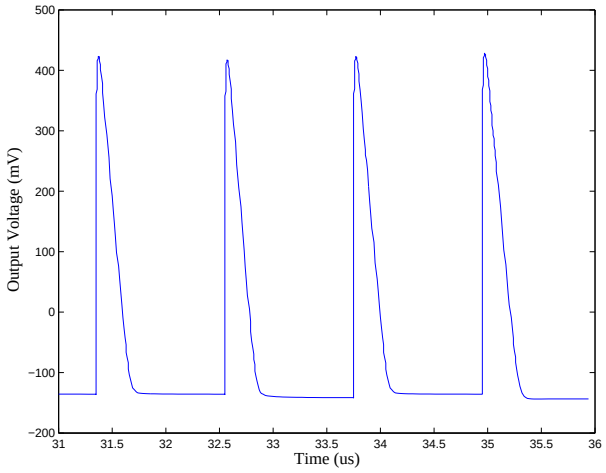


Figure 5. Circuit simulation of the 8×8 APS array.

3.3 Models For The Figures of Merit of The APS Array

We now discuss the baseline characterization of the APS array. The models used for characterizing the various figures of merit are presented. The array has been characterized for the following figures of merit or attributes: (i) Average power dissipation P_{APS}, (ii) Capture time C_{time}, (iii) Output voltage swing V_{swing}, and (iv) Dynamic Range DR.

3.3.1 Power Dissipation

At nano-CMOS technology, the total power of the APS array can be expressed as the sum of significant components as follows:

$$P_{APS} = P_{gate} + P_{sub} + P_{dyn}, \quad (1)$$

where P_{gate} is the gate-oxide leakage, P_{sub} is the subthreshold leakage, and P_{dyn} is the dynamic power consumed by all transistors in the array. Each of the current components can be analyzed from their governing expressions to identify the parameters affecting it.

Gate-oxide leakage current density of a device can be represented as follows [8, 13] :

$$J_{ox} = \alpha \left(\frac{V_{ox}}{T_{ox}}\right)^2 \times \exp\left(\frac{-\beta\left(1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)^{\frac{3}{2}}\right)}{\left(\frac{V_{ox}}{T_{ox}}\right)}\right), \quad (2)$$

where α and β are technology dependent factors. From equation 2, we can see that gate-oxide leakage is exponentially dependent on variations in T_{ox}. A higher T_{ox} leads to lower gate-oxide leakage current. The subthreshold leakage current in a transistor is represented as follows [9, 13]:

$$I_{sub} = \gamma \times \exp\left(\frac{V_{gs}-V_T}{S v_{therm}}\right) \times \left(1-\exp\left(\frac{-V_{ds}}{v_{therm}}\right)\right). \quad (3)$$

where $\gamma = \mu_0 \times \left(\frac{\epsilon_{ox} W}{T_{ox} L_{eff}}\right) v_{therm}^2 e^{1.8}$. The subthreshold leakage current is exponentially dependent on the threshold

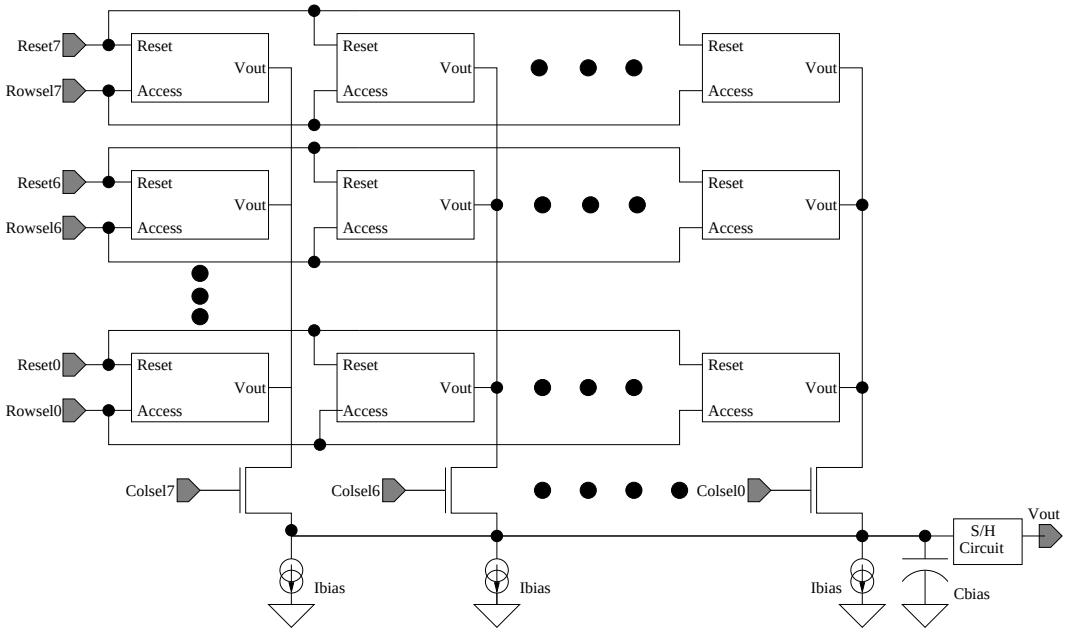


Figure 4. An 8×8 APS array constructed using a collection of APS.

voltage (V_T). From equation 3, we see that if T_{ox} is increased, the length (L_{eff}) is increased, and/or the width (W_{eff}) is reduced, there will be a reduction in the subthreshold leakage. The dynamic power can be represented as follows:

$$P_{dyn} = \eta \times C_L \times V_{dd}^2 \times f. \quad (4)$$

This form of power dissipation depends on loading conditions and not the device features. Also due to the quadratic relationship between P_{dyn} and V_{dd}, a lower supply leads to lower dynamic power dissipation. The total power, accounting for all the current components of APS array P_{APS} is the target attribute to be optimized. The APS array consumes a baseline total power of $16.32\mu W$ for $32nm$ CMOS technology node.

3.3.2 Output Voltage Swing

The output voltage swing (V_{swing}) of the array is defined as the maximum swing achieved by the output voltage. It is an important figure of merit because it affects the dynamic range (DR) of the array. From figure 5, we measure the baseline V_{swing} as $428mV$. This value is 47.6% of V_{dd}, which is in the acceptable range (2).

3.3.3 Dynamic Range

The dynamic range of the APS array can be formulated as follows [16]:

$$DR = 20 \times \log_{10} \left(\frac{\left(\frac{q \times Q_{max}}{t_{int}}\right) - I_{dark}}{\left(\frac{q}{t_{int}}\right)\sqrt{\sigma_{total}^2 + \left(\frac{I_{dark} \times t_{int}}{q}\right)}} \right), \quad (5)$$

where,

$$Q_{max} = \left(\frac{C_{diode} \times V_{swing}}{q} \right), \quad (6)$$

where σ_{total}^2 = variance of noise due to readout and reset (in $electron^2$), t_{int} = integration period. The baseline DR of the APS for $32nm$ CMOS technology is calculated to be $59.47dB$.

3.3.4 Capture Time

As discussed in section 3.2, the input to each pixel in the array has been modeled in the form of a pulse shaped photocurrent I_{photo}. The capture time is defined as the delay from the 50% level of the input swing (I_{photo}) to 50% level of the output voltage (V_{out}). For measurement of capture time (C_{time}) of the array, we have considered the pixel in the middle of the array, as it suffers the maximum loading. Thus it gives us the maximum C_{time} of the array. The APS array has a baseline C_{time} of $5.65\mu s$ for $32nm$ CMOS.

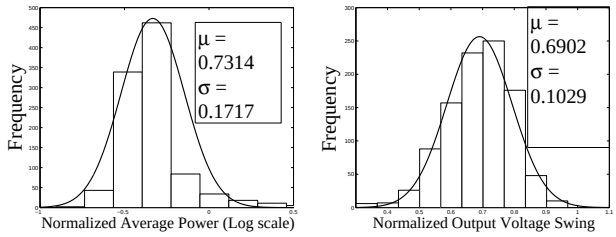
The baseline characterization results for the APS array are shown in Table 3.

Table 3. Baseline characterization results.

Parameter	Value
Technology	$32nm$ PTM
V_{dd}	$0.9V$
P_{APS}	$16.32\mu W$
C_{time}	$5.65\mu s$
V_{swing}	$428mV$
DR	$59.47dB$

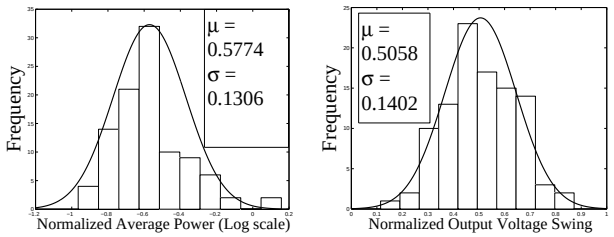
4 The Proposed Variability-Aware Optimization

We now present the proposed algorithm used for APS array optimization for nano-CMOS technology. The APS array has been subjected to simultaneous "intra-array" mismatch and



(a) Average power (b) Output swing

Figure 6. Distribution of (a) Average power P_{APS} and (b) Output voltage swing V_{swing} for the case: $V_{dd} = V_{dd-H}$ and $T_{ox} = T_{ox-L}$. This is also the baseline case.



(a) Average power (b) Output swing

Figure 7. Distribution of (a) Average power P_{APS} and (b) Output voltage swing V_{swing} for the case: $V_{dd} = V_{dd-L}$ and $T_{ox} = T_{ox-L}$.

"inter-array" process variation and the effects on the figures of merit are studied. The process parameters identified for mismatch and process variation are: (i) supply voltage V_{dd}, (ii) NMOS threshold voltage V_{Tnmos}, (iii) PMOS threshold voltage V_{Tpmos}, (iv) NMOS gate-oxide thickness T_{oxnmos}, and (v) PMOS gate-oxide thickness T_{oxpmos}.

The figures of merit under consideration are P_{APS} and V_{swing}. Hence they form the objective set F for optimization. The process parameters are subjected to "intra-array" mismatch and "inter-array" process variation simultaneously for $R = 1000$ runs. For the "intra-array" mismatch, the parameters are assumed to have a Gaussian distribution and are assigned mean (μ) values as the baseline values specified in the design, and a standard deviation (σ) of 5%. For the "inter-array" process variation also, the parameters are assumed to have a Gaussian distribution and are assigned mean (μ) values as the baseline values specified in the design, and a standard deviation (σ) of 10%. P_{APS} shows a lognormal distribution in figure 6(a). Due to the significant impact of various leakage mechanisms (P_{sub}, P_{gate}) having an exponential relationship with the process parameters, this observation is intuitive from the governing expressions. V_{swing} shows a Gaussian (normal) distribution (figure 6(b)). This is considered as the baseline case.

To demonstrate the array optimization, P_{APS} minimization and V_{swing} maximization has been kept as the objective. Power is always a constraint for nanoscale SoCs. Hence P_{APS} is chosen. Also, V_{swing} directly affects the dynamic range of the APS, thus giving an important measure of performance. However, the proposed methodology can be extended to other figures of merit as well. This is a multi-objective optimization. However, it is unlikely that both these objectives would be optimized by the same alternative parameter choices. For design and analysis of Monte Carlo experiments, the parameters to be used are: (i) supply voltage V_{dd}, (ii) NMOS gate-oxide thickness T_{oxnmos}, and (iii) PMOS gate-oxide thickness T_{oxpmos}. From equations (4), (2), (3), it can be seen that these parameters affect the power consumption significantly. Hence, they form the design variable set D for the optimization algorithm. We have not considered V_{Tnmos} and V_{Tpmos} as optimization parameters, as they are dependent on a variety of parameters such as doping concentration of source or drain diffusions, channel length.

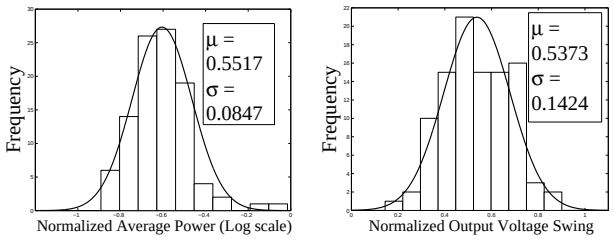
We now present the algorithm for two values of design variables with H denoting high and L denoting low values. Thus, V_{dd-H}, V_{dd-L}, T_{ox-H}, and T_{ox-L} are the possible values of the design variables. V_{dd-H} and T_{ox-L} are baseline values as per $32nm$ CMOS technology node. V_{dd} scaling refers to reduction in V_{dd} (i.e. from V_{dd-H} to V_{dd-L}), while T_{ox} scaling refers to increase in T_{ox} (i.e. from T_{ox-L} to T_{ox-H}). As in a traditional CMOS process, the gate oxides of NMOS and PMOS transistors are grown together, T_{oxnmos}, T_{oxpmos} are scaled together i.e. they are assigned either a higher (T_{ox-H}) or lower (T_{ox-L}) value together.

For the above scenario, we have 4 different combinations. However, the situation is much involved for other discrete sets of design variables. These values are assigned to the μ of optimization parameters for $R = 100$ Monte Carlo runs. The array is subjected to 5% "intra-array" mismatch and 10% "inter-array" process variation for each of the 4 combinations. The Monte Carlo data for F are obtained, and normalized. Normalization involves division of each value of the data by the maximum value of data. The μ and σ values for P_{APS} and V_{swing} are recorded in Table 4 for $V_{dd-H} = 0.9V$, $V_{dd-L} = 0.7V$, $T_{ox-H} = 2.0nm$, and $T_{ox-L} = 1.65nm$. P_{APS} is observed to have a lognormal distribution (figure 6(a), 7(a), 8(a), and 9(a)) and V_{swing} is observed to have a Gaussian distribution (figure 6(b), 7(b), 8(b), and 9(b)) using a least squares fit.

Table 4. Monte Carlo simulation results.

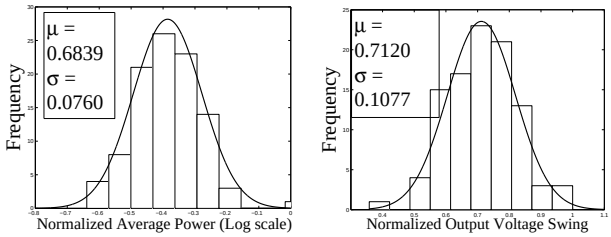
V_{dd} (V)	T_{ox} (nm)	$\mu_{P_{APS}}$ (μW)	$\sigma_{P_{APS}}$ (μW)	$\mu_{V_{swing}}$ (mV)	$\sigma_{V_{swing}}$ (mV)
V_{dd-L}	T_{ox-L}	0.5774	0.1306	0.5058	0.1402
V_{dd-L}	T_{ox-H}	0.5517	0.0847	0.5373	0.1424
V_{dd-H}	T_{ox-L}	0.7314	0.1717	0.6902	0.1029
V_{dd-H}	T_{ox-H}	0.6839	0.0760	0.7120	0.1077

The following prediction equations are obtained using the



(a) Average power (b) Output swing

Figure 8. Distribution of (a) Average power P_{APS} and (b) Output voltage swing V_{swing} for the case: $V_{dd} = V_{dd-L}$ and $T_{ox} = T_{ox-H}$.



(a) Average power (b) Output swing

Figure 9. Distribution of (a) Average power P_{APS} and (b) Output voltage swing V_{swing} for the case: $V_{dd} = V_{dd-H}$ and $T_{ox} = T_{ox-H}$.

design of experiments method on monte carlo experiments:

$$\hat{\mu}_{P_{APS}} = 0.6361 + 0.0716 \times V_{dd} - 0.0183 \times T_{ox}, \quad (7)$$

$$\hat{\sigma}_{P_{APS}} = 0.1157 + 0.0081 \times V_{dd} - 0.0354 \times T_{ox}, \quad (8)$$

$$\hat{\mu}_{V_{swing}} = 0.6113 + 0.0898 \times V_{dd} + 0.0133 \times T_{ox}, \quad (9)$$

$$\hat{\sigma}_{V_{swing}} = 0.1233 - 0.0180 \times V_{dd} + 0.0018 \times T_{ox}. \quad (10)$$

The prediction equations are of the form:

$$\hat{Y} = \bar{Y} + \left(\frac{\Delta V_{dd}}{2}\right) \times V_{dd} + \left(\frac{\Delta T_{ox}}{2}\right) \times T_{ox}, \quad (11)$$

where $\hat{Y}$ is the response, $\bar{Y}$ is the average, $\frac{\Delta V_{dd}}{2}$ and $\frac{\Delta T_{ox}}{2}$ are the half-effects of the design variables. A linear relationship between the design variables and response is assumed, with a maximum discrepancy of 1% between the observed results and results calculated using the predictive equations. If a non-linear relationship is assumed, the complexity would increase accordingly. From equations 7, 8 and 10, we observe that $\hat{\mu}_{P_{APS}}$, $\hat{\sigma}_{P_{APS}}$ and $\hat{\sigma}_{V_{swing}}$ are to be minimized for power minimization, while $\hat{\mu}_{V_{swing}}$ needs to be maximized for V_{swing} maximization (equation 9). It can be seen that $\hat{\mu}_{P_{APS}}$ and $\hat{\sigma}_{P_{APS}}$ are perfectly correlated, i.e. optimizing the mean

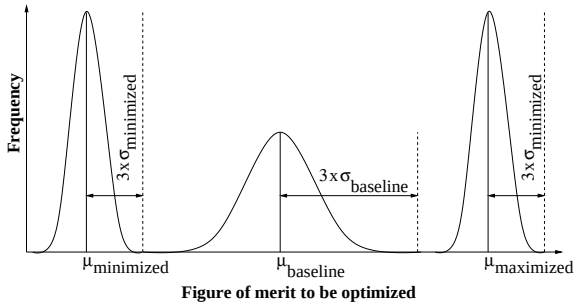


Figure 10. Objectives of the variability-aware optimization.

would also optimize the standard deviation. However, $\hat{\mu}_{V_{swing}}$ and $\hat{\sigma}_{V_{swing}}$ are not correlated. Hence a combined effect of the mean and standard deviation must be considered, for possible generalization of the proposed methodology. Also, this information is available only after the prediction equations have been obtained. The purpose of the paper is process optimization so parametric yield is not considered. We form two objective functions $f_{P_{APS}}$ and $f_{V_{swing}}$ as follows:

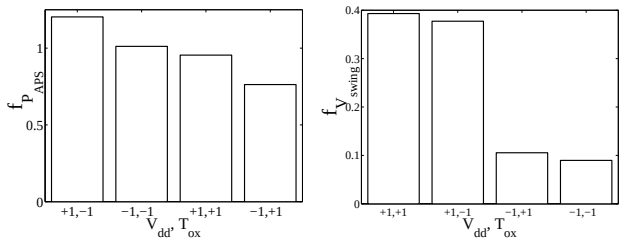
$$\begin{aligned} f_{P_{APS}} &= \hat{\mu}_{P_{APS}} + 3 \times \hat{\sigma}_{P_{APS}}, \\ &= 0.9832 + 0.0959 \times V_{dd} - 0.1245 \times T_{ox}. \end{aligned} \quad (12)$$

$$\begin{aligned} f_{V_{swing}} &= \hat{\mu}_{V_{swing}} - 3 \times \hat{\sigma}_{V_{swing}}, \\ &= 0.2414 + 0.1438 \times V_{dd} + 0.0079 \times T_{ox}. \end{aligned} \quad (13)$$

Figure 10 shows the theory behind the formation of the objective functions. The idea is that $\mu_{baseline}$ of the figure of merit to be optimized needs to be shifted left or right depending on whether it needs to be minimized ($\mu_{minimized}$) or maximized ($\mu_{maximized}$). Also, the $3 \times \sigma_{baseline}$ of the figure of merit (which is a measure of the spread) needs to be minimized to $3 \times \sigma_{minimized}$. A $3 \times \sigma$ limit has been considered, so that 99.5% of all the figure of merit values will fall within the $3 \times \sigma$ limit. From equations 12 and 13, we see that $f_{P_{APS}}$ needs to be minimized and $f_{V_{swing}}$ is to be maximized. The Pareto chart for $f_{P_{APS}}$ in figure 11(a) shows that the design variable set D = [V_{dd-L}, T_{ox-H}] leads to the minimum value of $f_{P_{APS}}$. The value of $f_{V_{swing}}$ corresponding to this set (figure 11(b)) is also acceptable. This is confirmed by using this value of D to simulate the array which yields an acceptable V_{swing} (46.4% of V_{dd}). Power minimization is treated as primary objective. We achieve a 21% reduction in P_{APS} with a 24% penalty in V_{swing}. The baseline and optimal values of P_{APS} and V_{swing} are shown in Table 5. The algorithm is shown in figure 12.

5 Conclusion and Future Research

We have presented a novel design flow and optimization algorithm suitable for variation-tolerant (robust) design of nano-CMOS APS. A $32nm$ 8×8 APS array has been subjected to



(a) $f_{P_{APS}}$ (b) $f_{V_{swing}}$

Figure 11. Pareto plots for (a) $f_{P_{APS}}$ and (b) $f_{V_{swing}}$.

Table 5. Baseline and optimal values of figures of merit

Value	P_{APS} (μW)	V_{swing} (mV)
baseline	16.32	428
Optimal	12.91	325

this design flow in the presence of simultaneous "intra-array" mismatch and "inter-array" process variation. This gives APS designers an insight into their circuits yield caused by transistor mismatch and process variation before going into fabrication. Design and analysis of Monte Carlo experiments on the baseline array has been carried out leading to 21% power reduction at the cost of 24% output voltage swing reduction. In the future, we plan to investigate variability-area design of APS for post-nano-CMOS, such as high-κ/ metal gate, Carbon Nanotube, and Dual-Gate FETs.

6 Acknowledgments

This research is supported in part by NSF award number 0702361.

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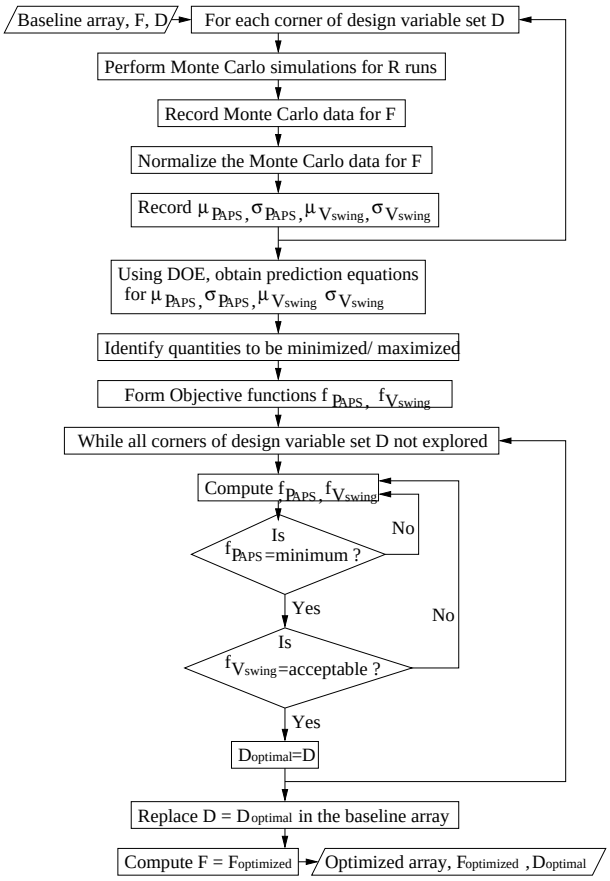

Figure 12. Flowchart of the proposed algorithm.

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