A Combined Packet Classifier and Scheduler Towards Net-Centric Multimedia Processor Design

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***Abstract*— We introduce a Net-centric Multimedia Processor (NMP) with built-in Digital Rights Management (DRM) facilities to facilitate internet protocol packet processing and video processing without use of the main CPU. Packet classification and scheduling are the two most computational intensive operations. In this paper we propose an algorithm and architecture which can perform simultaneous classification and scheduling towards high-performance and power-efficient realization of the NMP. The architecture is prototyped in VHDL and simulated for power, frequency, logic usage and throughput for 4 different logic families in the Xilinx environment.**

I. Introduction and Motivation

The future broadband Internet scenario is a TV with a set-top box: TV signal, voice, and broadband data in a common IP network using a digital subscriber line access multiplexer (DSLAM). More and more entertaining and educating applications, such as commercial TV, video on demand, time-shifted TV, video phones, game portals, personal digital library, etc. will be supported by Internet Protocol Television (IP-TV) [1].

Many unsolved problems, such as scalability, high-quality experience, support of broad service portfolio, cost-effective service deployment, DRM (for security and copyright protection, etc.) still exist for IP-TV. Industrial and academic efforts are in full swing to resolve these issues. However, DRM of the video content in IP-TV still remains one of the most important unsolved problems. Thus, we introduce a Net-centric Multimedia Processor (NMP) with built-in DRM facilities which can be integrated in any of the multimedia creating equipment. The NMP has multimedia processing capabilities along with networking capabilities. The NMP can completely offload computationally intensive multimedia processing and network packet processing from the main CPU of a computer thus making the CPU available for other applications. The NMP can be a part of line cards of common routers, network cards, set-top boxes, or other high-speed communications devices in the IP network cloud.

II. The Proposed Net-centric Multimedia Processor (NMP)

The architecture proposed for the NMP to be designed using system-on-a chip (SoC) technology is shown in Fig. 1 [2]. The system architecture of the NMP consists of several processing elements (PEs), each with dedicated operational capabilities and all of them connected through an internal bus. The internal bus forms the physical communication channel among the PEs as well as other components of the NMP. Packet classification is an intensive task in an NMP and is carried out by the packet classifier. It reads the header of an incoming packet, determines the stream to which the packet belongs, decides the outgoing interface using routing lookup, and passes the packet to the appropriate PE for further processing. The outgoing packet is dynamically buffered by the packet scheduler until it is sent to the outgoing link. The instruction and control memory is used to store the instructions corresponding to the program that will be executed using the NMP. The data memory is used to store or buffer the (video/IP) data, and an appropriate mechanism is needed to avoid data conflict among the PEs. Input interface and output interface are two ports through which the proposed NMP will communicate with the external environment.

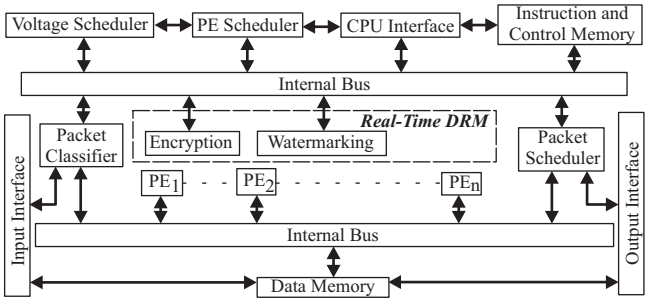


Fig. 1. High-Level Representation of the Proposed Architecture of the NMP.

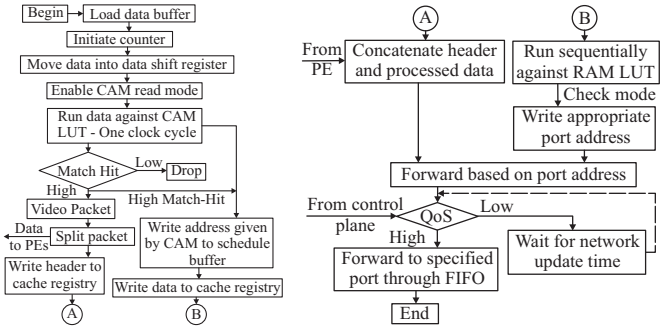
Classification and scheduling along with DRM are key functionalities of the NMP, however we deal with classification and scheduling in this paper. The existing packet classification or scheduler solutions are not targeted towards video broadcasting and are power hungry, and thus cannot be used for portable applications [3], [4], [5]. Hence, we propose algorithms and architectures discussed in the next section which can perform simultaneous classification and scheduling and can be realized using minimal logic and dissipating minimal power.

III. The Proposed Classification-Scheduling Algorithm and Architecture

The challenge is to develop the classification and scheduling for high-performance processing while reducing the operation latency, logic usage, and power dissipation. The NMP must be equipped with units so that as IP packets arrive, they can

be processed directly without using the central processing unit. We propose to design the classifier-scheduler module which will classify and schedule data for the NMP. The proposed module will differentiate between IP packets and video packets. The video packets are further processed for digital rights management (DRM) using corresponding PEs. IP packets which carry regular traffic will traverse as usual for further processing in other PEs.

We present an algorithm in Fig. 2 and the corresponding high-level representation of the architecture in Fig. 3 for simultaneous classification and scheduling. The algorithm classifies and sends data to PEs and joins back the data with the header after the processing is performed. The scheduler collects them and using the updates from the controller schedules the packets based on Quality-of-Service (QoS) parameters. The classifier-scheduler is tied to the controller through data buses and to the memory with address buses. As soon as the string of data (the IP packet) flows in, the classifier checks the header against Content Addressable Memory (CAM) Look Up Tables (LUTs), strips the header and stores it in cache. The remaining of the packet is forwarded to PEs, and after the PEs send the data back, the registry is updated and it is joined with the header. The schedulers registry is constantly updated by the QoS updater and once a new packet comes in, it takes the update and schedules it or pushes the packet back in the queue.



(a) Beginning phases, continued in (b) (b) Last phases, continued from (a)

Fig. 2. Flow chart of combined classification and scheduling algorithm.

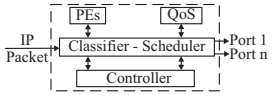


Fig. 3. High-Level Architecture of the Combined Classifier-Scheduler.

IV. Prototyping and Experimental Results

For the propose of experimentation a prototype is modeled using VHDL and simulated through Xilinx. CAM architecture is used as the basis for the classifier-scheduler. For the propose of simulation, we have added a bit flag in the options field in the physical packet address, so that the classifier-scheduler can easily identify a video packet from a non-video packet. If the flag is high, the packet is considered a video packet else considered as an IP packet.

Complete synthesis of the VHDL description of the module is performed along with its mapping, placement and routing. The models are simulated for 4 different logic families. It is a designer's choice to select a particular logic family depending on a target application. The power dissipations has been estimated under the ambient temperature of 25^oC and supply voltage of $2.5V$. The experimental results are graphically presented in Fig. 4. The throughput was highest for Automotive-Spartan3, but the risk is high power dissipation. On the other hand, Virtex-XV and Spartan-2E were observed to be more appropriate for power and throughput point of view.

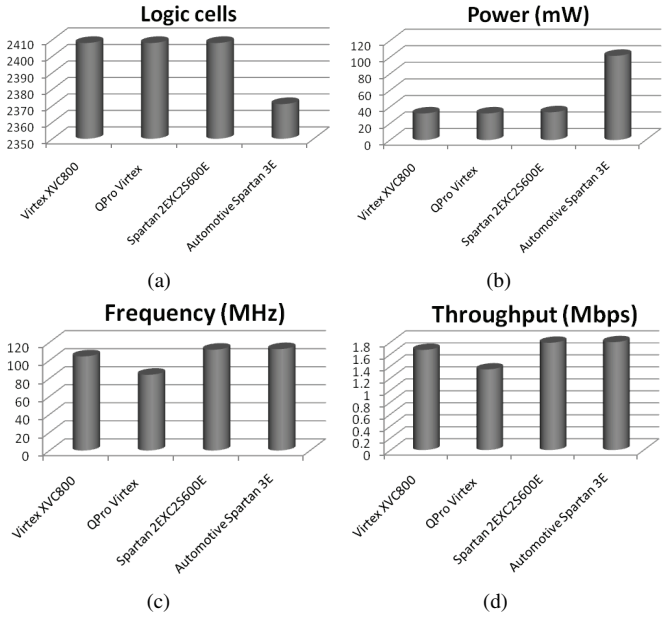


Fig. 4. Classifier-Scheduler Prototyping for Various Technology.

V. Conclusions and Future Works

We have achieved the classifier-scheduler in structural and behavioral design. The classifier-scheduler can be used for NMP as well as network processors with appropriate modifications. We have introduced the architecture of NMP, and analyzed the complexities of developing NMP as a SoC design. We have also built other modules, such as watermarking and encryption. Many other modules are in the process of building. Further, we will use low-power techniques like power gating and voltage scaling to handle power issues.

VI. Acknowledgment

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