Single Ended 6T SRAM with Isolated Read-Port for Low-Power Embedded Systems

Jawar Singh, Dhiraj K. Pradhan, Simon Hollis, Saraju P. Mohanty* and J. Mathew
Department of Computer Science, University of Bristol, UK.
Department of Computer Science and Engineering, University of North Texas, USA.*
Email-ID: jawar@cs.bris.ac.uk, saraju.mohanty@unt.edu

***Abstract*— This paper presents a six-transistor (6T) single-ended static random access memory (SE-SRAM) bitcell with an isolated read-port, suitable for low-V_{DD} and low-power embedded applications. The proposed bitcell has a better static noise margin (SNM) and write-ability compared to a standard 6T bitcell and equivalent to an 8T bitcell [1]. An 8Kbit SRAM module with the proposed and standard 6T bitcells is simulated, including full blown parasitics using BPTM, 65nm CMOS technology node to evaluate and compare different performance parameters. The active power dissipation in the proposed 6T design is 28% and 25% less, compared to standard 6T and 8T SRAM modules respectively.**

I. Introduction

Embedded systems particularly targeted towards low duty-cycles and portable applications, such as mobile phones or PDAs, must have low energy consumption, as these systems are battery powered. In such systems, a considerable amount of power is consumed during memory accesses, which has significant impacts on battery life. Hence, efficient active and leakage power saving SRAM designs need to be explored for longer operation of battery powered applications. There are two primary areas having a strong potential for active and leakage power saving [2]. First, lowering the operating voltage and second reduction in dis/charging capacitance of word and bit lines. It has reported that up to 70% of the total active power is dissipated in bit lines dis/charging during read and write operations [3]. Hence, reduction in charging capacitance has strong prospect of power saving.

Reduction in supply voltage poses several design challenges for low power high density SRAMs. These challenges arise due to a reduced static noise margin (SNM) and increased variability in nanoscale CMOS (nano-CMOS) technologies. In modern system on chips (SoCs), where total power and total area is dominated by the SRAM, reduction in V_{DD} for SRAMs can save both active energy and leakage power [4]. Also, for system integration, SRAM must be compatible with subthreshold combinational logic operating at ultra-low voltages [5]. However, this leads to increase in sensitivity of design and process parameter variability. This problem will worsen in nanometer technologies with reduction in operating voltage and makes SRAM design more challenging. These practical challenges limit standard 6T SRAM bitcells and architectures to a higher V_{DD}.

The current literature is rich in different types of SRAM bitcell designs consisting of 7 to 10 transistors targeted to improve the read stability and write-ability [6], [7]. Read stability has been improved in designs [8]–[10] by isolating the bitcell nodes from bitlines. Write-ability in the prior designs [1], [5], [6], [8] enhanced by either weakening of cross-coupled inverters or routing an extra supply voltage. All these features in the prior designs lead to increases in area overhead or energy consumption.

In this paper, a 6T SE-SRAM bitcell and its word-orientation array design for robust, high density and low-power embedded systems is presented. The proposed design has been exhaustively evaluated and results were compared with standard 6T bitcell and 8T bitcell [1]. In the proposed 6T bitcell, isolation of read current path improves the read SNM, while strong write-ability of logic '1' is achieved by write assist transistor.

The rest of this paper is organized as follows: Section II introduces the proposed bitcell and word-oriented SRAM design. The operation and stability margins are presented in Section III. The issues and remedy of bitline leakage are presented in Section IV. Section V discusses the physical design, active power and read access time; the conclusions were given in Section VI.

II. Proposed 6T bitcell and word-oriented SRAM array design

The proposed 6T SRAM bitcell shown in Fig. 1, consists of a cross coupled inverter pair (INV1 and INV2) connected to a bitline (BL) using access transistor (M5) and an isolated read-port transistor (M6). The dotted transistors (M_{WA} and M_{RA}) represent write and read assist transistors respectively, for a memory word which can be of 8, 16, or 32 bit.

In word-oriented SRAM array design with the proposed bitcell, a word has non-interleaved more than 1-bit per word. If n be the number of bitcells in a word-oriented memory which should contains more than 1-bit per word, that is, $n \geq 2$. For instance, a word with the proposed 6T bitcell has $n = 32$ bitcells, as shown in Fig. 2. Since read and write operations access the n bits of a word simultaneously, one could share the read/write assist transistors of a bitcell, as shown dotted in Fig. 2. Therefore, we only need one read/write assist transistor per word. Consequently, each bitcell in a word has six transistors with two additional dotted transistors per word (Fig. 2). Also reading/writing of a word (cells) is not affected, when other word is accessed for writing/reading,

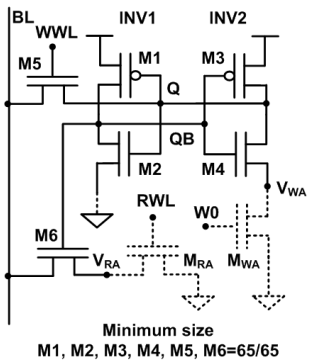

Fig. 1. The proposed single-ended 6T SRAM bitcell with dotted read and write assist transistors

because a word shares read/write assist transistors by row, not by column.

Proper sizing of read/write assist transistor is crucial because functioning and performance as a whole of a memory block depends upon these transistors. If we overestimate their size, then there is a wastage of valuable silicon area, increase in leakage, and switching power dissipation. Similarly, if we underestimate the size, then the read and write operations would be too slow or significant delay due to the increased resistance to ground. The use of both transistors is fundamentally different because one (read assist) transistor has to provide low resistive path to read current during read operation. The other (write assist) transistor has to provide high resistance path for successful write operation to weaken the cross coupled inverters. As both read and write requirements are conflicting in nature, there is a need to analyze the sizing issues separately for read and write assist transistors.

A. Read Assist Transistor

The shared read assist transistor in the proposed word-oriented SRAM design needs judicious sizing for the proper functioning and desired performance. Since, all the individual read assist transistors (refer Fig. 1) of a bitcell are replaced by a single shared read assist (M_{RA}) transistor in a word-oriented SRAM design (refer Fig. 2). The read assist transistor forms the critical path, essentially when reading '0' because it has to discharge the precharged bitline (BL) to the sensing level ($0.5V_{DD}$). Also, in the worst case, when all bitcells in a word holds '0', a shared read assist transistor has to discharge all the precharged BLs to the sensing level. Hence, the performance of the proposed SRAM is determined by the '0' read access time, which is mainly depend upon the size of M_{RA}. Consequently, the size of M_{RA} in word-oriented SRAM design, when a word has common read assist transistor (M_{RA}) is critical for estimating the read access time or in other words operating frequency. At the same time it should not be over sized so that the subthreshold leakage current may pull down the precharged BL to low and cause an erroneous read. The erroneous read problem due to BL leakage has been studied in the subsequent section IV. Fig. 3 shows the SPICE transient simulations for 32 and 64-bit words to estimate the size of the shared read assist transistor for a target '0' read access time. For instance, the target '0' read access time is set to 1ns, which can be achieved by keeping the W/L ratio 4 times for a 32-bit word-oriented SRAM array.

B. Write Assist Transistor

In the proposed word-oriented SRAM array, all individual bitcell's M_{WA} transistors are replaced by a single equivalent transistor (M_{WA}). Thus, M_{WA} should be sized properly, so that all the bitcells in that word must be written correctly. In the worst case scenario, that can be either writing '1' or '0' in all the bitcells. The M_{WA} has to weaken the cross coupled inverters by floating the INV2 of all the bitcells in that word. Weakens the loop regardless of whether we intended to write '1' or '0' in all or fewer bitcells in that word. The weakening of the loop of a single bitcell or all the bitcells in a word is equivalent, because drain to source voltage (V_{DS}) of M_{WA} is always higher than '0', when gate to source voltage (V_{GS}) of M_{WA} is zero. Thus, a minimum sized transistor would be well suited for this purpose. Also, after the write access time M_{WA} has to provide a ground to node V_{RA} of all the bitcells. For providing a ground to node V_{RA}, M_{WA} has to pass only the leakage current of all the bitcells either they are having '0' or '1' at node Q. Since, the transistor M_3 (when node Q at '0') and transistor M_4 (when node Q at '1') are in cut-off mode, therefore, there is only leakage current to flow through M_{WA}[see Fig. 1]. As only M_{WA} has to provide leakage current path to all the bitcells of a word which is always less than the dynamic current. Also, for minimum leakage and data retention it is recommended to use a minimum sized transistor. The SPICE simulation for different word size of SRAM array reveals that there is no significant improvement in the write-ability of the SRAM with increasing/decreasing the size of M_{WA}.

III. Operation and stability margins

Read and write operations and their margins such as static noise margin (SNM) and write-ability margin to determine the efficacy of a SRAM bitcell are presented in this Section. In order to demonstrate the soundness of the proposed design, bitcell margins were simulated and compared with the standard 6T and 8T bitcells. The BPTM of 65 nm CMOS technology node [11] assuming to apply to a $16 \times 16 \times 32$ bit module. Each bitcell margins shown in the subsequent sections were simulated corresponds to 8-Kbit memory capacitance and 4-σ process variations in the threshold voltage V_t.

A. Read Operation

Information read out from the proposed SRAM bitcell is carried out via a single ended bitline (data-line). Prior to the read operation, BL is precharged to V_{dd} and the read word line (RWL) is asserted high (W0 is high) to turn on the M_{RA}, which is essentially applicable for reading '0'. For reading '1', BL has to remains at precharged level ($\sim V_{dd}$) because transistor M6 is turned off. It is important to notice that only the read '0', high to low transition is affected by the insertion

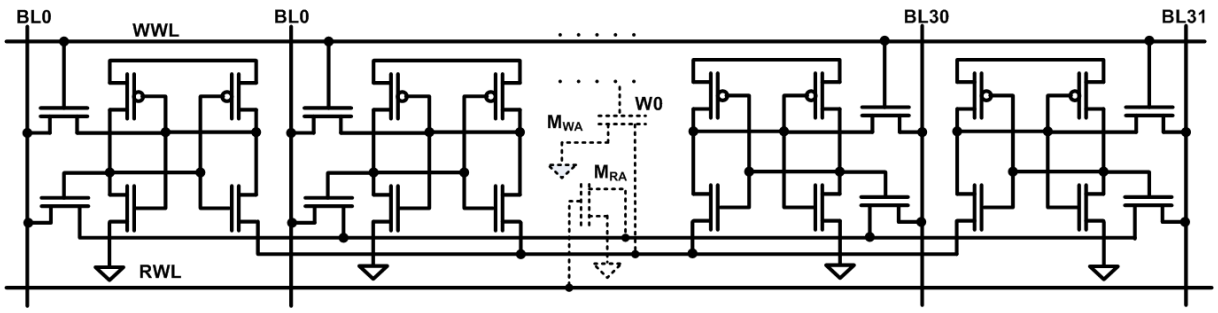

Fig. 2. A 32-bit word organization of the proposed 6T SE-SRAM cell with dotted read and write assist transistors.

of the M_{RA} and that the read '1', low to high transition will not be affected. As a result, reading '1' is directly sensed from the precharged BL. In both the cases either reading '1' or '0', storage nodes are isolated from the read current path. It results in reduced capacitive coupling noise due to BL and hence, significantly enhances the data stability during read and hold states.

B. Write Operation

It is a fact that the write operation in single ended SRAM bitcells is difficult because of strongly cross coupled inverters. To overcome this problem, a write assist transistor M_{WA} is used, which is controlled by W0. The usage of M_{WA} is to weaken the cross coupling of proposed 6T bitcell inverters during write access time. Initially, we assume that the node Q$=0$ and QB$=1$, write word line (WWL) is asserted high to turn on the write access transistor M5 that connects the precharged bitline (BL) to node Q. As both the inverters (INV1 and INV2) are strongly cross coupled, so forcing the node Q to '1' is difficult through a pass gate device (M5). Hence, we weaken the pull down strength of INV2 by inserting a series transistor M_{WA}, which is controlled by W0 to cut-off during write operation. In other words, M_{WA} is used to weaken the strongly cross coupled inverters. Hence, it enhances the write-ability, even at lower operating voltages.

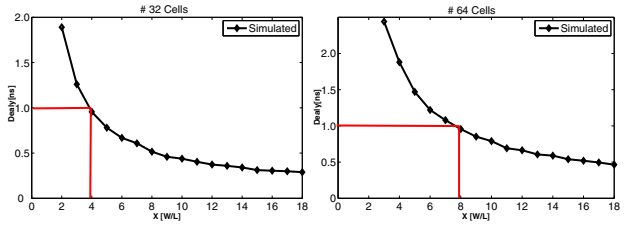

Fig. 3. Estimation of target read access time for different word sizes that enables the size of read assist transistor (W/L).

C. Read Static Noise Margin

Read SNM of the proposed 6T, standard 6T and 8T bitcells are shown in Fig. 4 to present a comparative perspective. The proposed 6T bitcell has $0.302V$ SNM, while the standard 6T bitcell SNM is $0.152V$ at a supply voltage of $1.0V$ and $\beta = 2$ (refer Fig. 4(a)). SNM of the proposed 6T bitcell at a supply voltage of $0.3V$ is equal to that of the standard 6T bitcell at $0.5V$ and $\beta = 4$ (refer Fig. 4(b)). However, the normalized SNM to supply voltage for different bitcell ratio (β= 2, 3 and 4) in Fig. 4(b) shows that the variation of SNM in the proposed 6T bitcell (for minimum feature size) is smaller than that of the standard 6T bitcell, mainly because of reduced capacitive coupling and isolation of read current path from storage node Q and QB. The process variations in V_t degrade the read SNM of standard 6T and proposed 6T bitcell by up to 50% and 13% respectively compared to nominal design corner as shown in Fig. 5. The proposed 6T bitcell provide $2.65X$ higher worst-case read SNM as compared to the standard 6T SRAM bitcell under same process variations. Thus, the proposed 6T bitcell has better worst-case noise margin and process variation tolerant.

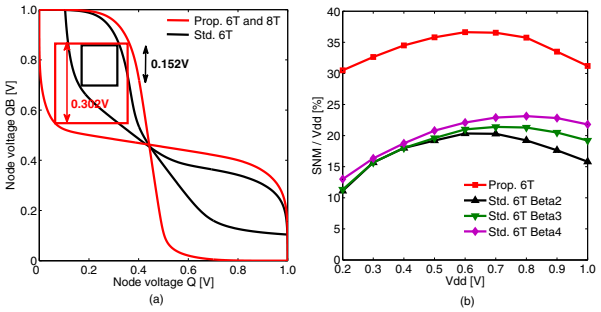

Fig. 4. SNM comparison of standard 6T, 8T and proposed 6T bitcell during a read operation at $V_{dd} = 1V$ in Fig. (a). SNM normalized to supply voltage for different cell ratio ($\beta = 2$, 3 and 4) is shown in Fig. (b).

Read operation of an 8T bitcell is similar to the proposed 6T bitcell, such as precharging of the read bitline prior to each read operation and sensing the data directly from bitline. Also both proposed 6T and 8T bitcells employ the isolated read-port mechanism, therefore, read SNM of the proposed bitcell is equivalent to an 8T bitcell.

D. Write-Aility Margin

Write ability of a standard 6T SRAM bitcell is best characterize using write trip voltage which is defined as the maximum voltage on the bitline needed to flip the bitcell content [12]. Due to asymmetric nature of the proposed 6T SRAM bitcell, we have analyzed both the states for writing

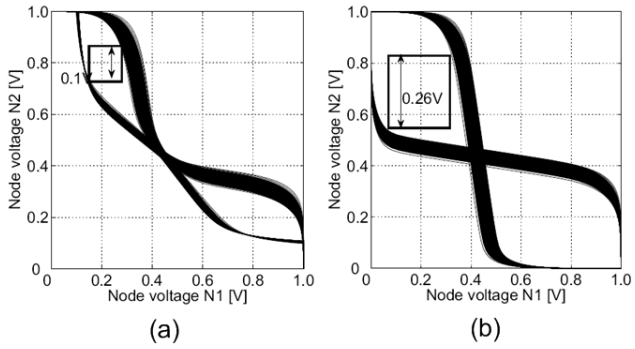

Fig. 5. Monte Carlo simulation of voltage transfer characteristics (VTCs) shown with worst case SNM during read operation (a) for standard 6T and (b) for proposed 6T and 8T bitcells.

'1' and '0'. In order to write '1' (Q= 1 and QB = 0) to a bitcell storing '0' (Q = 0 and QB = 1), low internal node Q of the bitcell is pulled up above the trip voltage of the INV1. Since, the pull down strength of the INV2 has been weaken during write access time due to stacked transistor M_{WA}, it makes pulling up of low internal node Q above the trip voltage easier. Similarly, writing '0' (Q = 0 and QB = 1) to a cell storing '1' (Q = 1 and QB = 0), high internal node Q of the cell has to discharge via bitline (BL) well below the trip voltage of the INV1, so that the cross-coupled inverter pair starts working and the cell content gets flipped. To guarantee that a correct write operation will occur, it is important that the node Q is pulled up (down) above (below) the trip voltage of INV1 within the write access time i.e. when WWL is high otherwise a write failure will occur.

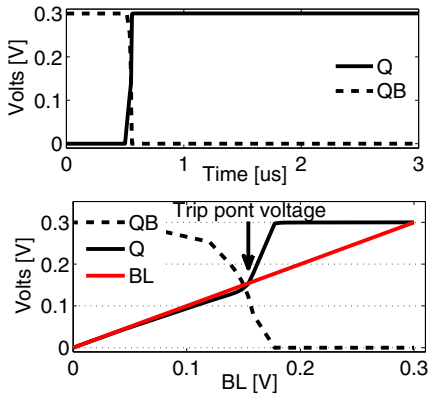

Fig. 6. Transient SPICE simulation of write trip voltage of the proposed 6T bitcell at V_{dd}=0.3 V for writing $0 \rightarrow 1$.

For the transient SPICE simulations of write trip point voltage, a metric has been widely adopted is used for measuring the write-ability (write margin) of proposed 6T and 8T bitcells are shown in Fig.6 and 7 respectively. The simulation results, demonstrate the write-ability of the proposed 6T and 8T bitcells at V_{dd}=0.3 V for writing $0 \rightarrow 1$. Writing $0 \rightarrow 1$, is shown here because in the proposed 6T writing $1 \rightarrow 0$ is easier and quicker, however, in 8T the writing is symmetric. The write trip point voltage of the proposed 6T is 13% (148mV) higher than 8T bitcell where a virtual VDD scheme has used. Thus, the proposed design has little bit less write-ability compared to 8T bitcell. However, it has an advantage since an erroneous write will not take place easily compared to 8T [1], due to bitline noise.

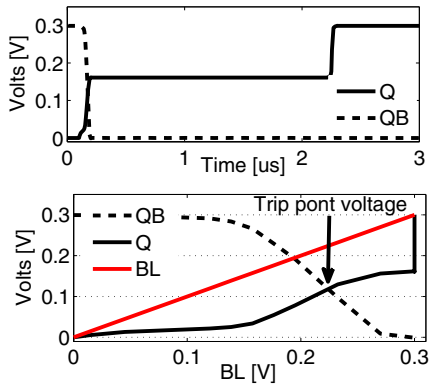

Fig. 7. Transient SPICE simulation of write trip voltage of the proposed 8T [1] bitcell at V_{dd}=0.3 V for writing $0 \rightarrow 1$.

IV. Bitline Leakage

The maximum number of bitcells per bitline are limited by total bitline (BL) subthreshold leakage currents from the unaccessed bitcells, which makes conventional data sensing impractical [1], [9]. In [1], the BL leakage problem is solved by using the read-buffer foot which is shared among the bitcells of a word. In the proposed design sub-V_t leakage current from the unaccessed bitcells is data dependent and in the worst case when all the unaccessed bitcells hold '0' as shown in Fig. 8(a). In the worst case read operation, when the bitline is precharged to V_{DD}, the read assist transistors of all the unaccessed bitcells are in cut-off region because of low read wordline (RWL=0). The subthreshold leakage current of a NMOS transistor is mainly depends on the V_{DS}, when V_{GS}=0V. Hence, subthreshold leakage current from the proposed 6T read-port is reasonably lower than the 8T read-port, because V_{DS} of a transistor controlled by RWL in 6T read-port is less than the 8T read-port transistor by a factor of V_t/V_{DD}.

The transient SPICE simulations for BL voltage of a proposed 6T bitcell are shown in Fig. 8(b). To read '0', BL is correctly pulled low by the read-port of an accessed bitcell. While it remains high for reading '1' when the accessed bitcell holds '1' and unaccessed bitcells in that column hold '0'. It should be noticed that the BL is not erroneously pulled low by the leakage currents of the unaccessed 255 bitcells. However, a small 10% residual droop can be observed, due to the gate and junction leakage from the read-port transistors.

In order to make certain in the proposed design that the BL leakage does not cause any misread or erroneous reads,

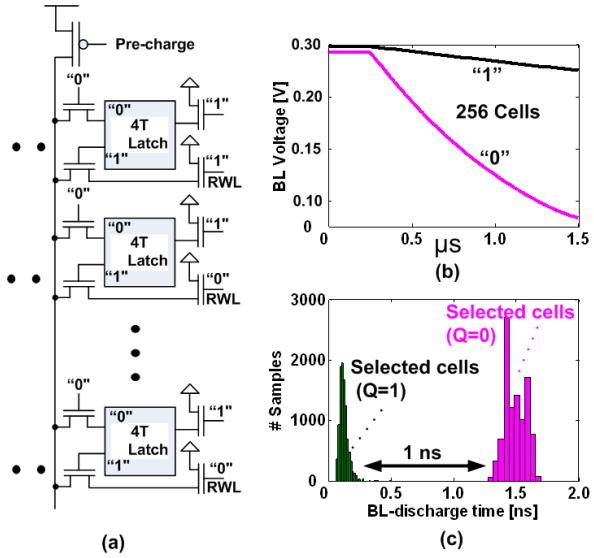

Fig. 8. Proposed 6T bitcell (a) BL leakage (b) BL not erroneously pulled low (c) BL discharge time distribution for storage node Q is '1' and '0'.

it must provide a distinguishable bitcell read current from the leakage. The BL discharge time for reading '1' and '0' was compared. The distribution of BL discharge time from V_{DD} to $0.5 \times V_{DD}$ when the bitcell storage node Q is "high" and "low". The 32 bitcells/word and 256 bitcells/BL module was used. The BL discharge time distribution with 255 unaccessed bitcells is shown in Fig. 8(c). It can be seen that the clearance of BL discharge time between the slowest bitcell for Q=1 and the fastest bitcell for Q=0 is 1ns, so there is enough timing margin to latch the data exactly.

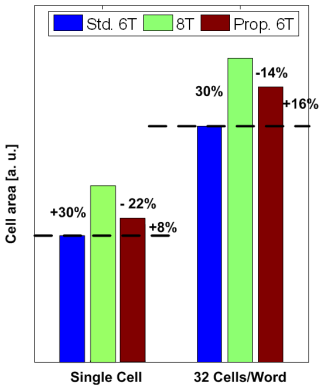

Fig. 9. Comparison of a bitcell and a 32-bit word area for standard 6T, 8T [1] and the proposed 6T.

V. Area, Power and Performance of the 6T SRAM Array

Fig. 10 shows the layout of the proposed word-organized 6T SRAM bitcell with four bitcells and read/write assist transistors. We present only four cells for clarity. The proposed bitcell layout area is $0.68\mu m^2$ ($0.55\mu m \times 1.22\mu m$, read and write assist transistors excluded), which is 8% higher (because of additional contacts) than the standard 6T SRAM bitcell for $\beta = 2$ and 22% less than the 8T bitcell [1]. However, due to the need to resize the read assist transistor the area of a 32-bit word with proposed bitcell is 16% (including the read and write assist transistors) higher than the standard 6T bitcell and 14% less than the 8T bitcell, as shown in Fig. 9. We have used three metal layers (M1, M2 and M3). Metal layer M1 is used for routing the supply rails (V_{DD} and V_{SS}), M2 is used for routing the shared contacts among bitcells, read and write signals. M3 is used for routing the bitlines. The design has been successfully laid-out for different word sizes. Parasitic were extracted and included in a SPICE deck for simulation results presented in this paper.

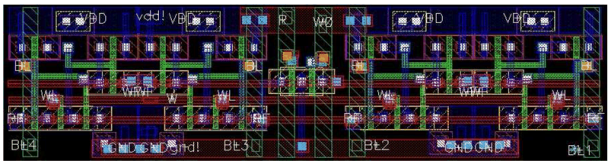

Fig. 10. Layout of the proposed word-oriented 6T SRAM bitcell with four bitcells and read/write assist transistors in the middle.

A. Power Dissipation

Fig. 11 shows the read operation waveforms of 6T and 8T bitcells. Read operation waveforms of both the bitcells are identical, because both employ the single ended isolated read-port mechanism. Hence, bitline power dissipation pattern for read event in both the bitcells is identical. Write operation of standard 6T and 8T bitcells are identical and hence they have identical write power dissipation pattern from bitlines. However, the proposed 6T has a different write mechanism because it employs single ended write via a pass gate device. As most of the active power up to 70% of the total is dissipated in BLs dis/charging during read/write operation in SRAMs [3], hence, BLs dis/charging pattern is a good measure for active power. Fig. 11 depicts that a certain amount of power is dissipated in 6T by precharging the BL prior to a read operation and discharging only when BL has to changed. However, no power is dissipated by the BL if the upcoming bit is the same (only for high) as previous one. Similarly, for write operation, precharging of the BL dissipates a certain amount of power for each write operation if the upcoming bit is the same(only for low) as previous one. However, no power is dissipated in BL if the upcoming bit is the same (only for high) as the previous one.

Fig. 12 compares active power in the proposed 6T, standard 6T and 8T bitcells for different read/write operations. As 6T and 8T bitcells are asymmetric in nature, their active power consumption pattern is also asymmetric. In Fig. 12 operation W0_1 stands for writing '1' into the bitcell while its original content was '0'. Similarly, R1_0 stands for reading '0' from the bitcell, while its previous output was '1'. For operations R1_1 the active power of 6T/8T bitcells has drastically reduced as compared to standard 6T bitcell, because R1_1 operation is

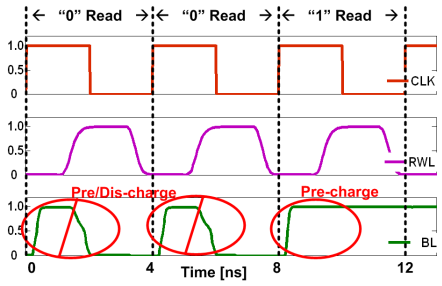

Fig. 11. Transient SPICE simulation of bitline (BL) precharging and discharging during read operation of proposed 6T and 8T bitcells.

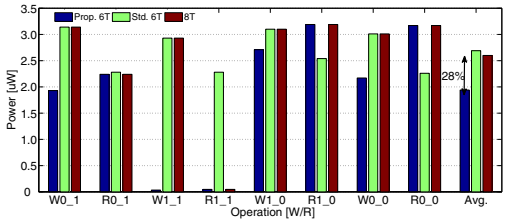

Fig. 12. Active power pattern for different read/write operations of proposed 6T, standard 6T and 8T SRAM bitcells.

performed without dis/charging the read bitline of the 6T/8T bitcells. Under such operations, pre/charged bitline can be used for future read/write operation. Alternatively, in 6T bitcell one bitline has to discharge during these operations. The average active power under different read/write operations in the proposed 6T is 28% and 25% lower than the standard 6T and 8T bitcells [Fig. 12].

B. Read access time

Fig. 13 compares the distribution of the read access time of proposed 6T, standard 6T and 8T bitcells. The read access time distribution was obtained by the Monte Carlo simulations. Each bitcell was simulated under 4σ random variations in threshold voltage of each transistor. For the proposed 6T and 8T read access time was calculated when the read wordline (RWL) rises to $0.5 \times V_{DD}$, where,V_{DD}=1V, to a time when the output of the sense amplifier is reached to $0.5 \times V_{DD}$. Similarly, in standard 6T read access time was defined as the time between the WL rises to $0.5 \times V_{DD}$ to a time when we got the expected differential voltage of bitlines $(50mV)$. The mean read access time of proposed 6T and 8T bitcells is very close that is $2.76ns$ and $2.48ns$, respectively. The read access time of the proposed 6T bitcell is 10% higher than that of the 8T bitcell because we swap the position of the read-port control transistor with respect to 8T bitcell, reducing the read performance of proposed the 6T bitcell. However, the mean read access time of standard 6T bitcell is significantly lower, compared to the proposed 6T and 8T bitcells because of the use of a differential sense amplifier.

VI. Conclusion

A single ended SRAM 6T bitcell design and its word-orientation for robust, high density and low power SRAMs

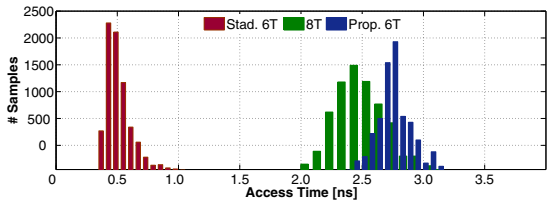

Fig. 13. Distribution of read access time of proposed 6T, standard 6T and 8T bitcells.

is presented in this paper. The immunity to device parameter variability and high density in the proposed design is achieved by isolating the read current path. The improved read and write-ability, reduced active and leakage power dissipation compared to standard 6T and 8T bitcells makes the new approach attractive for nano-CMOS regime in which process variation is a major design constraint. Experimental results shows that the proposed design has tremendous potential for nano-CMOS SRAM design, such as $2.65\times$ worst case SNM compared to standard 6T.

VII. Acknowledgment

Author Jawar Singh acknowledges support from the Government of India, National Overseas Fellowship award no.11015/12/2005/SCD-V. Author Saraju P. Mohanty acknowledges partial support from NSF award no. 0702361.

References

[1] N. Verma and A. P. Chandrakasan, "A $256kb$ 65nm 8T Subthreshold SRAM Employing Sense-Amplifier Redundancy," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 141–149, Jan. 2008.

[2] I. Kiyoo, S. Katsuro, and N. Yoshinobu, "Trends in low-power ram circuit technologies," *Proceedings of the IEEE*, vol. 83, pp. 524–543, April 1995.

[3] L. Villa, M. Zhang, and K. Asanovic, "Dynamic zero compression for cache energy reduction," in *International Symposium on Microarchitecture*, 2000, pp. 214–220.

[4] N. S. Kim, K. Flautner, D. Blaauw, and T. Mudge, "Circuit and microarchitectural techniques for reducing cache leakage power," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 12, no. 2, pp. 167–184, 2004.

[5] A. Wang and A. Chandrakasan, "A 180 mv fft processor using subthreshold circuit techniques," in *Proc.IEEE ISSCC Dig. Tech. Papers*, 2004, pp. 229–293.

[6] C.-C. Wang, C.-F. Wu, R.-T. Hwang, and C.-H. Kao, "Single-ended sram with high test coverage and short test time," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 1, pp. 114–118, Jan 2000.

[7] Z. Liu and V. Kursun, "Characterization of a novel nine-transistor sram cell," *Very Large Scale Integration (VLSI) Systems, IEEE Transactions on*, vol. 16, no. 4, pp. 488–492, April 2008.

[8] R. Aly, M. Faisal, and M. Bayoumi, "Novel 7t sram cell for low power cache design," *SOC Conference, 2005. Proceedings. IEEE International*, pp. 171–174, 19-23 Sept. 2005.

[9] B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm sub-threshold sram design for ultra-low-voltage operation," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 3, pp. 680–688, March 2007.

[10] T.-H. Kim, J. Liu, J. Keane, and C. Kim, "A 0.2 v, 480 kb subthreshold sram with 1 k cells per bitline for ultra-low-voltage computing," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 2, pp. 518–529, Feb. 2008.

[11] "Predictive technology model (ptm)," http://www.device.eecs.berkeley.edu/ ptm/download.html/, 2008.

[12] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene, "Read stability and write-ability analysis of sram cells for nanometer technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2577–2588, Nov 2006.