A Subthreshold Single Ended I/O SRAM Cell Design for Nanometer CMOS Technologies

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***Abstract*— Lowering supply voltage is an effective technique for power reduction in memory design, however traditional memory cell design fails to operate, as shown in [3], [10], at ultra-low voltages. Therefore, to operate cells in the subthreshold regime, new cell structures needs to be explored. Towards this, we present a single-ended I/O (SEIO) bit-line latch style 7-transistor static random access memory (SRAM) cell (7T-LSRAM) as an alternative for nanometer CMOS technology which can function in ultra-low voltage regime. Compared to existing 6-transistor (6T) cell or 10-transistor cell design, the proposed cell has 2X improved read stability and 36% better write-ability at lower supply voltage. Furthermore, the 7T-LSRAM has improved process variation tolerance. The area analysis shows that there is 18% increase in area penalty compared to the standard 6T cell, however the improved performance and process variation tolerance could justify the overhead.**

I. Introduction and Contributions

Low energy consumption is the prime requirement of a memory dominated embedded systems as they are often battery powered. Lowering supply voltage is one of the options to reduce power (energy) consumption. However, ultra-low-power design of high-density SRAMs in which the operating voltage is below the transistor threshold voltage is extremely challenging. This is due to reduced static noise margin (SNM) and increased variability in design and process parameters. Therefore, reducing the operating voltage for memories to reduce the leakage power and active energy in energy constraint applications is one of the first choice of semiconductor manufacturers for ultra-low-power applications. Also for system integration, SRAM must be compatible with subthreshold combinational logic operating at ultra-low voltages [9].

In subthreshold, the standard 6T SRAMs fail to deliver the yield and density requirements [3]. The yield goes down due to several reasons including, the degraded static noise margin (SNM), poor write-ability, increased sensitivity of design and variation in process parameters. Moreover, the density requirement is mainly limited due poor driving capacity of the bit-lines, which allows fewer number of cells per bit-line and reduced bit-line sensing margin [10]. This motivates us to explore alternative SRAM cell structure suitable for nanoscale CMOS circuits operating at subthreshold targeted ultra-low-power applications. The research proposed in this paper has following contributions:

- In this paper, a single-ended I/O (SEIO) bit-line latch style 7T SRAM cell hereafter referred as 7T-LSRAM as an alternative for nano-CMOS technology is proposed.
- The proposed 7T-LSRAM cell can function in ultra-low voltage regime thus allowing subthreshold operation.
- The proposed 7T-LSRAM cell gives better read stability, better write-ability compared to standard 6T or 10T-ST cell. For comparison, apart from the standard 6T which is widely accepted as a standard design, we choose 10T-ST because this is one of the latest designs available in the literature [7].

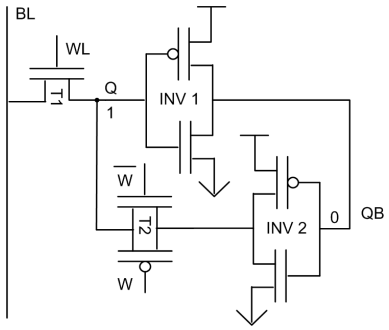

Fig. 1. Proposed single-ended I/O bit-line 7-transistor SRAM cell structure.

- The proposed 7T-LSRAM has improved process variation tolerance with respect to standard 6T cell and 10T-ST cell. This makes it attractive for nano-CMOS regime in which process variations are significant design constraint for important circuit elements like SRAM.

The rest of this paper is organized as follows. In Section II, we present the proposed cell design and its operation. Section III presents the experimental results and we also compared the cell design metrics with other cell designs in the literature. Further, we discussed how the proposed design well suited for future technologies. Final conclusions are drawn in Section IV.

II. Proposed SEIO 7T-LSRAM Cell Design

The proposed 7T-LSRAM cell that can function at ultra low voltage as shown in Fig. 1. The proposed SRAM cell consists of cross-coupled inverter pair (INV 1 and INV 2), read and write access transistor (T1), and transmission gate (T2). The transmission gate (T2) is used to open the feedback connection between inverters, INV 1 and INV 2, during the write operation. Instead of having two bit-lines as in standard 6T SRAM cell, these lines have been replaced by a single bit-line (BL). Both reading and writing operations are performed over the SEIO bit-line (BL). However, the word-line (WL) has to assert high prior to write and read operation as similar to standard 6T SRAM cell. During data retention period, when the SRAM cell is not being accessed, word-line (WL) is low and a strong feedback is provided to the cross-coupled inverters by the transmission gate T2.

Area of the proposed cell is compared with standard 6T, we have done the layout of both the cells. Fig. 2 (a) and (b) respectively shows one of the possible layouts of the standard 6T-SRAM and proposed 7T-LSRAM cells using $65nm$ CMOS technology. The DRC and LVS have been performed using ASSURA Cadence. Parasitic were extracted at the cell level and included in HSPICE deck for simulation. In the 7T-LSRAM cell one additional transistor and one extra line is required to be routed as compared to standard 6T SRAM cell. The

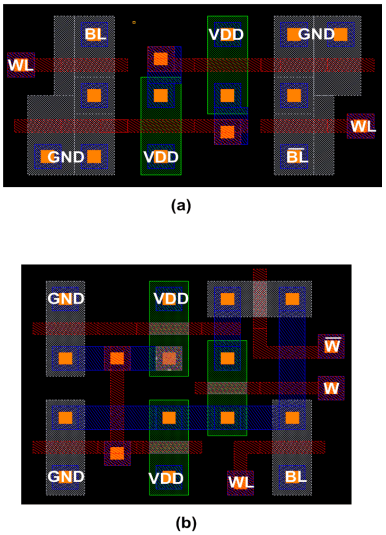

Fig. 2. (a) Standard 6T SRAM cell layout and (b) proposed latch style 7T SRAM cell layout.

proposed bit cell has estimated 18% more area than a standard 6T cell. It may be noted that the 18% area overhead is composed of not only one added transistor but also for the contact area of the write control signal W and $\bar{W}$. Thus, the area overhead due to use of 7T-LSRAM cells in target application is not significant and can be overlooked due to the advantages it provides.

A. Write Operation of the 7T-LSRAM Cell

A reliable write operation in nano-CMOS technology SRAMs at reduced V_{dd} is difficult due to ratioed contention between NMOS access and PMOS pull-up transistors. Several write assist circuits and weakening cross-coupled inverters techniques have been proposed to overcome this problem [2], [6]. It would be evident from [2], [6] that the weakening of the cross-coupled inverters has failed to provide improved SNM. In the proposed design, rather than weakening of the cross-coupled inverters we completely connects and disconnects the inverter through a transmission gate T2. This unique solution facilitates read SNM almost equal to hold SNM of the cell even at reduced supply voltage as shown in Fig. 5. Further, it also delimits the ratioed contention during write operation. The write operation begins with asserting WL high and disconnecting the feedback between inverters, INV 1 and INV 2. The feedback connection and disconnection are performed through a transmission gate T2 with appropriate write control signals. Once the inverters get disconnected, it is easy to charge/discharge the node Q to an equivalent level "1" / "0".

To illustrate a write "0" or "1" operation, initially we assume that the node Q at logic level "1" (or "0") and QB at logic level "0" (or "1"). Fig. 3 show the simulated timing diagram for write "0" and "1" operations. During write access, the word-line (WL) goes high which connects the bit-line (BL) to node Q and disconnects the feedback between inverters, INV 1 and INV 2 with the help of transmission gate T2. After write operation, cell feedback connection restores the full voltage level at node Q and QB which is marked in Fig. 3.

B. Read operation the 7T-LSRAM Cell

The read stability of the SRAM cell is well characterized and has been analyzed with static noise margin (SNM) both in standby and during read access mode in [1], [8]. The stability of SRAM cell is usually defined by the SNM as a maximum value of DC noise voltage

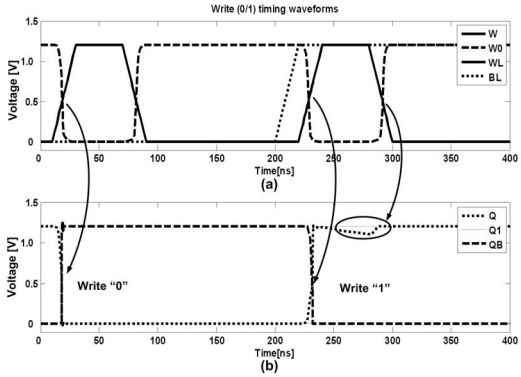

Fig. 3. Timing waveforms showing successful write "1" at node Q to the bit-cell.

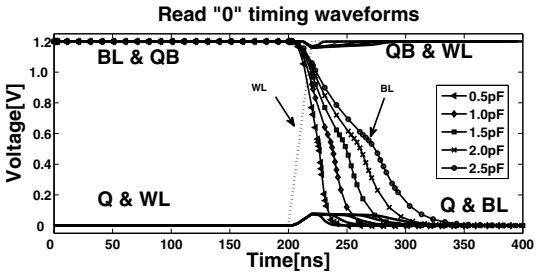

Fig. 4. Timing waveforms for read "0" when node Q at "0" and BL is precharged to $V_{dd} = 1.2V$ under different bit-line capacitance.

that can be tolerated without flipping the internal storage node state. It is well known that during read operation the read SNM of a standard 6T SRAM cell degrades. As prior to read access both bit-lines are precharged to logic level "1". Since, the "0" storage internal node of the cell gets pulled up to a voltage higher than ground through the access transistor because of voltage division effect between access transistors and pull down transistors which degrades the read SNM as shown in Fig. 5. This can be eliminated by the use of register file type of design [9], buffering of the node state [3] and to provide a independent read current path of the storage node [4]. In the proposed 7T-LSRAM cell, neither there is a buffering of the storage node nor independent current path being provided to the storage node during read access. The use of single ended I/O and transmission gate T2 which provides the strong coupling between inverters and prevent the "0" storage internal node of the cell to a much higher voltage than ground. Hence, the proposed design has improved read SNM equivalent to hold state SNM even at reduced V_{dd} as shown in Fig. 5.

For read operation, first precharge the bit-line (BL) and assert the word-line (WL) to a logic level "1". The access transistor T1 provides path to the storage node Q to charge/discharge the bit-line (BL) to an equivalent level "1" / "0". Fig. 4 illustrates the read "0" operation under different bit-line capacitance to show that there is no destructive read "0" failure due to rise in node Q voltage. The read "1" operation is not shown here as it is obvious and will not lead to destructive read failure because both the node Q and bit-line are at logic level "1".

III. Circuit Level Simulation Results

In this section, we present the circuit level simulation results based on the $65nm$ BPTM technology node using HSPICE^{TM}. A detail analysis and comparison of standard 6T-SRAM, Schmitt trigger based

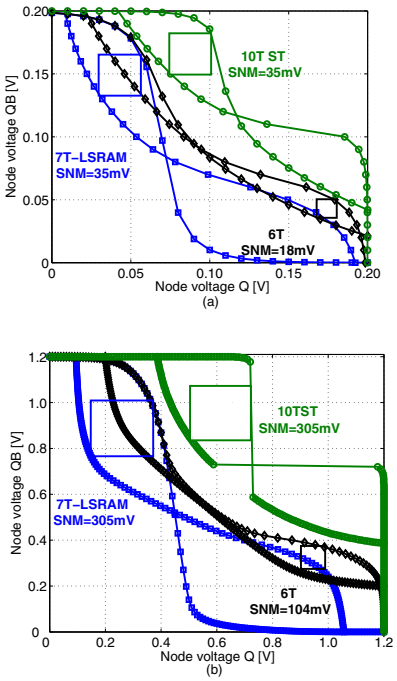

Fig. 5. Read static noise margin (SNM) comparison of standard 6T, 10T-ST and proposed 7T-LSRAM cell at (a) $V_{dd} = 0.2V$ and (b) $V_{dd} = 1.2V$.

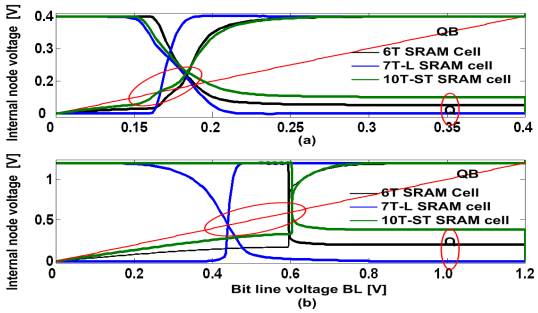

Fig. 6. WTP comparison of a standard 6T, 10T-ST [7] and proposed 7T-LSRAM cell at (a) $V_{dd} = 0.4V$ and (b) $V_{dd} = 1.2V$.

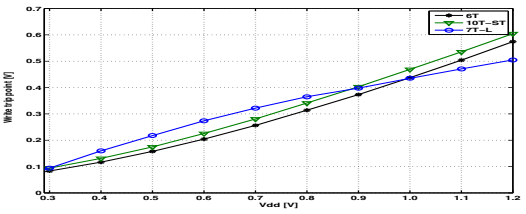

Fig. 7. WTP versus V_{dd} comparison of a standard 6T, 10T-ST and proposed 7T-LSRAM cell.

10T-ST [7] and proposed 7T-LSRAM cell at different V_{dd} and under process variations have been made. We have considered the widely used standard metrics for comparison of SRAM cells such as hold SNM, read SNM and write trip voltage.

A. Read and Hold Static Noise Margin

The static noise margin (SNM) voltage is the best measure for read and hold stability which is estimated graphically as the length of a side of the largest square that can be embedded inside the lobes of the butterfly curve [8]. The read SNM of the 7T-LSRAM cell is almost equivalent to hold SNM of the standard 6T cell, or in other words the proposed cell read stability degradation is low during read access. However, the 7T-LSRAM cell has about 3X improvement in the read SNM compared to standard 6T, while it has equal SNM to 10T-ST cell at $V_{dd} = 1.2V$. In the subthreshold regime at $V_{dd} = 0.2V$ the improvement in read SNM is about 2X and 1X as compared to standard 6T and 10T-ST cells respectively, as shown in Fig. 5. The use of differential read in the prior art SRAM cell design degraded the read SNM.

B. Write-ability

The write ability of a SRAM cell is best characterize with the help of write-trip-point (WTP), which determines how expensive in terms of energy it is, to write into a cell. Lower the write trip point higher the pulling down energy required and *vice-versa*. The write-trip-point defines the maximum voltage on the bit-line needed to flip the cell content [5].

Fig. 6 (a) and (b) show the WTP comparison of a standard 6T, 10T-ST and proposed 7T-LSRAM cell at $V_{dd} = 0.4V$ and $V_{dd} = 1.2V$, respectively. The WTP of the 7T-LSRAM cell is 12% and 16% less than the standard 6T and 10T-ST at $V_{dd} = 1.2V$ as shown in Fig. 6(b). Thus, it can be concluded that the writing operation of the proposed cell is 12% to 16% expensive in terms of energy consumption as compared to standard 6T and 10T-ST SRAM cells. In other words, 7T-LSRAM is more robust to noise that can cause undesirable write, because it require more energy to pull down the bit-line to change the cell state. Also after the write-trip point, state of both the internal node changes $1 \rightarrow 0$ or $0 \rightarrow 1$ perfectly, whereas in standard 6T and 10T-ST SRAM cell one of the internal node state floats after the trip-point as marked in Fig. 6(a) and (b). In the subthreshold regime at $V_{dd} = 0.4V$ the improvement in WTP is 36% and 22% higher as compared to standard 6T and 10T-ST SRAM cells as shown in Fig. 6(a). Thus, it can be concluded that the there is a significant amount of energy saving during write operation in subthreshold regime as compared to standard 6T and 10T-ST SRAM cells. In addition, it is observed that 7T-LSRAM has better WTP in lower operating voltage as compared to standard 6T, 10T-ST as shown in Fig. 7.

C. Process Variation Tolerance

The random dopant fluctuations and line edge roughness causes mismatch in design and process parameters of a device, particularly threshold voltage (V_{th}) which is a strong determinant of SRAM power performance and parametric failures [1]. The parametric failures such as read, write and access failures in SRAM can be characterized by the target value of the performance parameters such as read and hold SNM and WTP which determines the yield.

In order to evaluate and compare the effectiveness of the 7T-LSRAM cell under process variations, Monte Carlo (MC) simulations are done for performance parameters. The statistical distribution mean μ and standard deviation σ of the performance parameters are estimated for standard 6T, 10T-ST and 7T-LSRAM cell to take the variability into account due to variations in threshold voltage. We assume that the variation of V_{th} as an independent random variable with a Gaussian distribution for all the transistors in standard 6T, 10T-ST and proposed 7T-LSRAM cell.

The MC simulations of read SNM at $V_{dd} = 0.4V$ for a standard 6T, 10T-ST and proposed 7T-LSRAM cell are shown in Fig. 8, which shows that the process variation at lower voltage is more pronounced in standard 6T than 10T-ST and 7T-LSRAM cell. Statistical distribu-

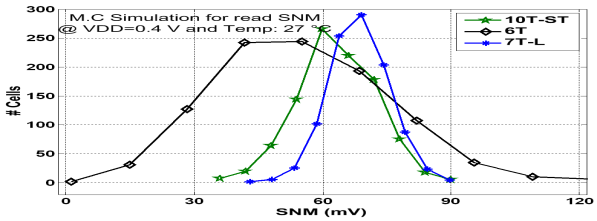

Fig. 8. MC simulation distribution of a standard 6T, 10T-ST and proposed 7T-LSRAM cell for Read SNM comparison at $V_{dd} = 0.4V$.

TABLE I
STATISTICAL DISTRIBUTION OF WTP AT $V_{dd} = 0.4V$

$V_{dd} = 0.4V$	$Mean(\mu)$ [mV]	$Std.Devi.(\sigma)$ [mV]
Standard 6T SRAM	117.63	12.55
10T-ST [7]	132.81	11.64
Proposed 7T-LSRAM	158.25	07.92

tion of WTP obtained from the MC simulation for a standard 6T, 10T-ST and proposed 7T-LSRAM cell at $V_{dd} = 0.4V$ and $V_{dd} = 1.2V$ are shown in Fig. 9. It is observed that the proposed 7T-LASRM cell has mean WTP about 12% and 16% less as compared to standard 6T and cell at $V_{dd} = 1.2V$. However, standard deviation of WTP at $V_{dd} = 1.2V$ is reduced by 12% and almost same as compared to standard 6T and 10T-ST SRAM cell respectively. At $V_{dd} = 0.4V$, mean of the WTP has increased by 36% and 22% as compared to standard 6T and 10T-ST SRAM cell respectively. However, standard deviation of WTP at $V_{dd} = 0.4V$ is reduced by 31% and 35% as compared to standard 6T and 10T-ST SRAM cell respectively. These statistical results are summarized in Table I and II. Thus, the proposed cell provides better process variation tolerance at low voltage operation.

D. Scalability

We have simulated the proposed cell under process variation for different design and process paramenters using the predictive technology models (PTM) and compared the results with standard 6T and 10T-ST cells. The analysis shows that 7T-LSRAM cell has better read, hold SNM and WTP compared to the standard 6T cell. For $V_{dd} = 0.2V$, using predictive models, the 7T-LSRAM cell predicts 2X improvement in read SNM compared to its counterpart standard 6T. Furthermore, for WTP the 7T-LSRAM cell has better write-ability of about 36% and 22% as compared to standard 6T and 10T-ST at $V_{dd} = 0.4V$. The above results show that proposed 7T-LSRAM cell scales well with future technologies. As mentioned earlier, with increased process variations, the memory cell failure probability would worsen at lower supply voltages.

IV. CONCLUSIONS

Subthreshold memory design has received a lot of attention in the past years, but most of them uses large number of transistor to

TABLE II
STATISTICAL DISTRIBUTION OF WTP AT $V_{dd} = 1.2V$

$V_{dd} = 1.2V$	$Mean(\mu)$ [mV]	$Std.Devi.(\sigma)$ [mV]
Standard 6T SRAM	574.94	12.10
10T-ST [7]	604.76	11.01
Proposed 7T-LSRAM	503.10	10.80

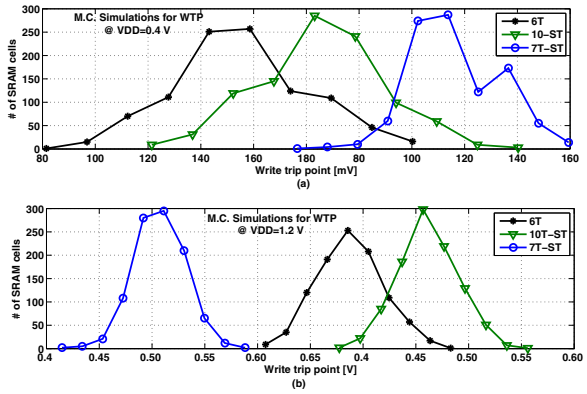

Fig. 9. MC simulation distribution of a standard 6T, 10T-ST and proposed 7T-LSRAM cell for WTP comparison at (a) $V_{dd} = 0.4V$ and (b) $V_{dd} = 1.2V$.

achieve subthreshold region operation. What is discussed in this paper is a 7T-LSRAM cell which uses moderate increase in area for ultra low voltage operation. Merits and demerits of the proposed design are investigated in detail and compared with existing approaches. Compared to existing designs, for instant standard 6T/10T-ST, the proposed cell has 2X improved read stability and 36% better write-ability at lower supply voltage. Our area analysis shows that there is 18% increase in area penalty compared to the standard 6T cell. The new 7T-LSRAM inherently process variation tolerant, this makes the new approach attractive for nanoscale technology regime in which process variations is a major design constraint.

REFERENCES

[1] A.J.Bhavnagarwala, X. Tang, and M. J.D. The impact of intrinsic device fluctuations on cmos sram cell stability. *IEEE Journal of Solid-State Circuits*, 36:658–665, Apr 2001.

[2] R. Aly, M. Faisal, and M. Bayoumi. Novel 7t sram cell for low power cache design. *SOC Conference, 2005. Proceedings. IEEE International*, pages 171–174, 19-23 Sept. 2005.

[3] B. Calhoun and A. Chandrakasan. A 256-kb 65-nm sub-threshold sram design for ultra-low-voltage operation. *IEEE Journal of Solid-State Circuits*, 42(3):680–688, March 2007.

[4] L. Chang, D. Fried, J. Hergenrother, J. Sleight, R. Dennard, R. Montoye, L. Sekaric, S. McNab, A. Topol, C. Adams, K. Guarini, and W. Haensch. Stable sram cell design for the 32 nm node and beyond. *VLSI Technology, 2005. Digest of Technical Papers. 2005 Symposium on*, pages 128–129, 14-16 June 2005.

[5] E. Grossar, M. Stucchi, K. Maex, and W. Dehaene. Read stability and write-ability analysis of sram cells for nanometer technologies. *IEEE Journal of Solid-State Circuits*, 41(11):2577–2588, Nov 2006.

[6] R. Hobson. A new single-ended sram cell with write-assist. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, 15(2):173–181, Feb 2007.

[7] J. Kulkarni, K. Kim, and K. Roy. A 160 mv robust schmitt trigger based subthreshold sram. *Solid-State Circuits, IEEE Journal of*, 42(10):2303–2313, Oct. 2007.

[8] E. Seevinck, F. List, and J.Lohstroh. Static-noise margin analysis of mos sram cells. *Journal of Solid-State Circuits*, 25 (2):784–754, 1987.

[9] A. Wang and A. Chandrakasan. A 180 mv fft processor using subthreshold circuit techniques. In *Proc.IEEE ISSCC Dig. Tech. Papers*, pages 229–293, 2004.

[10] M. Yamaoka, N. Maeda, Y. Shinozaki, Y. Shimazaki, K. Nii, S. Shimada, K. Yanagisawa, and T. Kawahara. Low-power embedded sram modules with expanded margins for writing. *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, pages 480–611 Vol. 1, 10-10 Feb. 2005.