Parasitic Aware Process Variation Tolerant Voltage Controlled Oscillator (VCO) Design

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Abstract

In this paper we present a parasitic aware, process variation tolerant optimization methodology that may be applied to nanoscale circuits to ensure better yield. A current-starved voltage controlled oscillator (VCO) is treated as a case study and to the best of the authors' knowledge, this is the first VCO design that accounts for both parasitic degradation and process variation together. The physical design of the VCO is carried out in a generic $90nm$ *Salicide* $1.2V/2.5V$ *1 Poly 9 Metal process design kit. The oscillation frequency is the objective function with the area overhead as constraint. A performance degradation of* 43.5% *is observed when the parasitic extracted circuit was subjected to worst case process variation. After a single physical design iteration, the frequency of oscillation was within* 4.5% *of the target.*

1 Introduction and Motivation

As CMOS technology scales to the nanometer region, process variations cause significant interconnect and device inter- and intra-die parameter variations. These variations include device geometry change, dopant density change, threshold voltage and circuit timing change, etc. The circuit's parasitics also cause further circuit performance degradation. In other words, parasitics along with process variation can lead to severe degradation in circuit performance. Capturing and modeling the process variation becomes essential to device and interconnect extraction tools for accurate timing and power analysis. Traditional parasitic extraction is no longer adequate for todays technology. The standard design cycle must include process variation along with parasitic extraction, in order to produce variation tolerant physical designs.

Parasitic and process variation aware optimization methodologies require that the parasitics be considered at the beginning of the design. Where radio frequency (RF) components are designed assuming ideal components, it is observed that parasitics have serious degrading effects at high frequencies. The only way to overcome these effects is to consider parasitics as an integral part of the circuit. This motivates the essential need for parasitic-aware design and optimization. If parasitics have an acute effect on the design, as in an RF VCO, an early layout needs to be created so that the parasitics can be extracted and their effect estimated. Without that early layout-parasitic information, designers rely mostly on experience.

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2 Design Issues and Contributions

Multiple iterations between the front-end circuit design and back-end layout, are normally required to achieve parasitic closure in radio frequency integrated circuits [11]. Let us assume that such manual process requires X number of iterations. The primary purpose of our methodology is to reduce the number of manual iterations to 1, by performing the X number of iterations on a parasitic parameterized netlist instead of the layout. Hence, we reduce the X number of iterations required for parasitic closure, to one manual physical design iteration. The proposed design flow is shown in figure 1. In the process variation analysis step, the parasitic parameterized netlist is subjected to worst case process variations, and then optimized. This procedure ensures that the resulting final physical design is not only resistant to parasitic effects, but also to process variations.

This is a novel methodology for physical design of nanoscale CMOS (nano-CMOS) RF components to meet the required design specifications. It is a 1 iteration approach, in which the layout has to be done only twice. Once before the optimization, and once after the optimization. In this communication, the fully extracted physical design (consisting of resistors (R), capacitors (C), inductors (L) and mutual inductors (K)) is optimized to meet the target specification of oscillation frequency, while being subjected to *worst-case* process variation. However, this technique could be applied to optimize other parameters as well, e.g. phase noise, etc. The design, discussed in section 4 is of a high frequency, low phase noise VCO. As can be seen from figure 2, there is large discrepancy between the oscillation frequency of the logical design and the physical design. The physical design was then subjected to process variation analysis. The third curve in figure 2 shows that the discrepancy increases even more when the VCO was subjected to

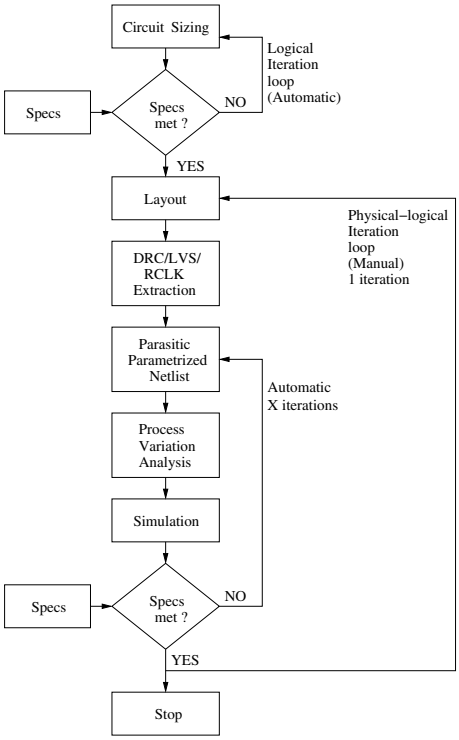

Figure 1. Proposed Circuit-Parasitic and Process-Variation Aware RFIC design flow

worst case process variation. The optimization was carried out using the parasitic-aware netlist generated by the physical design in a worst case process variation environment, and then the next iteration in the physical design was carried out using the optimized parameters. This constitutes 1 iteration. The optimized physical design was then tested, and the results are presented in figure 5. Hence the convergence for the objective was achieved using only 1 iteration. More details are presented in section 5.

3 Related Research Works

Many research address parasitic and variation aware design to overcome degradations due to device and package parasitics and to achieve optimal performance [9, 2]. A few CMOS RF circuits have been synthesized using the parasitic-aware optimization technique implemented with a simulated annealing heuristic [4, 7, 8]. In [3], an LC VCO has been subjected to a parasitic-aware synthesis. In [10], a design of experiments approach has been used to optimize the oscillation frequency. A simulation-based circuit synthesis example is presented in [12]. In [6], a current-controlled oscillator is subjected to process variations.

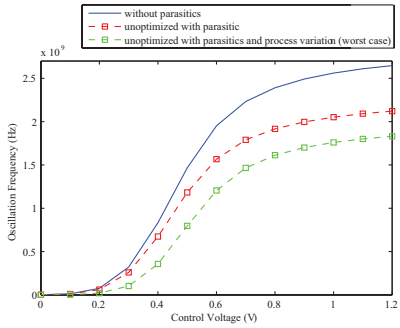

Figure 2. Frequency-voltage transfer characteristics of the unoptimized VCO

4 Logical Design of the VCO

The type of VCO considered in this work is of the current starved type, as other designs require large resistors and capacitors consuming large silicon area. The design, as shown in figure 3, comprises of two input stage transistors with high impedance, an odd numbered chain of inverters along with two current source transistors per inverter, which limit the current flow to the inverter; that is they are starved for current. The circuit has no stable operating point and it will oscillate at some frequency that is determined by the number of inverters, size of the transistors in the circuit, and the current flowing through the inverter, which is dependent upon the input voltage to the VCO. The operating frequency of the VCO, f_0 can be determined using a simple capacitance charging estimate [1]:

$$f_0 = \left(\frac{I_D}{N * C_{tot} * V_{DD}} \right), \quad (1)$$

where V_{DD} is the supply voltage, I_D is the current flowing through the inverter, N is the odd number of inverters in the VCO circuit and C_{tot} is the total capacitance of each stage given by the sum of the input and output capacitances of an inverter. The operating frequency of the VCO can be mainly controlled by an applied DC input voltage, which adjusts the current I_D through each inverter stage. The total capacitance C_{tot} is calculated as follows:

$$C_{tot} = \left(\frac{5}{2} \right) C_{ox}(W_p L_p + W_n L_n), \quad (2)$$

where C_{ox} is the gate oxide capacitance per unit area, W_n and W_p are the widths and L_n and L_p are the lengths of the inverter NMOS and PMOS transistors, respectively. The gate oxide capacitance per area C_{ox} is calculated as:

$$C_{ox} = \left(\frac{\epsilon_{r_{ox}} \epsilon_0}{T_{ox}} \right), \quad (3)$$

where $\epsilon_{r_{ox}}$ is the relative permittivity of SiO_2, ϵ_0 is absolute permittivity, and T_{ox} is the gate oxide thickness.

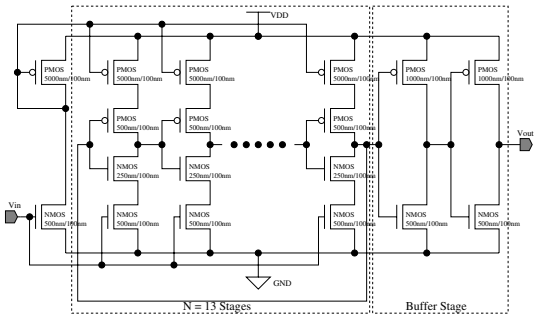

Figure 3. Nominal case logical design of VCO

The functional specification for the design is the oscillation frequency. The target oscillation frequency is kept at a minimum of $2GHz$ for this design. The number of stages is fixed to 13 to ensure the high frequency requirements and an area optimal design. Minimum sized transistors were used to design the inverters. The length is kept constant for all devices. Hence, $L_n = L_p = 100nm$, $W_n = 250nm$ and $W_p = 2{*}W_n = 500nm$. Choosing minimum width transistors also ensures an area optimal design. The current starved NMOS and PMOS devices are sized to provide the required current I_D. Thus, we obtained $L_{ncs} = L_{pcs} = 100nm$, and $W_{ncs} = 500nm$ and $W_{pcs} = 10 * W_{ncs} = 5\mu m$, where W_{ncs} and W_{pcs} are the widths and L_{ncs} and L_{pcs} are the lengths of the current-starved NMOS and PMOS transistors, respectively.

5 Performance Optimization of the VCO for Parasitics and Process Variations

5.1 Design Optimization

As can be seen from equations (1) and (3) that the oscillation frequency depends on V_{DD}, and V_T (I_D depends on V_T), and gate oxide thickness T_{ox}. Hence any variation in these process (V_T, T_{ox}) parameters and supply (V_{DD}), would lead to a degradation in the oscillation frequency. Process variations can be modeled using technology files or analytical formulae. Technology files are process dependent and can be created based on the information provided by foundries. In this work, a technology file based on a general 90nm process design kit was used, in which the oxide thicknesses (T_{ox}) and threshold voltages (V_T) were modeled for their worst case values. Also the supply voltage was modeled for its worst case value. For the design optimization, first a baseline logical design was performed using the design equations presented in section 4. The physical design was prepared using that baseline design. After full-extraction ($RCLK$), a 25% degradation in the oscillation frequency was observed between the logical and physical designs. The physical design was then subjected to process and supply variation where V_{DD}, $V_{T,NMOS}$, $V_{T,PMOS}$, $T_{ox,NMOS}$ and $T_{ox,PMOS}$ were varied by $+/-10\%$ from their nominal values. The worst case was identified as the one in which V_{DD} reduced by 10%, and all the process parameters increased by 10%. In this case, a 43.5% discrepancy was observed between the logical and physical designs. The results are summarized in Table 1.

Table 1. Summary of frequency discrepancy

Parameter	Unoptimized Physical Design	Unoptimized Physical Design + Process variation	Optimized Physical Design + Process Variation
frequency	$1.56GHz$	$1.13GHz$	$1.91GHz$
discrepancy	25%	43.5%	4.5%
V_{DD}	$1.2V$ (nominal)	$1.08V$ (-10%)	$1.08V$
$V_{T,NMOS}$	$0.1692662V$ (nominal)	$0.186193V$ ($+10\%$)	$0.186193V$
$V_{T,PMOS}$	$-0.1359511V$ (nominal)	$-0.149546V$ ($+10\%$)	$-0.149546V$
$T_{ox,NMOS}$	$2.33nm$ (nominal)	$2.563nm$ ($+10\%$)	$2.563nm$
$T_{ox,PMOS}$	$2.48nm$ (nominal)	$2.728nm$ ($+10\%$)	$2.728nm$

The initial values of various attributes are: (i) Target oscillation frequency $f_0 = 2GHz$. (ii) Logical design oscillation frequency $f_{0,\text{logical}} = 1.95GHz$. (iii) Physical design oscillation frequency $f_{0,\text{physical}} = 1.56GHz$. (iv) Physical design oscillation frequency in a worst case process variation environment $f_{0,\text{physical}-\text{process}} = 1.13GHz$.

The parasitic-aware netlist generated from the first layout iteration is modified by varying the design variables in order to achieve the required oscillation frequency in a worst case process variation environment. The widths of PMOS and NMOS devices in the inverter (W_n, W_p) and the PMOS and NMOS devices in the current-starved circuitry (W_{ncs}, W_{pcs}), and the lengths of all devices ($L_n = L_p = L_{ncs} = L_{pcs} = L$) constitute the design variables.

These are the constraints for the design methodology. The objective is to achieve a minimum target oscillation frequency of $2GHz$. The stopping criterion is kept at 2% of target. This netlist is then used in an optimization loop using a circuit simulator and a conjugate gradient optimization technique. The final optimized values obtained for the design variables are recorded in Table 2. The physical design of the VCO is then carried out using these parameter values, and the following results are obtained: (i) Target oscillation frequency $f_0 = 2GHz$. (ii) Logical design oscillation frequency $f_{0,\text{logical}} = 1.95GHz$. (iii) Physical design oscillation frequency in a worst case process variation environment $f_{0,\text{physical}-\text{process}} = 1.91GHz$. (iv) Physical design oscillation frequency in a nominal case process environment $f_{0,\text{physical}-\text{nominal}-\text{process}} = 2.54GHz$.

Hence we obtain a final optimized layout, with $1.91GHz$ oscillation frequency under worst case process variation, and $2.54GHz$ oscillation frequency in nominal conditions. We are able to obtain convergence with only 1 iteration in

Table 2. Summary of design parameters

Parameters	Varied from	Varied to	Optimized value
W_n	$200nm$	$500nm$	$415nm$
W_p	$400nm$	$1\mu m$	$665nm$
W_{ncs}	$1\mu m$	$5\mu m$	$4\mu m$
W_{pcs}	$5\mu m$	$20\mu m$	$19\mu m$
L	$100nm$	$110nm$	$100nm$

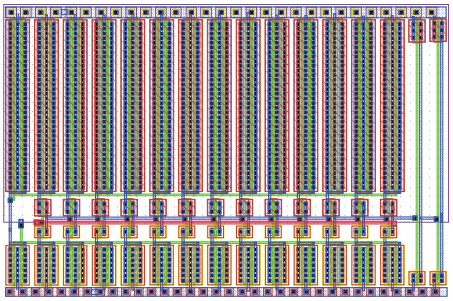

Figure 4. Final optimized layout of the VCO

layout. This technique can be applied for optimization of other parameters such as phase noise, jitter etc. [5].

5.2 Physical Design of the Optimal VCO

The physical design of the VCO has been carried out using a generic $90nm$ Salicide 1.2V/2.5V 1 Poly 9 Metal process design kit. A full extraction of the layout is performed (including resistors (R), capacitors (C), inductors (L) and mutual inductors (K)) so that the impact of inductive coupling could be assessed and minimized on the layout. The final layout is shown in figure 4, which is the optimal design, resistant to process variations and parasitics. As can be seen from the figure, multi-fingered transistors are laid out to minimize the area overhead, considering that the optimization resulted in wide transistors.

5.3 Characteristics of the Optimal Circuit

Figure 5 shows the frequency-voltage transfer curves for the logical and physical designs after optimization. It is evident that the optimized curve closely follows the logical design curve. We also obtained a phase noise of $-109.13dBc/Hz$ at an offset frequency of $10MHz$.

6 Conclusions

In this paper, we present a novel parasitic and process variation aware design methodology for optimization of performance for RF circuit components. The oscillation frequency has been treated as the target specification in a VCO. The degradation of the oscillation frequency due to parasitic and process variation effects has been narrowed down from 43.5% to 4.5%. This was achieved in only one iteration of the physical design, a tremendous reduction in overall design time. Thus we obtained a process variation

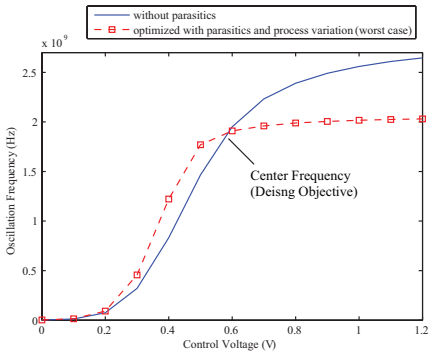

Figure 5. Frequency-voltage transfer characteristics of the optimized VCO

Table 3. Measured Performance of the VCO

Parameter	Value
Technology	$90nm$ CMOS $1P$ $9M$
Supply Voltage (V_{DD})	$1.2V$
Oscillation frequency (Nominal process)	$2.54GHz$
Process and supply variation	V_T $(+10\%)$, T_{ox} $(+10\%)$, V_{DD} (-10%)
Oscillation frequency (Worst-case process)	$1.91GHz$
Number of design variables	5 (W_n, W_p, W_{ncs}, W_{pcs}, L)
Number of objectives	1 ($f_0 >= 2GHz$)

aware design, as the target technology is nano-CMOS in which such variations do affect design metrics and yield. The performance summary of the VCO is given in Table 3.

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