A Dual Oxide CMOS Universal Voltage Converter for Power Management in Multi-V_{DD} SoCs

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Abstract

Level converters are becoming overhead for the circuits they are being employed in. If their power consumption continues to grow, they will fail to serve the very purpose they were built for. In this paper we propose the application of a dual-T_{ox} (DOXCMOS) technique for the power-delay optimization of a DC to DC voltage level converter under oxide thickness (T_{ox}) and transistor geometry constraints. The results show power savings of 83% and delay improvement of 60% over existing designs. The proposed level converter is capable of performing level-up/down conversion, and blocking of the input signal. The design is area optimal, with a minimum number of transistors. It is a robust design producing a stable output for voltages as low as $0.6V$ and loads varying from $10fF$ to $200fF$ for a $90nm$ technology. The average power dissipation of the converter with a $45fF$ capacitive load is $19.89\mu W$. The entire design cycle has been carried out up to physical design, including parasitic re-simulation. To the best of the authors' knowledge, this is the first level converter designed using a DOXCMOS technology for power-delay optimization.

1 Introduction and Motivation

The demand for low power consuming circuits is increasing with the requirements for personal computing devices and wireless communications equipment. Several factors, such as battery life, heat dissipation, packaging costs, environmental concerns, and reliability issues are driving this demand. Dynamic power management techniques using variable supply voltage (variable V_{dd}) are popular for system level power reduction and multiple supply voltage (Multi-V_{dd}) is a static solution for switching power reduction in ASICs. Since selective voltage reduction is a commonly used technique for overall power minimization, there is a need for the design of efficient level converters that have minimal area and power overhead.

For switching power reduction, a level-down conversion is required, where the non-critical blocks of the circuit are made to operate at lower power supply voltage [4]. A level-up converter is used as an interface where low V_{dd} cells (V_{ddl}) drive high V_{dd} cells (V_{ddh}) in order to reduce the short-circuit power dissipation [12]. One application is the dual-V_{dd} FPGA fabric [6]. In the standby mode of a circuit, no active switching occurs and all power dissipation is due to standby leakage. A simple power-saving scheme could be to shut off unused blocks in the standby mode. Thus, we propose a voltage level converter that can perform all these functions, step-up, step-down and blocking of signals. We call it a *Universal voltage-Level Converter* (ULC).

2 Contributions of this paper

The main contribution of this paper is the design of a power (accounting for dynamic power, subthreshold leakage, and gate leakage), delay, and area optimal voltage converter using nanoscale CMOS processes. The optimization constraints are the transistor oxide thickness and geometry. This level converter is capable of performing three types of operations on the voltage signal: (i) level-up conversion, (ii) level-down conversion, and (iii) blocking. To accomplish these tasks, universal level converter is made programmable. This design is thus suitable for dynamic power management. The physical design of the universal level converter conforms to the standards of Design For Manufacturability (DFM). The use of double vias ensures that a fault tolerant design is achieved. The metal lines are spread out to reduce cross-talk and ensure noise free power supply. This also ensures increase in functional yield and reliability. A unique contribution of this work is the introduction of dual-T_{ox} techniques in essentially analog designs. This approach allows the selective optimization of the conflicting targets of concurrent power, speed and area minimization.

3 Power and Delay Models and DOXCMOS Technology based Optimization Approach

3.1 Power Model

As transistors have been scaled down below the $100nm$ node, leakage composes nearly 50% of total power consumption. The reason for this is that the supply voltage has continually scaled down to reduce the dynamic power

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consumption of integrated circuits which depends on the square of the supply voltage. As the supply voltage is scaled down, to maintain performance, the threshold voltage has to be reduced in the same proportion. As threshold voltages are reduced, subthreshold leakage rises exponentially. For nanoscale technologies, gate-oxide leakage also arises.

The dynamic power consumption of a circuit is [8]:

$$P_{dynamic} = \alpha C_L V_{dd}^2 f, \tag{1}$$

This power depends on loading condition and not the device features. The subthreshold leakage in a transistor is [2, 10]:

$$I_{sub} = \mu_0 \left(\frac{\epsilon_{ox} W_{eff}}{T_{ox} L_{eff}}\right) v_{therm}^2 e^{1.8} exp\left(\frac{V_{gs} - V_T}{v_{therm} S}\right)\left(1 - exp\left(\frac{-V_{ds}}{v_{therm}}\right)\right) \tag{2}$$

It is clear from above that if T_{ox} is increased, the length (L_{eff}) is increased, and/or the width (W_{eff}) is reduced, there will be a reduction in the subthreshold current. Gate-oxide leakage current density of a device is [1, 10, 7]:

$$J_{DT} = A\left(\frac{V_{ox}}{T_{ox}}\right)^2 exp\left(\frac{-B\left(1 - \left(1 - \frac{V_{ox}}{\phi_{ox}}\right)^{\frac{3}{2}}\right)}{\left(\frac{V_{ox}}{T_{ox}}\right)}\right), \tag{3}$$

From this expression, we can see that gate leakage is exponentially dependent on variations in T_{ox}.

The total power of the ULC circuit is calculated as:

$$P_{ULC} = P_{dynamic} + P_{subthreshold} + P_{gate-oxide}, \tag{4}$$

where $P_{dynamic}$, $P_{subthreshold}$ and $P_{gate-oxide}$ can be calculated from equations 1, 2 and 3, respectively. Thus, we conclude that T_{ox}, width, and length of a transistor play a role in determining the power dissipation of a circuit.

3.2 Delay Model

The delay of a device is approximately given as [10]:

$$Delay \propto \left(\frac{C_L V_{dd}}{\mu\left(\frac{\epsilon_{ox}}{T_{ox}}\right)\left(\frac{W_{eff}}{L_{eff}}\right)(V_{dd} - V_T)^{\alpha}}\right), \tag{5}$$

where μ is the electron surface mobility and α is the velocity saturation index. Since in a ULC we have both up and down converters, the average delay $Delay_{ULC}$ is defined as:

$$Delay_{ULC} = \left(\frac{Delay_{up} + Delay_{down}}{2}\right), \tag{6}$$

The delay of the level converter is calculated from the 50% level of the input swing to 50% level of the output swing.

3.3 Optimization Approach

In order to obtain a power and delay optimal circuit we propose a dual-T_{ox} (DOXCMOS) approach, where the power-hungry transistors are assigned thick oxides, to reduce the overall power consumption [7]. Power-delay optimization is done by considering variations in the transistor parameters, T_{ox} and W. These parameters are considered to be independent of each other. We have kept the length of the transistors fixed at the nominal process length in order to reduce the complexity of the optimization process.

4 Design of the proposed Level Converter

4.1 Base-line design

For level-up conversion, we employe a Cross Coupled Level Converter (CCLC). In this circuit, there are two cross-coupled PMOS transistors to form the circuit load. They act as a differential pair [4]. Thus, when the output at one side is pulled low, the opposite PMOS transistor will be turned on. The output on that side will be pulled high. Below the PMOS load, there are two NMOS transistors that are controlled by the input signal V_{in}. The NMOS transistors operate with a reduced overdrive $V_{ddl} - V_T$, compared to the PMOS devices. They must be larger to be able to overpower the positive feedback [8]. For level-down conversion, we have employed a differential input level converter. It has a differential input, which enables a stable operation for low voltage and high speed use [5]. The differential input also offers immunity against power supply bouncing.

The transistor level circuit design of the ULC is achieved by stitching the individual sub-circuits performing step-up conversion, step-down conversion, and blocking. To achieve programmability we have used multiplexers. For circuit optimization, instead of using a 4:1 multiplexer or three 2:1 multiplexers, we have achieved the functionality using two 2:1 multiplexers. The above sub-circuits, as well as the overall ULC circuit are thoroughly tested for functionality. Then, they are exhaustively characterized through parametric, load, and power analysis. The simulation waveforms are not included due to lack of space. The average power consumption of the baseline design with 32 transistors is $97.83\mu W$ (from SPICE simulations).

4.2 Area Optimal Design

In this design, a switch constructed using transmission gates is attached in front of the up-level converter and down-converter. The output of the level converters can be controlled by the switches. We obtained an area optimal design by using 2 output nodes instead of 1. Also the number of transistors is reduced to 24, eliminating 8 transistors from the baseline design as shown in figure 1. The functional simulation of the proposed ULC is shown in figure 2. This waveform verifies the truth table given in Table 1. The sequence of operations is block, step-down, and step-up.

4.3 Power-delay Optimal Design

To minimize power, we first identify the power-hungry transistors shown in figure 1 by measuring the power consumed by each transistor of the circuit. The power is estimated using model presented in Section 3. These transistors

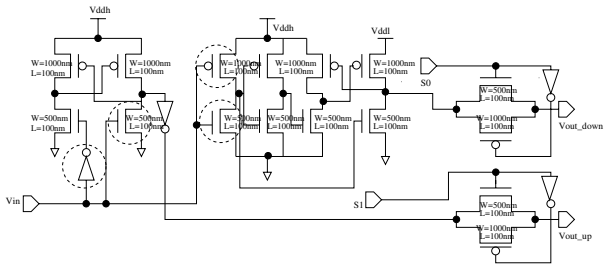

Figure 1. Area optimal ULC with 24 transistors; circled are power-hungry.

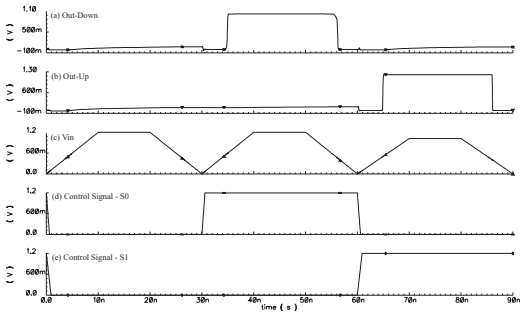

Figure 2. Functional simulation of the ULC.

were then subjected to the power-delay optimization technique. T_{ox} was varied between 10% to 200% of its nominal value, and the width of transistors is varied from $120nm$ to $1\mu m$. All transistors are assumed to have an effective length of $100nm$ corresponding to the nominal value of the $90nm$ process design kit used.

To optimize the power and delay, we varied the following parameters: (i) T_{ox} of the power-hungry NMOS transistors. (ii) T_{ox} of the power-hungry PMOS transistors. (iii) Width ($W_{NMOS_{down}}$) of the NMOS transistors of the down converter. (iv) Width ($W_{PMOS_{down}}$) of the PMOS transistors of the down converter. (v) Width ($W_{NMOS_{up}}$) of the NMOS transistors of the up converter. (vi) Width ($W_{PMOS_{up}}$) of the PMOS transistors of the up converter.

The optimized values of delay and power are obtained as: (i) Optimized Average Power (P_{ULC}) = $16.68\mu W$. (ii) Delay of up converter ($Delay_{up}$) = $80.35ps$. (iii) Delay of down converter ($Delay_{down}$) = $80.43ps$. (iv) Average delay ($Delay_{ULC}$) = $80.39ps$.

Table 1. Selection Signals

Select Signal		Type of Operation
0	0	Block Signal
0	1	Down Conversion
1	0	Up Conversion

The final values of the optimization parameters are: (i) T_{ox} of the power-hungry NMOS transistors = $2.667nm$ (14% increase from nominal). (ii) T_{ox} of the power-hungry PMOS transistors = $3.624nm$ (32% increase from nominal). (iii) Width ($W_{NMOS_{down}}$) of the NMOS transistors of the down converter = $120nm$. (iv) Width ($W_{PMOS_{down}}$) of the PMOS transistors of the down converter = $298.9nm$. (v) Width ($W_{NMOS_{up}}$) of the NMOS transistors of the up converter = $428.3nm$. (vi) Width ($W_{PMOS_{up}}$) of the PMOS transistors of the up converter = $220.1nm$.

We achieved 83% power savings compared to the baseline design and 60% delay savings compared to existing designs presented in the literature [4].

4.4 Characterization

We have characterized the ULC using three types of analysis: parametric, load and power analysis to check the robustness of the design.

The parametric analysis involves testing of the up-conversion and down-conversion of the ULC. For the up-conversion V_{in} was varied from $0.1V$ to $1.02V$ and for the down-conversion V_{in} was varied from $0.1V$ to $1.2V$ and the outputs were recorded. As in figure 3, a stable up-conversion happens for voltages as low as $0.65V$, and stable down-conversion happens for voltages greater than $0.6V$.

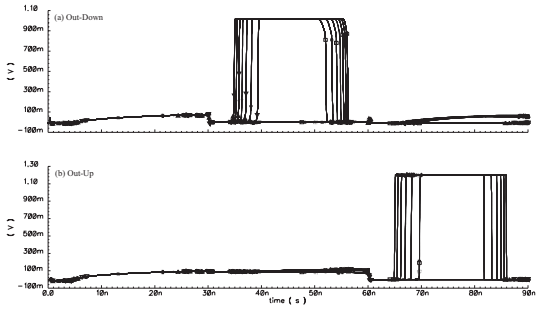

Figure 3. Parametric analysis with voltage.

Load analysis simulations of the complete ULC circuit were performed. The load capacitance is varied from $10fF$ to $200fF$ in steps of $10fF$. These values of load capacitance represent realistic loads [11] for a $90nm$ CMOS technology. The results, as shown in figure 4, demonstrate that the level converter produces a stable and predictable output voltage under varying load conditions.

The power analysis of the ULC is performed at a capacitive load of $10fF, 45fF$, and $90fF$. Table 2 shows the values obtained. It is evident that there is not significant difference in power consumption with varying loads.

5 Physical Design for $90nm$ Technology

The physical design of the ULC has been performed using a generic $90nm$ salicide "$1.2V$/$2.5V$ $1P$ $9M$" process

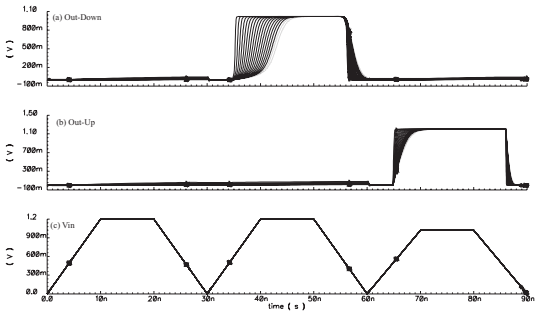

Figure 4. Performance of the ULC under varying output capacitive load ($10fF$ to $200fF$).

Table 2. Power Consumption

Capacitive Load (fF)	Average Power Consumption (μW)
10	17.23
45	19.89
90	23.27

design kit. In this layout it was necessary to supply both V_{ddh} and V_{ddl} to the cell. The two supply rails travel side-by-side to provide the two voltages. Such a layout does not comply with the conventional power routing, but is more robust [4]. The post-parasitic re-simulations matched with the simulations results of the schematic level simulation. Figure 5 shows the layout (physical design) of the area optimal ULC. To improve the functional yield and reliability of the physical design, we have followed Design For Manufacturability (DFM) methodologies. The use of additional vias has been made in the design wherever possible to make it more fault tolerant [3]. The metal lines have been spread out wherever possible to control the capacitance and crosstalk.

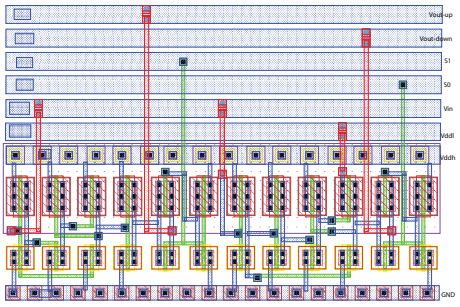

Figure 5. Physical design of the ULC.

6 Conclusions

In this paper, we have proposed a DOXCMOS approach along with transistor geometry variations to reduce the power-delay overhead of level converters. To the best of the authors' knowledge, this is the first ULC being subjected to such power saving techniques. The ULC is capable of performing three types of distinct operations on the input signal. This makes the ULC highly suitable for use in the context of dynamic power management techniques in circuits. The robustness of the level converter is tested using parametric, load and power analysis. It is observed that a stable output is obtained for voltages as low as $0.6V$ and capacitive loads varying from $10fF$ to $200fF$. The average power consumption of the level converter is $16.68\mu W$. A comparative perspective of selected related research is presented in Table 3. Each design uses different technology and performs different operations and hence fair comparison is not possible.

Table 3. Comparative Perspective

Works	Tech.	Power	Delay	Conversion
Ishihara [4]	$130nm$	–	$127ps$	Level-up & down
Yu [11]	$350nm$	$220.57\mu W$	–	Level-up
Sadeghi [9]	$100nm$	$10\mu W$	$1ns$	Level-up
This Work	$90nm$	$16.68\mu W$	$80.39ps$	Up/down/block

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