A Nano-CMOS Process Variation Induced Read Failure Tolerant SRAM Cell

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***Abstract*— In a nanoscale technology, memory bits are highly susceptible to process variation induced read/write failures. To address the above problem, in this paper a new memory cell is proposed which is highly stable against nanoscale process variations as well as power efficient. The effectiveness of the proposed cell is exhaustively evaluated through detailed Monte Carlo simulations. It is observed that the 16% variation in threshold voltage results in negligible effects on Static Noise Margin (SNM) during read operation. Experiments under different loading conditions indicate that there is reduction 2X (approximately) in power dissipation and 2X (approximately) in leakage.**

I. Introduction

The advent of nanoscale System on a Chip (SoC) allows higher integration density and performance which makes the design of low power embedded SRAMs increasingly important. Moreover, with increase in device density a larger fraction of the SoC area is devoted to SRAM, because on-chip memory offers high system performance in exchange of space and power. Furthermore, SRAM leakage can dominate the total leakage of the chip and becomes one of the major challenge in future SoC design. There are mainly three directions in which research have been devoted to reduce the power consumption of SRAM, by reduction in (a) charging capacitance, (b) operating voltage and (c) static current. In this paper, a new memory cell is proposed without precluding application of the traditional techniques for low power design. Therefore, all existing architectural techniques can be applied to our proposed cell to achieve further power optimization.

The SRAM cells are typically designed with minimum silicon area and are most sensitive to process variations and device mismatch [1]. Device mismatch due to process variation in length, width and gate-oxide thickness results in large deviation in threshold voltage [2] [3]. Several issues arise in SRAM due to process variation. The first and foremost is smallest viable size transistor is used to accommodate large number of transistors in SRAM design. Secondly, full logic levels are not achieved due to read timing constraints, and finally, the conflicting requirement under read and write operation such as memory cell must not change the state when accessed for reading but quickly change the state when accessed for writing [4].

In order to address these requirements, in this paper we propose a SRAM cell that would help in achieving the full logic level at the output and eliminate the read and write timing constraints. Also, it can tolerate the impacts of device mismatch due to process variation that will not persuade the stability and performance. The proposed design has two major differences compared to the traditional 6T SRAM design. Firstly, it does not require sense amplifier and pre-charge circuitry for pre-charging of bit and bit-bar lines prior to read and write operations. Secondly, transmission gates (TG) are used instead of access transistors. These differences make the proposed cell process variation induced read failure tolerant and low power. In summary, following are the major contributions:

- A 10T SRAM cell circuit and its physical layout are presented. The design is tested for different capacitive loads.
- The proposed design can tolerate process variations with small or no impact on stability, read static noise margin (SNM) and performance.
- The proposed design provides significant amount of power savings (including leakage) with some trade-off of performance, whereas, stability is remain untouched.

In order to obtain a comparative view, the traditional 6T SRAM and proposed 10T SRAM cells are designed using 90nm technology node. The process variation study conducted and presented in this paper is rely on the Monte Carlo simulation that could be performed in a reasonable time.

The rest of the paper is organized as follows. The problems and limitations that can arise due to process variations in 6T SRAM is presented in Section II. In Section III, a new 10T SRAM cell is presented and its operation is illustrated. Power and stability analysis of the 10T SRAM is presented in Section IV. The paper is concluded in Section V.

II. 6T SRAM Limitations Under Process Variations

In this section we will explore how the process variation influences the stability performance and power of a 6T SRAM cell [5] [6].

A. Stability

The stability of 6T SRAM cell is analyzed through Static Noise Margin (SNM) [7] [8]. The most common way of representing the SNM graphically for a bit cell in holding and reading state is shown in Fig. 1. The *Voltage Transfer Characteristics* (VTC) of inverter $M_{1,2}$ and the inverse VTC of inverter $M_{3,4}$ for 6T SRAM cell are shown. The resulting

two lobed curves is used to determine the SNM. In order to recognize the impacts on stability under process variations we use SNM obtained from VTC [9]. The cell's VTC in hold and during the read operation is shown in Fig. 1(a) and (b), respectively. There are three intersection points of the hold state VTC as shown in Fig 1(a): (V_Q, V_{QB}) = $(1.2, 0)V$, $(0, 1.2)V$ and $(0.482, 0.482)V$. The stable (steady) states are corresponding to intersection points $(1.2, 0)V$ and $(0, 1.2)V$, because at these points the cross coupled inverters feedback loop gain is less than unity, whereas state at $(0.482, 0.482)V$ is unstable because the cross coupled inverters feedback loop gain exceeds unity. The VTC in read operation as shown in Fig. 1(b) illustrates the stable (steady) state which is corresponding to intersection points $(1.2, 0.287)V$ and $(0.287, 1.2)V$. Thus, during read operation V_{QB} raised from $0V$ to $0.287V$ which reduces the SNM, and can be observed in Fig 1(b). *It is clear from the above discussion that the cell's stability degrades during read operation.*

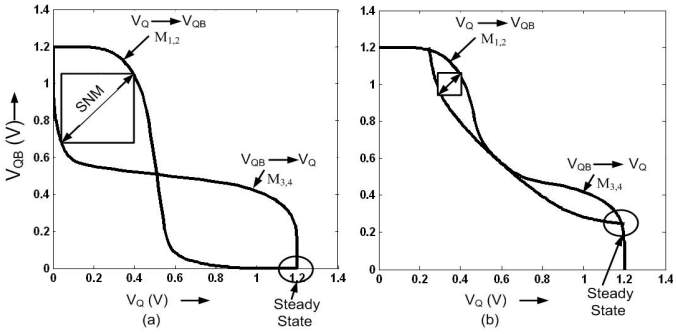

Fig. 1. Traditional 6T SRAM cell's VTC and SNM under: (a) read state and (b) hold state.

B. Power

As larger fraction of SoC area is devoted to SRAM because of this reason, SRAM leakage can dominate the total system power. In a 6T SRAM cell, there are three strong leakage paths because there is only one OFF transistor along the path and one weak leakage path because there are three stacked transistors along the path. The traditional 6T SRAM consumes substantial amount of power (including leakage) to preserve the information. It is also observed that the power consumption becomes *worse and expected to be more than 20 times due to process variation* [10].

III. The Proposed 10T SRAM cell

The proposed 10T SRAM cell is comprises of 10 transistors as shown in Fig. 2. We refer inverter $M_{1,2}$ composed of transistors M1 and M2 and inverter $M_{3,4}$ comprising of transistors M3 and M4. These inverters $M_{1,2}$ and $M_{3,4}$ are connected back to back in a closed loop fashion in order to store the 1-bit information. We use three transmission gates TR, TW, and TH for read, write and hold states, respectively, instead of access transistors used in traditional 6T SRAM design. These transmission gates are formed by placing an NMOS transistor in parallel with a PMOS transistor. The use of transmission gate is to care fully input and output the data to/from the cell node Q at full logic level. The cost of this feature is an extra transistor but it can be a minimum feature size transistor that will provide full swing during write and read operation. This feature of the proposed design eliminates the use of sense amplifier (S.A.) and pre-charging circuitry for pre-charging of bit and bit-bar lines prior to read and write operations.

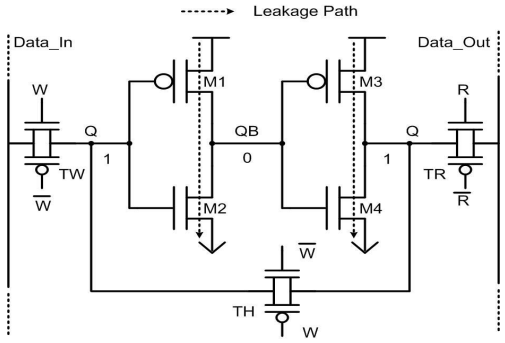

Fig. 2. Proposed 10T SRAM cell design along with the leakage path.

The sense amplifier and its associated circuitry such as pre-charge circuitry in traditional SRAM design involves carefully matched transistors designed to minimize impacts of process variation in threshold voltage, leakage etc. Thus, eliminating the use of sensitive circuits helps to achieve the low power memory and improve the stability of proposed cell. This is mainly because sense amplifier and its associated circuitry are not required in the proposed design. The detailed analysis of power and stability under process variation is discussed in section IV. Also the use of separate transmission gates, which provides another major advantage that it preclude the conflicting requirements of write and read which exists in traditional 6T SRAM.

The physical design of the proposed 10T SRAM cell is shown in Fig. 3. Every effort is made to minimize area of the memory cell and symmetry which allow the core array to be generated by simply "tiling" the cells together vertically and horizontally. Moreover, the PMOS and NMOS transistors are placed symmetrically such that overall interconnections become less complex. Three levels of metal and one layer of poly are used for the layout. Data_In, Data_out, read (R and R′) and write (W and W′) lines are routed in Metal2 vertically. Metal3 is used for gate connections of the hold transmission gate (TH). The physical design is verified through DRC (design rule check), LVS (layout versus schematic), and RCX (parasitic extraction).

A. Write Operation

The operation and working of this 10T SRAM cell is described in this section. The write operation starts with write control signal (W) which control transmission gate, TW. For successful writing another transmission gate, TH is used. The NMOS and PMOS transistors of this transmission gate TH

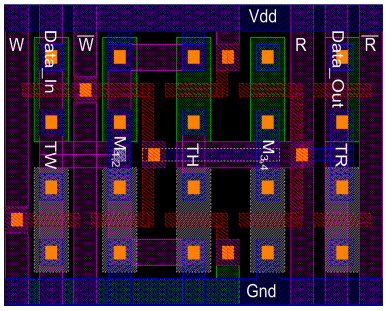

Fig. 3. Proposed 10T SRAM cell layout.

are connected to control signal W′ and W, respectively which keeps open the feedback loop of inverters $M_{1,2}$ and $M_{3,4}$ during the write operation only. When the write signal W goes high, the transmission gate TW connects Data_In line to the node Q of the memory cell. As the write signal W is asserted high transmission gate TW forces the node Q (the stored information) to the same level of the Data_In line. Once, node Q of the cell changes its state during write operation and write signal W asserted low, the transmission gate TH provides closed loop to both the inverters to store the written 1-bit information. The availability of full logic level (1 or 0) at the node Q of the memory cell during write (1 or 0) operation can be observed in Fig. 4(a).

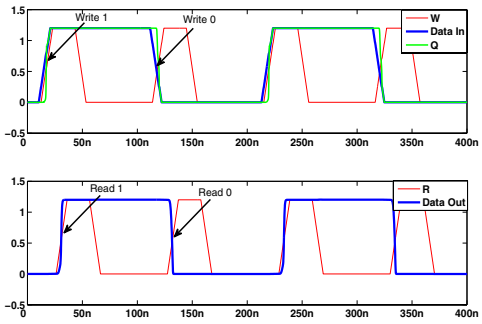

Fig. 4. 10T SRAM cell waveforms for (a) write (1 or 0) and read (1 or 0) operation.

B. Read Operation

The read operation of the 10T SRAM cell begins with the read control signal (R and R′), control signal R is connected to gate of NMOS transistor of transmission gate TR and complement of read control signal R′ is connected to the gate of PMOS transistor of transmission gate TR. When the read signal goes high, this turned on the transmission gate TR that provides the path between output data line(Data_Out) and memory cell node Q. As the read signal R is asserted high transmission gate TR forces the Data_Out line to the same level of the node Q (the stored information). This way, the content of the cell node Q is transferred to the Data_Out line. Full logic level (1 or 0) is obtained at the output as shown in Fig. 4(b) without sense amplifier.

C. Hold State

Under hold state, when there is no read and write control signals or in other words the both read and write control signals are active low (R=0 and W=0), which disconnect the cell node Q from both the Data_In and Data_Out lines. In this state the transmission gate, TH, provide back to back feedback loop to both the inverters $M_{1,2}$ and $M_{3,4}$ that holds the last stored information. Fig. 4(a) and (b) shows the HSPICE simulation waveforms of the proposed 10T SRAM cell for write (0 or 1) and read (0 or 1) operations, respectively. One can observe that the node voltage (Q) and output voltage are available at full logic level (1 or 0) without use of sense amplifier.

IV. Analysis of the Proposed 10T SRAM Cell

In this section, we compare the stability and power metrics of the proposed 10T SRAM cell with traditional 6T SRAM cell.

A. Stability

The stability of 10T SRAM cell is analyzed with SNM butterfly curves obtained form the VTC of inverter $M_{1,2}$ from Fig. 2 and the inverse VTC of inverter $M_{3,4}$. The cell's VTC and SNM in hold state and during the read operation is shown in Fig. 5(a) and (b). There are three intersection points of the hold state VTC as shown in Fig. 5(a): (V_Q,V_{QB}) = $(1.2, 0)V$, $(0, 1.2)V$ and $(0.482, 0.482)V$. The stable (steady) states are corresponding to intersection points $(1.2, 0)V$ and $(0, 1.2)V$, whereas the cell's state at corresponding to $(0.482, 0.482)V$ is unstable. It is observed that the SNM of the 10T SRAM cell in hold state is equivalent to the 6T SRAM cell SNM in hold state [see Fig1(a)]. Thus, the hold stability of the proposed cell remains untouched.

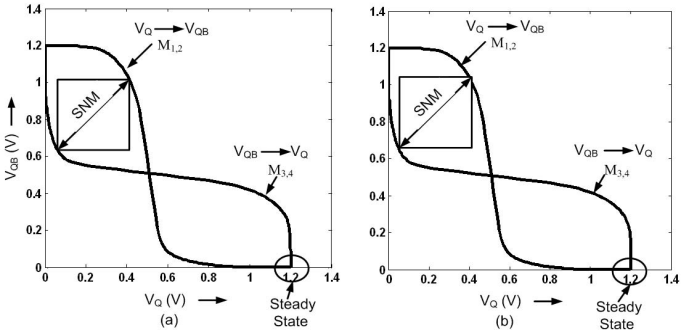

Fig. 5. 10T SRAM cell's VTC and SNM under : a) hold state b) read operation.

The VTC and SNM in read operation of the 10T SRAM cell is shown in Fig 5(b) which illustrates the stable (steady) states of the cell that are corresponding to intersection points (V_Q,V_{QB}) = $(1.2, 0)V$ and $(0, 1.2)V$ because at these points the cross coupled inverters feedback loop gain is less than unity. Whereas, under read operation of the 6T SRAM cell, stable (steady) state intersection points shifts vertically and cause to raise in V_{QB} (initially V_{QB}=0) which degrades the

stability and SNM of the cell. We can easily figure out that the SNM of the proposed cell much higher than that of traditional cell. Also, there is no vertical shifts in intersection point that leads to increase in V_{QB} (initially V_{QB}=0).

We have exhaustively evaluated the stability and SNM through detailed 4000 Monte Carlo simulations to ensure there is no process variation induced read failure. The application of 16% [8] threshold voltage variation which is strongly related to the device geometry (length, width and oxide thickness etc.) and doping profile did not persuading the stability and SNM of the proposed cell [see Fig. 6(a) and (b)]. The stable (steady) state intersection points under process variation in threshold voltage causes vertical shift in intersection points which results in poor SNM and highly susceptible to read failure of 6T SRAM cell as shown in Fig. 6(b). However, 10T SRAM cell's performance under process variation in threshold voltage has negligible effects on SNM and stability compared to 6T SRAM cell as shown in Fig. 6(a). Thus the proposed *10T SRAM cell can tolerate process variation induced read failure*.

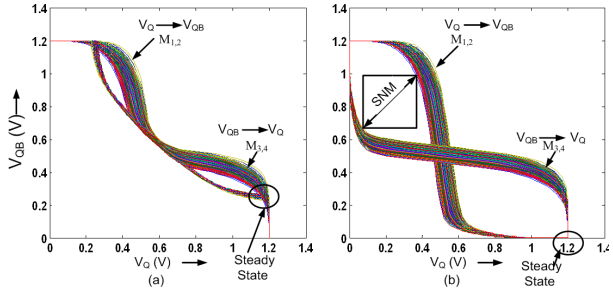

Fig. 6. Monte Carlo simulated VTC and SNM with 16% [8] threshold voltage variation: (a) 6T SRAM cell and (b) 10T SRAM cell.

B. Power

In the proposed design power dissipation and leakage is reduced due to the appropriate use of transmission gates. We performed the power analysis of the proposed 10T SRAM and also the traditional 6T SRAM. The results are presented in Table I along with the leakage and access time. For power analysis three different loading conditions are considered [11]. As evident from the table, the power dissipation for the proposed 10T SRAM cell is always 2X (approximately) lesser than the 6T SRAM for any loading conditions. Also, the leakage current for the proposed 10T SRAM cell is always 2X (approximately) lesser than the 6T SRAM for any loading conditions. However, the access time for the proposed SRAM is longer than the traditional cell, which suggests power-performance trade-offs.

V. Conclusions

In this paper, a new 10T SRAM cell is presented that offer higher Static Noise Margin (SNM) and read failure stability. Experimental results reveal that the proposed cell is highly resistance against the process variation induced failures with negligible effects on the stability and SNM compared to conventional 6T SRAM cell. Total power dissipation (including leakage) in the cell is about 2X lesser than the conventional cell. The process variation study conducted through detailed Monte Carlo simulations proved that the proposed 10 SRAM cell is tolerant to process variation impacts. The cell performs the read/write operations and provides full logic level without use of sense amplifier under different loading conditions. In future we want to study the performance of the proposed cell in the context of large memory array.

TABLE I

Comparison between 6T and 10T SRAM cell with their power leakage and access time.

Capacitance (fF)	Cell	Power (μW)	Leakage (nA)	Access Time (ns)
250	6T	21.27	4.31	0.542
	10T	11.53	2.30	1.43
500	6T	24.91	4.27	1.94
	10T	12.24	2.33	3.47
750	6T	28.35	4.22	2.96
	10T	12.93	2.36	4.97
1000	6T	31.60	4.16	3.83
	10T	13.58	2.39	6.19

VI. Acknowledgement

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