A Process and Supply Variation Tolerant Nano-CMOS Low Voltage, High Speed, A/D Converter for System-on-Chip

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ABSTRACT

This paper presents a process variation tolerant, SoC ready, $1GS/s$, 6 bit flash analog-to-digital converter (ADC) suitable for integration into nanoscale digital CMOS technologies. The physical design is carried out with a generic $90nm$ Salicide $1.2V/2.5V$ 1 Poly 9 Metal process design kit using Design for Manufacturability (DFM) methodologies. Post-layout simulation results at nominal supply and threshold voltages are presented. The parasitic-extracted physical design of the ADC has been simulated for a supply voltage variation of $\pm 10\%$, and threshold voltage mismatch of $\pm 5\%$. The results show maximum variations of 10.5% and 5.7% in the INL and DNL respectively, with nominal $INL = 0.344LSB$ and nominal $DNL = 0.459LSB$, at a supply voltage of $1.2V$. The ADC consumes a peak power of $5.794mW$ and an average power of $3.875mW$. The comparators used in the ADC have been designed using the threshold inverting technique.

Categories and Subject Descriptors

B.7.1 [**Integrated Circuits**]: Types and Design Styles—VLSI (very large scale integration)

General Terms

Design

Keywords

Analog-to-Digital Converter, Flash ADC, TI Comparator, Low Voltage, High Speed, Process Variation, Nano-CMOS

1. INTRODUCTION AND MOTIVATION

Nowadays, a large number of SoCs are manufactured in the $90nm$ process node, and the ramp up for $65nm$ design starts is becoming more aggressive than expected. $45nm$ process design is following close behind, with early versions of design rules and process parameters already available [3, 2]. IP core providers are faced with the challenge of meeting analog performance in a technology that has been targeted for densely packed digital logic. The IP core should also be able to incorporate new circuit design techniques that accommodate lower supply voltages necessary for portable systems. Systems that once worked at $3.3V$ or $2.5V$ now need to work at $1.8V$ or lower, without any loss in performance. The minimum channel length shortening has resulted in the reduction of power supply voltage to the $1V - 0.7V$ range. The system-on-chip trend forces analog circuits to be integrated with digital circuits. To follow both the scaling of the minimum channel length and the system-on-chip trends, analog-to-digital converters (ADCs) need to be operated at low voltages, especially in portable devices. However, the minimum supply voltage for analog circuits predicted in the road map [3] does not follow the digital supply voltage reduction. Analog supply voltages between $1.8V$ and $2.5V$ are still being used. Hence, it is a great challenge to design a low supply voltage operating ADC because of the relatively high threshold voltage of short channel length transistors. Another important consideration for a SoC is that the analog/mixed signal circuits should be designed using a standard CMOS digital process. There are no process options such as deep N-WELL or on-chip inductors or varactors.

The ADC is an essential true mixed-signal circuit in SoC products because it bridges the gap between the analog circuits and the digital logic world. High-speed, low-resolution flash ADCs are required for the integration of radio frequency (RF) analog circuit components for complete SoC products. ADC circuit designs often contain matched transistors [14]. The threshold voltage of a MOS transistor is the gate voltage required to induce a channel for current flow through the transistor. Matched CMOS transistors are designed to be necessarily identical. During fabrication, the threshold voltage of a CMOS transistor is engineered during processing to a desired voltage. In a typical MOSFET process, ion-implanted charges are employed to shift the threshold voltage. This processing step, called the threshold voltage adjustment implant, is random in nature, consisting of varying energy levels of the implanted ions and subsequent temperature ramp step to diffuse the ions. The random nature of this process results in the random fluctuations in threshold voltage as a function of transistor area. Additionally, random variations in the lithography result in small geometric inaccuracies. The variation of the effective threshold voltage (V_t) increases as the transistor areas decrease. In CMOS analog circuits it is the variation of the threshold voltages between two transistors rather than their absolute voltage values that is of interest for the majority of applications. Hence in this paper we have analyzed the effect of threshold voltage mismatch on the ADC performance. Also, the power supply voltage variations in the ADC design have been accounted for, to verify its system-on-chip capability.

In summary, the demand for emerging application-specific, nano-scale mixed-signal SoCs which need process (threshold voltage

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mismatch) and power supply voltage variation tolerant ADC interfacing circuitry and development of mature nano-CMOS processing technology has motivated this research. The rest of the paper is organized as follows. Section 2 highlights the design issues and our contributions. Related prior research is summarized in Section 3. Discussion about logical transistor level design in presented in Section 4. Physical design and parasitic re-simulation is presented in section 5. Section 6 discusses the effect of process variation on the circuit attributes. Conclusions and future research directions are in Section 7.

2. CONTRIBUTIONS OF THIS PAPER, DESIGN ISSUES AND SOLUTIONS

The main contribution of this paper is the logical and physical design of a process and supply variation tolerant ADC using $90nm$ nano-CMOS technology, suitable for SoC integration. A low supply voltage, $V_{dd} = 1.2V$, is used. The physical design has been carried out up to parasitic extraction, and the post-layout simulation results are presented. Power analysis results, with a nominal $100fF$ load reveal that the proposed ADC consumes minimal power.

As V_{dd} decreases, the power dissipation decreases as it is proportional to V_{dd}^2. However, lower V_{dd} put a constraint on the choice of 63 voltage quantization levels for the 6 bit ADC that we present in this paper. An LSB value of $1mV$ has been chosen for this purpose. More details are given in section 4. The INL of initial straightforward version of the physical design was at an unacceptable error level ($INL > 1LSB$). Such INL degradation is due to IR drop in the power supply and ground lines. The power and ground buses have been populated with a large number of contacts to reduce the IR drop and reduce INL to $0.344LSB$. In addition, the power and ground buses have been widened, to reduce electromigration risk. To ensure a low-resistance path between the substrate or N-WELL surrounding the circuit and its nearest ground and V_{dd} connections, generous use of substrate contacts and N-WELL ties has been made.

Table 1: Comparative perspective of existing 6-bit flash ADCs

Works	Tech. (nm)	DNL (LSB)	INL (LSB)	V_{dd} (V)	Power (mW)	Rate GS/s
Geelen [9]	350	< 0.7	< 0.7	3.3	300	1.1
Uyttenhove [19]	350	–	–	3.3	–	1
Donovan [6]	250	–	–	2.2	150	0.4
Tseng [8]	250	< 0.1	< 0.4	2.5	35	0.3
Yoo [11]	250	–	–	2.5	66.87	1
Scholtens [16]	180	–	0.42	1.95	328	1.6
Sandner [7]	130	< 0.4	< 0.6	1.5	160	0.6
This Work	90	0.459	0.344	1.2	3.875	1

3. RELATED PRIOR RESEARCH WORKS

ADC design is a bottleneck in SoC design. More sophisticated circuitry in terms of speed, area and noise immunity is needed. Most of the literature available on ADCs focusses on comparator offset cancelation [6], elimination of power-hungry resistive ladders using capacitive interpolation [7] or simplifying the comparator design [8]. In [16], an average termination circuit has been proposed to reduce power consumption. The problem of metastability at high sampling speeds has been addressed in [19]. Little attention has been given to the SoC integration problem faced by ADCs today. In [20], the authors propose a solution using the threshold inverting technique. The authors in [10], propose an ADC design at $45nm$, but it is not supported with the physical design.

Table 1 provides a comparative perspective of our proposed ADC with others presented in the literature. Only 6-bit, flash type architecture ADCs have been chosen for fair comparison. It can be observed from the Table that our ADC is suitable for nano-scale SoCs, has superior INL and DNL performance and is a low-voltage, low-power, high-speed design.

4. TRANSISTOR LEVEL DESIGN OF THE PROPOSED ADC

Figure 1 shows a block diagram, high level representation of the 6-bit ADC. A flash architecture is chosen because of its inherent speed. The input to the ADC is analog and the output is in the form of digital codes. An n-bit ADC requires $2^n - 1$ comparators. The nominal switching point of each comparator is determined by appropriately sizing the transistors in the comparator. The comparator outputs form a thermometer code. The position of the meniscus (the 1-0 transition) represents the analog input and is determined by the thermometer decode circuit. The thermometer decoder generates a "1 of n" code which is converted to binary using the NOR ROM.

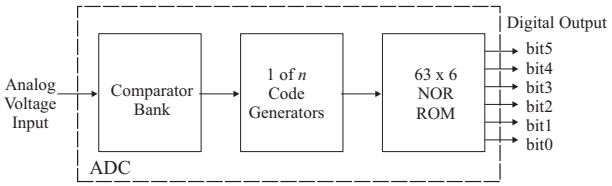

Figure 1: Block diagram of the flash ADC

4.1 Comparator Design

The comparators in our flash ADC have been designed using the threshold inverter (TI) technique [11, 12]. The advantages of the threshold inverting (TI) comparator are high speed and simplicity [12]. This eliminates the need for inherently complex high-gain differential input voltage comparators and additional resistor ladder circuit [17].

The TI comparator sets its switching threshold voltage $V_{\text{switching}}$ internally as the built-in reference voltage, based on its transistor sizes. In the conventional flash ADC, all the comparators are identical in size. The TI based ADC has individual comparators in different sizes. For an n-bit ADC, we require $2^n - 1$ different comparators, each having a different $V_{\text{switching}}$ value. Hence, a total of 63 comparators for a 6-bit ADC, each having different size of transistors is required. The switching voltage is generally calculated using the following expression [15]:

$$V_{\text{switching}} = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}\,(V_{dd} - |V_{tp}|) + V_{tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}, \qquad (1)$$

where W_p = PMOS width, W_n = NMOS width, V_{dd} = supply voltage, V_{tn} = NMOS threshold voltage, V_{tp} = PMOS threshold voltage, μ_n = electron mobility, and μ_p = hole mobility, assuming that the PMOS length (L_p) and NMOS length (L_n) are equal. However, short-channel devices do not follow the square-law model used in deriving equation 1. A more suitable expression to determine the

$V_{\text{switching}}$ for short-channel devices is given by [4]:

$$V_{\text{switching}} = V_{dd}\frac{R_n}{R_n + R_p}, \quad (2)$$

where R_n and R_p are the effective switching resistances for short-channel NMOS and PMOS transistors, respectively. As the switching resistance of a transistor is dependent on the width (W) of the transistor, we have varied the width of the PMOS (W_p) transistor in order to achieve the 63 different switching voltages required for the comparators. Another reason for doing this is that the channel length (L) of the transistor more effectively controls the performance; the frequency is proportional to $1/L^2$.

The sizes of NMOS transistors in the comparator were kept constant at $240nm/120nm$ (W_n/L_n). For determining the sizes of PMOS transistors, we used a DC parametric sweep using an analog simulator, where the input DC voltage was varied from 0 to $1.2V$ in steps of $1mV$. During this simulation, L_p was kept at $120nm$ while W_p was varied from $240nm$ (W_p=W_n) to $448nm$ (in steps of $1nm$) in order to obtain 63 linear quantization voltage levels. The TI comparator consists of four cascaded inverters, as shown in figure 2. Inverter 1 and 2 form the baseline comparator, while Inverter 3 and 4 provide increased gain and sharper switching. A good input voltage range was predicted to be:

$$\text{Input Voltage Range} = V_{dd} - (V_{tn} + |V_{tp}|). \quad (3)$$

We chose the input voltage range to vary from $493mV$ to $557mV$. The LSB value V_{LSB} is calculated as:

$$V_{LSB} = \left(\frac{\text{Input Voltage Range}}{2^n}\right). \quad (4)$$

For our design, V_{LSB} of $1mV$ is selected.

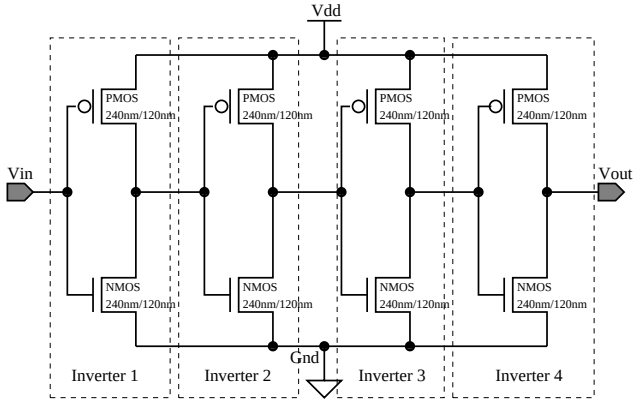

Figure 2: The threshold inverter (TI) comparator. In this figure W_p/L_p = W_n/L_n, which is the starting point for quantization.

4.2 1 of n code generator Design

Conversion of the thermometer code from the comparator output to binary code through the encoder is a crucial part of a flash ADC. The "1 of n" code generator consists of AND gates as combinations of an inverter followed by a NAND gate. The output from each of the AND gates is fed to the input of the NOR ROM. One of the two inputs to the AND gate is fed from the TI comparator output [5]. The other input to the AND gate is the inverted output from the next level comparator as shown in figure 3.

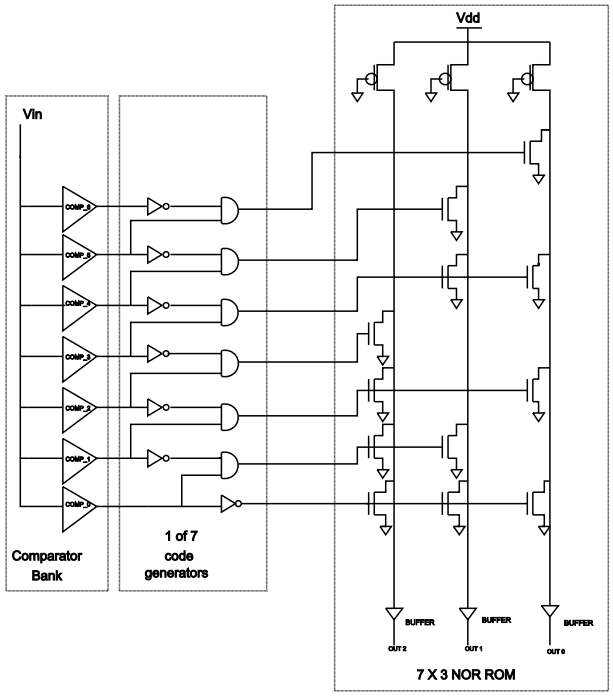

Figure 3: Complete circuit diagram for a 3-bit flash ADC shown for brevity. A similar 6-bit structure has been implemented in this paper.

4.3 NOR ROM Design

The purpose of the NOR ROM is to map the n-bit address input onto arbitrary values of m-bit data output. It consists of a grid of word lines (the address input) and bit lines (the data output), selectively joined together with transistor switches. It can represent an arbitrary look-up table with a regular physical layout. Here we have used the NOR ROM to convert the "1 of n" code into a binary code. As we have 63 word lines and 6 bit lines, we designed a 63×6 NOR ROM. The NOR ROM consists of PMOS pull-up and NMOS pull-down devices. The PMOS and NMOS sizes have been taken as $135nm/180nm$ and $180nm/180nm$, respectively. We have taken $W_p < W_n$ to obtain a good voltage swing. The logic is that the pull-up device (PMOS) should be narrow enough so that the pull-down devices (NMOS) can still pull down the output safely [15]. Finally, buffers are applied at the outputs to obtain symmetrical waveforms, with equalized rise and fall times. The buffer consists of two cascaded inverters having NMOS size of $240nm/120nm$ and PMOS size of $480nm/120nm$.

5. PHYSICAL DESIGN AND CHARACTERIZATION OF ADC

5.1 Physical Design

The physical design of the ADC has been carried out using a generic $90nm$ Salicide "1.2V/2.5V 1 Poly 9 Metal" process design kit. A digital CMOS process has been used for the physical design, demonstrating the SoC readiness of the ADC. The three major blocks of the flash ADC, namely the comparator bank, the "1 of n " code generator and the NOR ROM have been laid out column-wise. The overall layout is shown in figure 4. The post-layout simulation results are presented in subsequent sections. Power and ground routing is comprised of wide vertical bars, as can be seen

from the layout. This guarantees that electromigration risk is minimal and that IR drops are small. The small IR drop was also ensured through the generous use of contacts to the power and ground buses.

5.2 Post-layout Simulation Results

Figure 5 shows the functional results of the ADC, obtained from the post-layout simulation. The ADC is subjected to a transient analysis, where a linearly varying ramp covering the full scale range of the ADC, is given as input. Output digital codes from 0 to 63 are obtained correctly, with no missing codes. Also from this figure, we can observe a maximum sampling speed of $1GS/s$. The least significant bit (out 0) toggles the fastest, as expected. Successive bits toggle at half the frequency of the previous one. All 64 codes of the ADC are covered as the input ramp traverses the full-scale range.

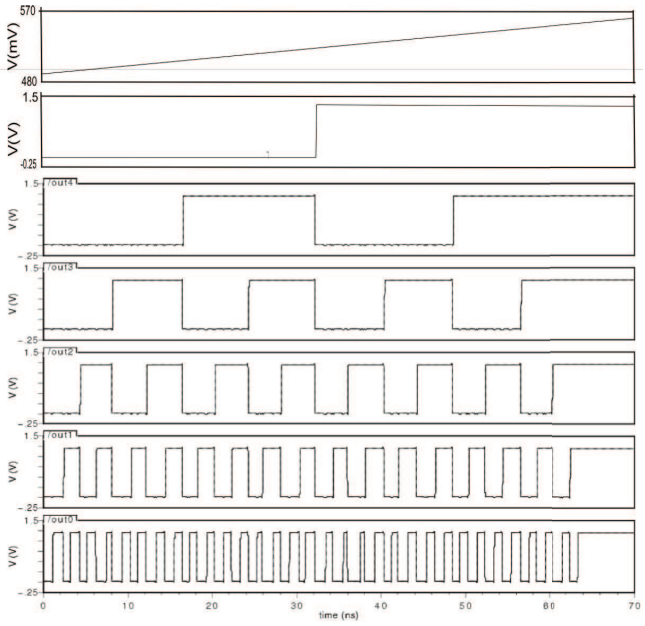

Figure 5: Simulation result of the 6 bit ADC operating at $1GS/s$.

5.3 Characterization

The ADC has been characterized for static performance. The Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) tests have been performed with nominal supply and threshold voltages to confirm satisfactory results before process and supply variation are introduced. Also, a power consumption analysis of the designed circuit has been performed.

5.3.1 Static Characterization

The histogram test is commonly used to characterize the linearity features of an ADC [1]. The number of occurrences of each code at the output of the converter are obtained. The proposed 6-bit ADC's INL and DNL have been measured using the histogram method. A mixed signal simulation environment is setup for this, where INL and DNL calculating blocks are Verilog-A modules. The Verilog-A block generates a voltage 'vout', which is sequentially set to 4096 equally spaced voltages between 'vstart' and 'vend', which is the input voltage range for ADC conversion. At each different value of 'vout' a clock pulse is generated causing the ADC to convert this 'vout' value. The resultant code of each conversion is stored. When all the conversions have been performed, the INL and DNL are calculated from the recorded data as follows:

$$INL[i] = width[i] + INL[i-1] - 1, \tag{5}$$

$$DNL[i] = width[i] - 1, \tag{6}$$

$$width[i] = \frac{1.0 * bucket[i]}{hits * (NUM_{CODES} - 2)}, \tag{7}$$

where $bucket$ holds the number of code hits for each code and $width$ holds the code width calculations. The total hits between codes 1 and 62 is denoted as $hits$. NUM_{CODES} is the number of codes, 64 for a 6-bit ADC. The maximum INL is recorded as $0.344LSB$ and the maximum DNL is recorded as $0.459LSB$. Figure 6 and figure 7 show the INL and DNL plots, respectively. Low distortion requires an ADC with low INL. Also a $DNL < 1LSB$ ensures a monotonic transfer function for the ADC.

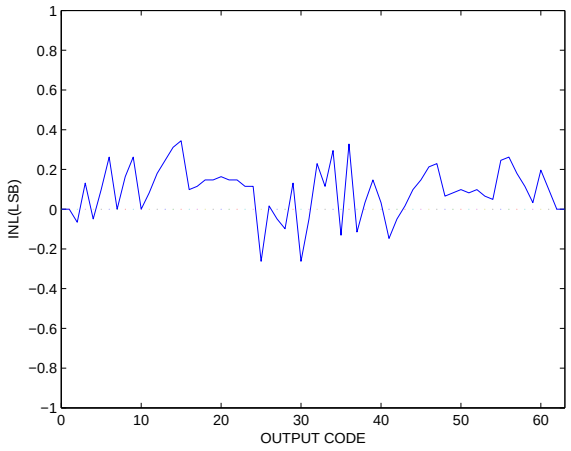

Figure 6: Integral Non-Linearity (INL) plot of the ADC.

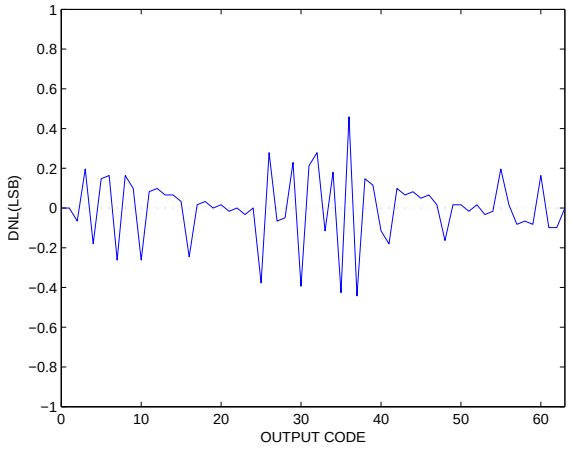

Figure 7: Differential Non-Linearity (DNL) plot of the ADC.

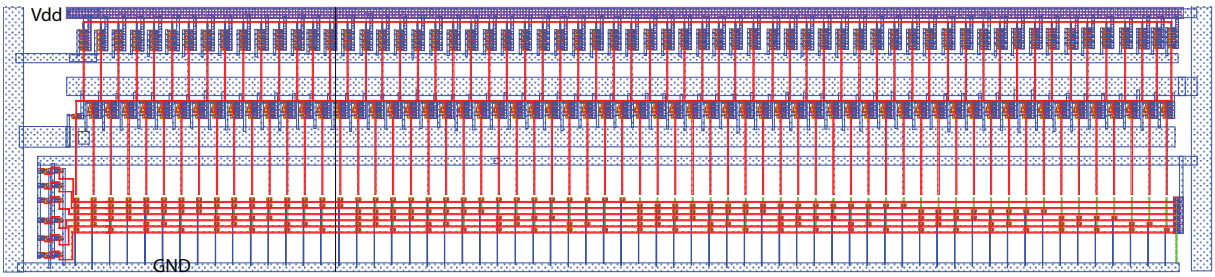

Figure 4: Complete layout of the $90nm$ ADC.

5.3.2 *Power Analysis*

The power analysis of the ADC was performed with a capacitive load of $100fF$, which is a reasonable load for a $90nm$ CMOS technology [13]. It was observed to consume a peak power of $5.794mW$ and an average power of $3.875mW$, which satisfies the lower bound on ADC power consumption [18]. The componentwise power consumption is shown in Table 2. It is evident that the comparator bank consumes maximum power. A power-saving scheme could be to turn-off the unused TI comparators. The instantaneous power plot of the ADC is shown in figure 8. The plot has a parabolic nature with peak power at the middle of the conversion process. This is because most of the comparators are turned on at the middle voltage, (Input Voltage Range)/2. The summary of the measured performance of the ADC is shown in Table 3.

Table 2: Componentwise power consumption of ADC

Component	Average Power (mW)
Comparator Bank	3.68125 (95%)
1 of n code generators	0.03875 (1%)
NOR ROM	0.155 (4%)
Total	3.875

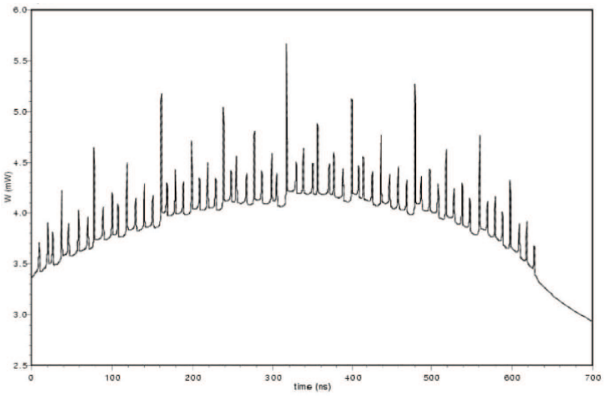

Figure 8: Instantaneous power plot of ADC with a load capacitance of $100fF$.

6. PROCESS AND SUPPLY VARIATION CHARACTERIZATION

The effect of process and supply variation is one of the most critical issues for an ADC. While the process variation is a static problem, the supply variation is a dynamic problem. The ADC has been tested for the effects of threshold voltage mismatch and supply voltage variation on the INL and DNL. It is assumed that $V_{\text{switching}}$ is not sensitive to variation in the length of the transistors (L_p, L_n), because the effective switching resistances of transistors are independent of their lengths (equation 2). Hence the effect due to device mismatch can be modeled to some degree by the effect of threshold voltage mismatch. The results reveal that while the INL and DNL values are within control, there is a shift observed in the input voltage range. Consequently, the V_{LSB} value also changes. To overcome this shift, one may add a programmable pre-amplifier to the input signal of the ADC, thereby adjusting the signal offset and amplitude [11].

Table 3: ADC performance with nominal supply and threshold voltages

Parameter	Value
Technology	$90nm$ CMOS $1P\ 9M$
Resolution	6 bit
Supply Voltage (V_{dd})	$1.2V$
Sampling Rate	$1GS/s$
INL	$0.344LSB$
DNL	$0.459LSB$
Peak Power	$5.794mW@1.2V$
Average Power	$3.875mW@1.2V$
Input Voltage Range	$493mV$ to $557mV$
V_{LSB}	$1mV$

A corner-based process variation methodology has been used for testing the ADC. The methodology is shown in figure 9. For process variation, the NMOS threshold voltage (V_{tn}) and the PMOS threshold voltage (V_{tp}) were varied by $\pm 5\%$ from their nominal values specified in the PDK, and the INL, DNL and input voltage range values were recorded. The results have been summarized in Table 4. The INL shows a variation from $+0.2\%$ to $+10.5\%$ and the DNL shows a variation from $+2.2\%$ to $+5.7\%$.

For the supply voltage variation, the nominal supply voltage ($1.2V$) has been varied by $\pm 10\%$, and the INL and DNL and input voltage range values have been recorded, as shown in Table 5. The INL shows a variation of -1% to $+4\%$ and the DNL shows a variation of $+1.8\%$ to $+4.8\%$. It can be observed that the INL and DNL values are satisfactory ($INL, DNL < 0.5LSB$). Hence we conclude that the ADC is process and supply variation tolerant.

7. CONCLUSION AND FUTURE WORKS

In this paper the design of a process and supply variation aware low voltage, high speed flash ADC has been presented. The logical and physical design of the ADC was performed using a digital CMOS process, demonstrating its SoC readiness. The comparators

Table 4: Effects of Supply voltage Variation

V_{dd} (V)	Input Voltage Range (mV)	V_{LSB} (mV)	INL (LSB)	DNL (LSB)
$1.08V(-10\%)$	448-500	0.8125	0.359	0.467
$1.2V$(nominal)	493-557	1	0.344	0.459
$1.32V(+10\%)$	537-614	1.203	0.339	0.481

Table 5: Effects of Process Variation

PMOS threshold voltage, NMOS threshold voltage	Input Voltage Range (mV)	V_{LSB} (mV)	INL (LSB)	DNL (LSB)
V_{tp}(nominal),V_{tn}(nominal)	493-557	1	0.344	0.459
$V_{tp}(+5\%)$,$V_{tn}(+5\%)$	495-557	0.96875	0.333	0.46
$V_{tp}(-5\%)$,$V_{tn}(-5\%)$	491-556	1.015625	0.345	0.477
$V_{tp}(-5\%)$,$V_{tn}(+5\%)$	500-564	1	0.36	0.485
$V_{tp}(+5\%)$,$V_{tn}(-5\%)$	501-566	1.015625	0.38	0.479

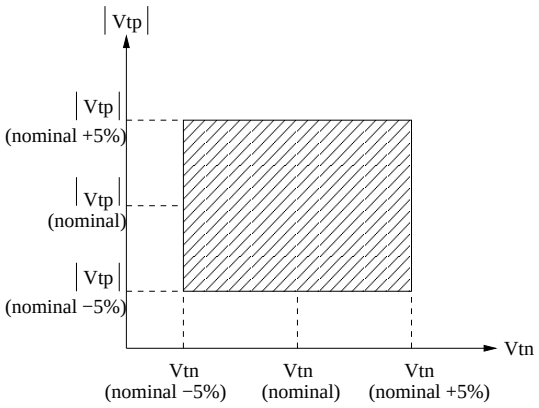

Figure 9: Corner methodology used for process variation study.

have been designed using the threshold inverting technique. The nominal results show that the ADC has an INL of $0.344LSB$, and a DNL of $0.459LSB$, showing a maximum variation of 10.5% and 5.7%, respectively, when subjected to $\pm 10\%$ variation in the supply and $\pm 5\%$ mismatch in the transistor threshold voltages. The analog supply voltage is $1.2V$. This is one of the lowest published power supply values used to implement high speed 6-bit ADCs. Several design issues have also been addressed, and used in the optimization procedure of the ADC, e.g. IR drop, low V_{LSB} etc. It is demonstrated that the design of low voltage, high speed and SoC ready ADCs is possible at $90nm$ technology and below. As part of a future work, we plan to carry out the complete design cycle including physical design for this ADC at $45nm$. Alternative encoder architectures will be explored to achieve higher sampling speeds.

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