Statistical Analysis of Steady State Leakage Currents in Nano-CMOS Devices

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***Abstract*— Motivated by the problem of process variation in nano-scale CMOS, in this paper, we propose a multivariate statistical technique that uses the well known approach of Principal Component Analysis (PCA), a technique extensively used in statistical modeling, to analyse the process variations. We use this approach to extract significant statistical information from the simulated data. We also propose a statistical model to characterize nano-scale CMOS device characteristics such as dynamic current I_{dyn}, gate leakage I_{gate}, and subthreshold leakage I_{sub} considering the effects of random variations in the process and design parameters such as gate oxide thickness T_{ox}, supply voltage V_{dd} and gate length L. These models can be used at higher level of circuit abstraction to study the design issues under process variation.**

I. INTRODUCTION

As process technology scales below 65 nano-meter regime, leakage currents grow exponentially and become a major contributor to the total power dissipation in a nano-scale CMOS circuits. Power dissipation is a critical design constraint in high performance system design, in addition to the case of traditional low power applications. To meet the increasing demand of low power VLSI circuits it is imperative to focus on leakage currents genesis and their analysis. Both dynamic and static power are significant fractions of total power dissipation in nano-scale CMOS devices. According to ITRS, the main components of power dissipation are dynamic current, subthreshold leakage and gate leakage [1] [2].

It has been observed that the major components are dynamic current I_{dyn}, gate leakage I_{gate}, and subthreshold leakage I_{sub}, and these components predominantly depend on the device geometry namely gate oxide thickness T_{ox}, and gate length L. Different leakage current components in the devices vary differently with varying supply voltage V_{dd}[3] [4]. Thus, in order to incorporate the process variation effects, statistical modeling of leakage current components is a key area to characterize nano-scale CMOS. Monte Carlo simulations provide a method to analyse the effect of process variation, but it is very expensive in terms of computational complexity.

The remainder of this paper is organized as follows. In Section II, we outline the novelty, contribution and related research. In Section III we present the mathematical modeling approach of subthreshold and gate leakage current components. The proposed methodology is explained in Section IV. In Section V, we assess proposed statistical approach to the extent of dynamic current I_{dyn}, subthreshold leakage current I_{sub} and gate leakage current I_{gate}. In Section VI, verification of proposed model is done for I_{dyn}, I_{sub}, and I_{gate}. Concluding remarks are given in Section VII.

II. CONTRIBUTIONS OF THIS PAPER AND RELATED RESEARCH

In the modeling of dynamic and leakage currents statistics of NMOS/PMOS transistors we use two methods having different level of computational complexity and accuracy. First method uses a Monte Carlo simulation to obtain the statistical analysis. The second method uses a multivariate statistical technique of PCA. This approach is novel, in a number of respects. One can use the proposed approach to extract important statistical measures from each data set which is represented by a small data set, results in significant reduction in computational burden without loosing the underlying statistical information. Our ultimate research goal is to develop statistical model to characterize nano-scale CMOS based architectural components for dynamic current, I_{dyn}, gate leakage, I_{gate}, and subthreshold leakage, I_{sub}, current considering the effects of random variation in the process and design parameters such as gate oxide thickness, T_{ox}, supply voltage, V_{dd}, and gate length, L. We considered all possible parameter combinations i.e. in the above three parameter variation, we have seven different cases. Together, we refer these cases as independent process variables or just variables. Analysis of different forms of current components of nano-scale CMOS devices has been attempted by various researchers [4]. However, most of the current works do not consider the effect of active (ON) and passive (OFF) state leakage. They do not account the effect of variation of device parameters on all prominent current components (gate-oxide leakage, dynamic, and subthreshold leakage). Some research works who address the variations are computationally complex, they only address variations in selected set of parameters, not the all the prominent parameters and there combined variation as done in this paper.

III. THE LEAKAGE MODELS

The mathematical modeling of subthreshold current, I_{sub}, and gate leakage current components are presented here. The following are the subthreshold and gate leakage equations are

used in the model [5].

$$I_{sub} = \mu \frac{W}{L} \sqrt{\frac{q\epsilon_{si} NDEP}{2\phi_s}} V_T^2 \cdot \left[1 - \exp\left(\frac{-V_{ds}}{V_T}\right)\right] \exp\left[\frac{V_{gs} - V_{th} - V_{off}}{vV_T}\right] \quad (1)$$

$$I_{gc0} = \frac{W \cdot L \cdot A \cdot V_{gs} \cdot V_{aux}}{T_{ox}^2} \exp\left[-BT_{ox}\left(AIGC - BIGC \cdot V_{oxpinv}\right)\right] \quad (2)$$

Where,

$$V_{aux} = NIGC \cdot V_T \cdot \log\left[1 + \exp\left(\frac{V_{gs} - V_{th0}}{NIGC \cdot V_T}\right)\right]$$

$$V_{oxpinv} = K1 \cdot \sqrt{\phi_s} + V_{gs} - V_{th}$$

$$I_{\text{gcd}} = \frac{1 - (PIGCD \cdot V_{ds}+) \cdot \exp\left(-PIGCD \cdot V_{ds}\right)}{PIGCD^2 \cdot V_{ds}^2 + 2e - 4} + \frac{1e-4}{PIGCD^2 \cdot V_{ds}^2 + 2e - 4} \quad (3)$$

$$I_{gcs} = \frac{PIGCD \cdot V_{ds} + \exp\left(-PIGCD \cdot V_{ds}\right)}{PIGCD^2 \cdot V_{ds}^2 + 2e - 4} - \frac{1 - 1e - 4}{PIGCD^2 \cdot V_{ds}^2 + 2e - 4} \quad (4)$$

The subthreshold leakage current I_{sub} is given by equation (1), where V_T is the thermal voltage, V_{off} is the offset voltage which determines the channel current at $V_{gs} = 0$, n is the subthreshold swing coefficients, W, L, μ, q, ϕ_s, ϵ_{si}, are the width, length, mobility of charge carriers, electron charge, surface potential and permittivity of silicon, respectively for the NMOS/PMOS transistors. Since only the gate channel current I_{gco} is the dominant gate leakage current, and the gate current for the PMOS is significantly smaller than the gate current of NMOS, we consider the modeling of gate to channel current only for the NMOS. However, the proposed model can easily extend to incorporate other gate leakage components and the gate leakage for the PMOS. The gate leakage equations are given by (2) to (4), where A, B are the physical constants, T_{ox} is the gate oxide thickness $AIGC, BIGC, CIGC\ and\ NIGC$ are the empirical parameters, $K1$ is the first order body bias coefficients and $PIGCD$ is a parameter for the partitioning of the gate to source/drain current.

IV. The Proposed Methodology

To model the dynamic and leakage currents statistics of NMOS/PMOS transistors, we use two methods which have different level of computational complexity and accuracy. The first method uses a Monte Carlo analysis to obtain the statistical analysis. The second method we use a multivariate statistical technique PCA to orthogonalize the Gaussian distributed variables. The analysis was carried out in three ways using both the methods:

1) First, we varied a single parameter at a time i.e one parameter was varied independently while other parameters were held constant. These are corresponding to variable 1 to 3.
2) Secondly, we vary the parameters in pairs of two and third parameter held constant. These are corresponding to variable 4 to 6.
3) Finally, all parameters are varied simultaneously although each parameter is statistically independent of others. This is corresponding to variable 7.

The variation in all the process and design parameters are assumed to be Gaussian distributed with variance of 10% which is reasonable assumption. For each variable we compute the μ and σ for dynamic and leakage currents. Each time the process and design parameters of interest varies and it takes the value from Gaussian distributed probability density function of given mean and variance.

A. Monte Carlo Analysis Method

We use the $45nm$ Berkeley Predictive Technology Model (BPTM) in this work [5], with base values of $T_{ox} = 1.4nm$, $V_{dd} = 0.7V$ and $V_{th} = 0.22V$. The width of the device was chosen to be very large ($W = 1000nm$), thus eliminating any narrow-width modulation effects in this analysis. In this analysis we uses 5000 HSPICE Monte Carlo simulation runs to computes the μ and σ of each variable for I_{dyn}, I_{gate}, and I_{sub}.

B. Principal Component Analysis Method

The basic idea of the PCA approach is to consider each of the variables as a input data point and determine the statistical structure of this data set using principal component analysis. The technique of PCA can be viewed as doing a rotation or coordination transformation in the parameter space, so that the resulting new statistical vectors referred to as principal components (PC's).

This is achieved by applying the singular value decomposition to the each variable data set. Figure 1 shows the fraction of variance explained by the different principal components. The number on the top of the bars show the cumulative variation accounted for up to that principal component. Note that three principal component explain more than 95% of the variance in the variables corresponding to dynamic current I_{dyn} for NMOS transistor. The singular value decomposition also provides the 7x3 rotation matrix that provides the transformation between the three significant principal components and the space of the normalized variables. This rotation matrix is shown in Table I. Rows of the table corresponding to seven different variables and the columns are corresponding to first three significant principal components. The developed statistical model employs a vary small data set of rotation matrix to compute compute the I_{dyn}, I_{gate}, and I_{sub} considering the effects of process variation.

V. Statistical analysis of Current Components

The primary goal of this analysis is to assess and characterize the extent of dynamic current I_{dyn}, gate leakage I_{gate},

TABLE I

ROTATION MATRIX OF THREE PRINCIPAL COMPONENTS

Variables	***Comp.1***	***Comp.2***	***Comp.3***
T_{ox}	0.0012	-0.7351	-0.3873
V_{dd}	-0.1449	-0.0551	0.3818
L	-0.1345	-0.0504	0.3203
T_{ox}, V_{dd}	0.5809	0.0258	-0.1961
T_{ox}, L	0.5544	0.0108	-0.1739
V_{dd}, L	-0.0713	0.1471	0.5431
T_{ox}, V_{dd}, L	-0.4325	0.6569	-0.4879

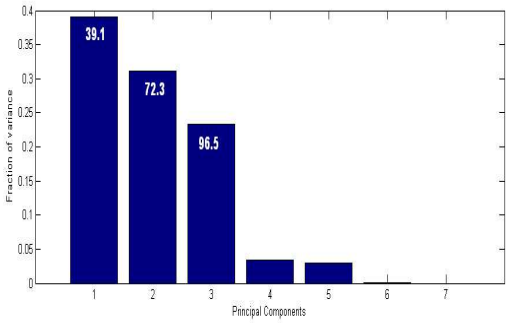

Fig. 1. Fraction of variance explained by the different principal components.

TABLE II

STATISTICAL DISTRIBUTION OF DYNAMIC CURRENT

Variables	$\mu\,(10^{-6}A)$		$\sigma\,(10^{-6}A)$	
	NMOS	***PMOS***	***NMOS***	***PMOS***
T_{ox}	317.57	147.50	8.67	4.60
V_{dd}	318.13	148.20	2.71	9.84
L	326.50	153.20	71.56	38.71
T_{ox}, V_{dd}	317.64	147.76	9.19	11.30
T_{ox}, L	328.85	154.61	75.73	41.40
V_{dd}, L	326.75	153.52	72.78	40.84
T_{ox}, V_{dd}, L	326.60	153.47	69.23	38.63

TABLE III

STATISTICAL DISTRIBUTION OF SUBTHRESHOLD LEAKAGE CURRENT

Variables	$\mu\,(10^{-9}A)$		$\sigma\,(10^{-9}A)$	
	NMOS	***PMOS***	***NMOS***	***PMOS***
T_{ox}	53.91	39.94	11.37	9.20
V_{dd}	52.96	48.96	10.28	32.96
L	165.8	108.09	435.8	262.18
T_{ox}, V_{dd}	53.47	49.24	11.37	37.02
T_{ox},L	212.3	138.71	1238.7	761.21
V_{dd}, L	165.2	130.99	434.24	343.27
T_{ox}, V_{dd}, L	161.0	125.65	499.3	381.33

and subthreshold leakage I_{sub} variation as a result of process variation in gate oxide thickness T_{ox}, supply voltage V_{dd} and gate length L. These characterizations were carried out for NMOS and PMOS transistors with the help of Monte Carlo Simulations. The distribution ($\pm$ 3σ) of these parameters is assumed to be Gaussian with the variance of 10%. Table II-IV shows the statistical distribution μ and σ of I_{dyn}, I_{sub}, I_{gate}. The first column of each table contains the variable, second and third column corresponding to μ and σ of I_{dyn}, I_{sub}, I_{gate} in NMOS and PMOS transistors respectively.

A. Dynamic Current (I_{dyn})

Table II shows the effect of parameters variation on dynamic current, I_{dyn}. The nominal value for dynamic current I_{dyn} for NMOS and PMOS transistors is 318.00 μA and 148.00μA respectively. The effect of variation in gate length L has a severe effect on I_{dyn} in NMOS worse than PMOS devices. Next parameter that severely affects the performance of the device under process variation is gate oxide thickness T_{ox}. The combination of both parameters worsens the effects on the performance of the device. However, when all the parameters are varied simultaneously the effect on I_{dyn} is less dominant compared to the 5th and 6th variables. The influence of variation in supply voltage V_{dd} is found to be less compared to L and T_{ox} variations.

B. Subthreshold Leakage Current (I_{sub})

Table III shows the statistical distribution of subthreshold leakage current. It is observed that the subthreshold current is extremely sensitive to the variations in L and T_{ox}. It is also observed that I_{sub} is not very sensitive to V_{dd}. Whereas, the combination of L and T_{ox} have a much stronger affects, which is analogous to variable 5 (i.e. T_{ox}, L). The nominal value of I_{sub} for NMOS and PMOS is 52.90nA and 39.00nA respectively. The variation in V_{dd} compensates the strong effect of T_{ox} and L variation on I_{sub} which is analogous to variable 7 (i.e. T_{ox}, V_{dd}, L).

C. Gate Leakage Current (I_{gate})

Table IV shows the effect of parameters variation on gate leakage current I_{gate}. The effect of variation in oxide thickness (T_{ox}) has a severe effect on NMOS worse than PMOS devices due to exponential dependence on T_{ox}. Next parameter that severely affects the performance of the device is gate length (L). The combination of both parameters worsens the effects on the performance of the device. The variation in supply voltage V_{dd} is found to be insignificant compared to L and T_{ox} variations.

VI. MODEL VERIFICATION

In order to verify the proposed statistical model to characterize nano-scale CMOS based architectural components for I_{dyn}, I_{sub}, I_{gate} considering the effects of random variations in the process and design parameters such as T_{ox}, V_{dd} and L.

TABLE IV

STATISTICAL DISTRIBUTION OF GATE LEAKAGE CURRENT

Variables	$\mu\,(10^{-9}A)$		$\sigma\,(10^{-9}A)$	
	NMOS	***PMOS***	***NMOS***	***PMOS***
T_{ox}	83.39	2.66	37.86	1.47
V_{dd}	76.10	2.36	0.44	0.01
L	76.57	2.33	1.58	0.02
T_{ox}, V_{dd}	81.78	2.61	36.51	1.43
T_{ox},L	82.33	2.59	36.70	1.39
V_{dd}, L	76.56	2.53	1.63	0.02
T_{ox}, V_{dd}, L	86.26	2.79	41.83	1.73

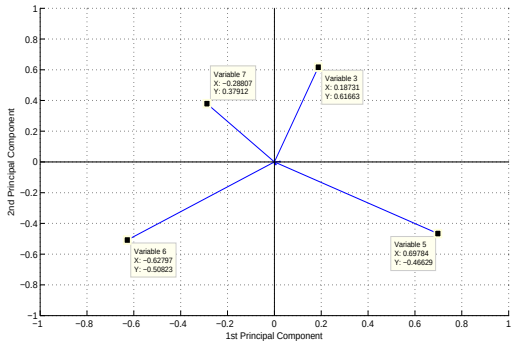

Fig. 2. Bi-plot of first and second principal components for dynamic current .

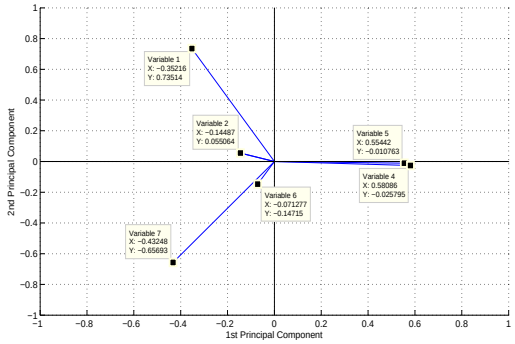

Fig. 3. Bi-plot of first and second principal components for subthreshold leakage current.

For each data set of leakage components and dynamic current, we compute the first and second principal components, as considerable information is contained in these components. Here we are presenting the obtained results of NMOS transistor only because of space limitations. The bi-plot of these variables for I_{dyn}, I_{sub}, I_{gate} are shown in Figure 2- 4. Here the variable 1 to7 are corresponding to variables T_{ox}, V_{dd}, L, $T_{ox}V_{dd}$, $T_{ox}L$, $V_{dd}L$, and $T_{ox}V_{dd}L$ respectively.

A. Dynamic Current (I_{dyn})

The effects of process variation on I_{dyn} for each set of variables are shown in Figure 2. It is observed that the variables 5, 6, 3 and 7 are affected by the process variation in increasing order, which are analogous to the results obtained from Monte Carlo simulation as shown Table 2, in rows 5, 6, 3 and 7 respectively.

B. Subthreshold Leakage Current (I_{sub})

As it is found from the statistical analysis that among three currents subthreshold current is most sensitive and strong effects of process variations. It is observed from the plot of first and second principal components shown in Figure 3, that all the variables are affected by the process variation. The similar trend in variation can also be, observed from Table 3, which is obtained from the Monte Carlo simulation.

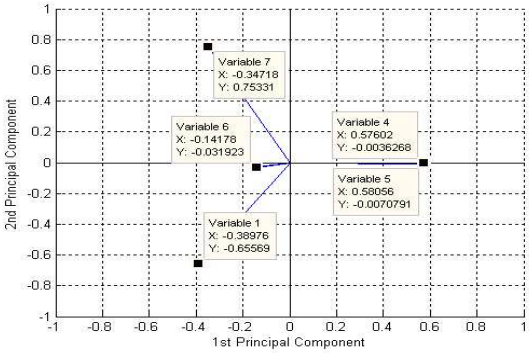

Fig. 4. Bi-plot of first and second principal components for gate leakage current.

C. Gate Leakage Current (I_{gate})

Figure 4 shows bi-plot of first and second principal components for each set of variables. It is observed that the variables 1, 7, 4, 5 and 6 are affected by the process variations in increasing order, which are analogous to rows 1, 7, 4, 5 and 6 respectively of the results obtained from Monte Carlo simulation, Table 4.

VII. Conclusion

In this paper, we proposed a multivariate statistical technique that uses the well known approach PCA. We use this approach to extract significant statistical information from the simulated data. We also developed a statistical model to characterize nano-scale CMOS device characteristics such as dynamic current (I_{dyn}), gate leakage (I_{gate}), and subthreshold leakage (I_{sub}) considering the effects of random variations in the process and design parameters like gate oxide thickness (T_{ox}), supply voltage (V_{dd}) and gate length (L). The proposed model drastically reduces the computational burden without loosing the underlying statistical information, hence these models can be used at higher level to study the design issues under process variation for any number of variables and design parameters.

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