A Universal Voltage Level Converter for Multi-V_{DD} Based Low-Power Nano-CMOS Systems-on-Chips (SoCs)

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Abstract

Level Converters are key components of multi-voltage based systems-on-chips. Recently, a great deal of research has been focused on power dissipation reduction using various types of level converters in multi-voltage systems. These level converters include either level up conversion or level down conversion. In this paper we propose a unique level converter called universal level converter (ULC). This level converter is capable of four types of level converting functions, such as up conversion, down conversion, passing and blocking. The universal level converter is simulated in CADENCE using 90nm PTM technology model files. Three types of analysis such as power, parametric and load analysis are performed on the proposed level converter. The power analysis results prove that the proposed level converter has an average power reduction of approximately 87.2% compared to other existing level converters at different technology nodes. The parametric analysis and load analysis show that the proposed level converter provides a stable output for input voltages as low as 0.6V with a varying load from 1fF-200fF. The universal level converter works at dual voltages of 1.2V and 1.02V (85% of Vddh) with V_{TH} value for NMOS as 0.339V and for PMOS as -0.339V. The ULC has an average power consumption of 27.1µW at a load of 45fF.

1. Introduction and Motivation

Power dissipation reduction in integrated circuits (ICs) is the most demanding issue for present chip-design engineers. This is due to the increasing popularity of high performance and low power ICs, especially for mobile application. Researchers have developed various techniques to reduce the power dissipated by an integrated circuit, such as transistor sizing, reducing the supply voltage and multiple threshold voltages [Ishihara 2004, Usami 1997]. However power consumption reduction by such methods suffers from various disadvantages, like increase in leakage and latency of the system. Power savings through transistor sizing disappears as soon as the available slack in the circuit is used up [Ishihara 2004].

A multi-voltage supply system is very efficient approach towards dynamic power dissipation reduction [Horowitz 2004]. In such systems the whole circuit is operating at different voltage levels such that all the circuits on the critical path are provided with higher voltage (Vddh) and those which are not on the critical path are supplied with lower voltage (Vddl). One of the main advantages of using this scheme is that we can use the regular fabrication process reduced parallel or pipelined data paths which might cause heavy area penalty and increase in latency [Sundararajan 2004]. However, there should be a proper trade off between the power consumption reduction and the overall robustness of the system [Ishihara 2004]. Moreover, care should be taken that there is no path for static current flowing from voltage source (Vdd) to ground, as this will lead to undesirable short-circuit power consumption [Yu 2001]. This is evident from Fig 1. Assume that the input at node N1 swings from high to low; if the output of inverter I1 operating at Vddl is connected directly to node N2 operating at Vddh, then the output of I1 is not sufficient enough to turn off the pull-up circuit of I2 completely. As the pull-down is also switched on, there exists a direct path for static current flow from Vdd to ground.

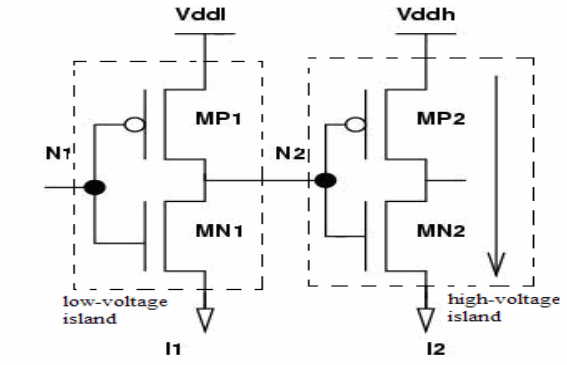

Fig. 1 Direct connection between Vddl and Vddh circuits demonstrating the need of level converter [Chin 2005]

This flow of short-circuit current is highly undesirable as it consumes power. Thus, a level converter is necessary as an interface between the two voltage islands operating at different voltages.

We propose a novel level converter called universal level converter. This level converter is capable of performing four types of operations on the signal such as (i) Level-up conversion, (ii) Level-down conversion, (iii) Blocking and (iv) Passing. It can convert a signal at lower voltage to a higher as well as convert a signal at higher voltage level to lower voltage level. In addition, it can also block or pass the signal from the input side to the output side. The universal level converters are very useful in multi voltage system-on-chips (SoC's). They can also be effectively applicable for LSI high speed input-output circuits, as an interface between internal and external buses as a server or exchanger. They can also be used as an interface circuit between optical devices for optical communications [Chin 2005].

This paper is organized in the following manner: Section 2 present the related work in this field. The description and schematic implementation of the proposed Universal Level Converter are discussed in section 3. Section 4 highlights the simulation set up and the characterization of the proposed universal level converter. A layout of the level converter is described in section 5. Finally, the paper is concluded in section 6 along with directions for future work.

2. Related Research Works

Level converter plays a very critical role in a Multi-Voltage Supply System. A lot of research has been done for power consumption reduction using multi voltage systems and level converters. In [Ishihara 2004] key properties and design metrics of level converters for dual-Vdd systems are examined. They have also proposed several level converters implemented in flip-flops called LCFFs. The authors have also compared their proposed LCFF's with some standard level converters like CCLC, SSLC and precharged circuits in terms of level converter performance and robustness as well as overall system level performance and robustness. In [Yu 2001], [Chin 2005], [Kulkarni 2001] and [Sadeghi 1999] a study of a conventional level converter circuit called DCVS (Dual Cascode Voltage Switch) is studied. The DCVS circuit consists of a cross-coupled pair of PMOS which act as a differential pair. Each of the above referenced papers proposes level converters based on a DCVS circuit addressing the contention problem in the conventional level converter circuit. In [Yu 2001] the same concept of cross coupled pair of PMOS is used with addition of two NMOS transistor to reduce the contention problem. In [Chin 2005] a keeper transistor is used as a level restorer [Bellaouar 1995]. A comparative perspective of various research works addressing level converters is represented in Table 1.

3. Design of Universal Level Converter

The proposed universal level converter performs four operations: level-up conversion, level-down conversion, blocking, and passing. The conversion of a signal at a low voltage level (Vddl) to a higher voltage level (Vddh) is called level-up conversion. In contrast, the conversion of a signal at a higher voltage level (Vddh) to a lower voltage level (Vddl) is called as level-down conversion. The blocking circuit is responsible for completely stopping any kind of signal at the input side to appear at the other side (Z or high impedance condition). Finally, the pass circuit passes the input signal to the output as it is. The proposed level converter is capable of all the above four mentioned functionalities depending on the type of requirement. The type of operation to be

Table 1: Related research in level converter design

Research Work	Year	Technology	Delay	Power Consumption	Type of Circuit	Design approach
Ishihara 2004	2004	0.13μm	287ps	----	Level-up conversion	Level converting flip flops
Kulkarni 1999	1999	0.13μm	----	----	Level-up conversion	DCVS and Keeper transistor
Yu 2001	2001	0.35μm	----	220.57μW	Level-up conversion	Symmetrical Dual Cascode Voltage Switch (SDCVS)
Sadeghi 2006	2006	0.1μm	----	----	Level-up conversion	Keeper transistor in pass transistor logic
Kanno 2000	2000	0.14μm	----	----	Level-down conversion	Differential input pair operation
Chin 2005	2005	0.18μm	----	----	Level-up conversion	Dual Cascode Voltage Switch (DCVS)

performed can be selected using two control signals. Fig. 2 shows the high level block diagram of the universal level converter. As shown in the diagram Vin is input signal and S0 and S1 are the two control signals. Vddl and Vddh constitute the dual voltage supply applied to the circuit. The ULC employs four different circuits to perform the four distinct operations. This schematic view of the universal level converter is shown in Fig. 3. As shown in the schematic view the ULC has four independent blocks for each of the four functions and a 4:1 multiplexer is used to couple all the four outputs signals to the output of the universal level converter. A cross coupled level converter is used as an up-converter circuit. A differential input level converter is used in the down-converter circuit. Transmission gates are used to build the pass and blocking circuits

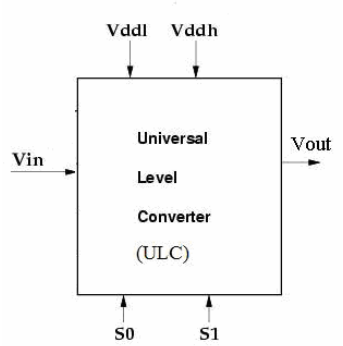

Fig. 2 High-level representation of the universal level converter

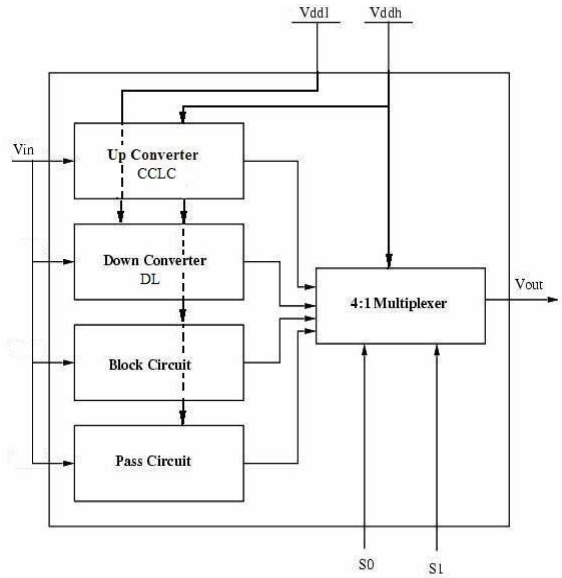

Fig. 3 Block diagram of universal level converter

A cross coupled level converter (CCLC) as shown in Fig. 4 is used as a level-up converter. The CCLC, which consists of a PMOS pair connected back to back, forms a differential pair such that if the voltage at the input swings from high to low the voltage at the output side will be pulled to a higher level [Ishihara 2004]. For down conversion a differential input level converter as shown in Fig. 5 is used. With the use of differential input pair, stable operation for low-voltage and high speed can be achieved [Kanno 2000]. Blocking circuit and the pass circuits are built by using transmission gates. For the blocking circuit a tri-state buffer which makes use of transmission gates is used in its 'not enabled' mode as a high impedance circuit. And a transmission gate used to form the pass circuit. A 4:1 multiplexer circuit is used to couple these four different outputs into one single output. The multiplexer is The transistor level schematic of the universal level converter is shown in Fig. 6. In the schematic Vin is were the input signal is applied, the output is observed at Vout and S0 and S1 are the two control signals which are used to select the desired operation, this makes the ULC programmable. Table 2 describes the values of S0 and S1 corresponding to a particular operation.

Table 2: Different operations based on S0 and S1

Select Signal		Type of Operation
S0	S1	
0	0	Pass Signal
0	1	Block Signal
1	0	Down conversion
1	1	Up conversion

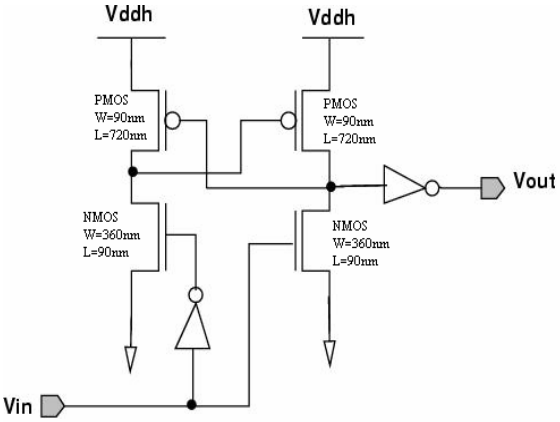

Fig. 4 Up converter circuit

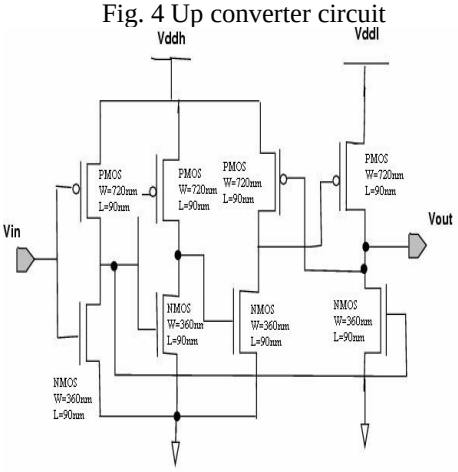

Fig. 5 Down converter circuit

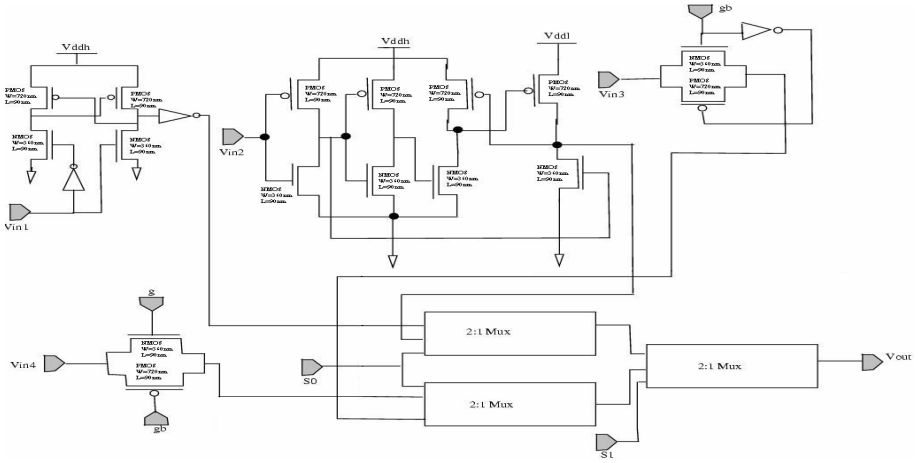

Fig. 6 Transistor level circuit diagram of the proposed level converter (ULC)

4. Characterization and Simulation Results

We have used the Predictive Technology Model 90nm models for simulating our design. A W/L ratio of 4:1 and 8:1 for the NMOS and PMOS respectively is used for simulation. The device parameters for NMOS are W= 360nm and L = 90nm and that for PMOS are W = 720nm and L = 90nm. A transient analysis for 100nsec was performed. The typical values of Vddl and Vddh used during simulation are 1.2V and 1.02V and a load capacitor of 45fF is used.

As level converters are implemented in low power designs, it is highly important to analyze and study the performance of the proposed level converter under different operating conditions. Thus, we have characterized the proposed universal level converter by performing three types of analysis: (i) parametric analysis, (ii) power analysis and (iii) load analysis which prove that our design is not only a low power design but it also provides stable output under a varying load conditions. The output results of up converter, down converter, pass circuit and block circuit are shown below in Fig. 7 – Fig. 10.

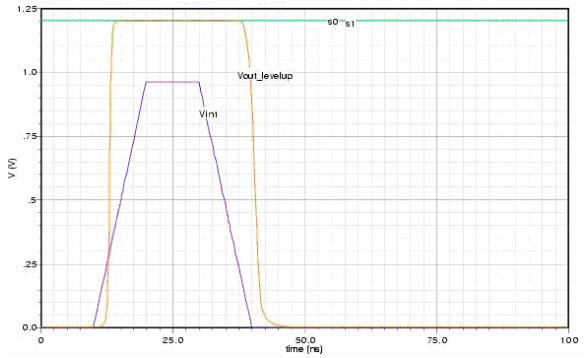

Fig. 7 Output for Level-up Conversion at Vddl = 1.02V, Vddh = 1.2V and load = 45fF

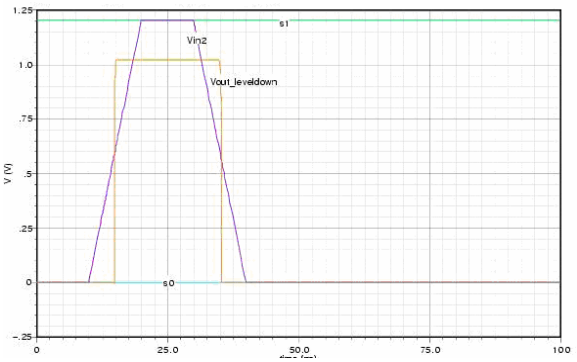

Fig. 8 Output for Level-down Conversion at Vddl = 1.02V, Vddh = 1.2V and load = 45fF

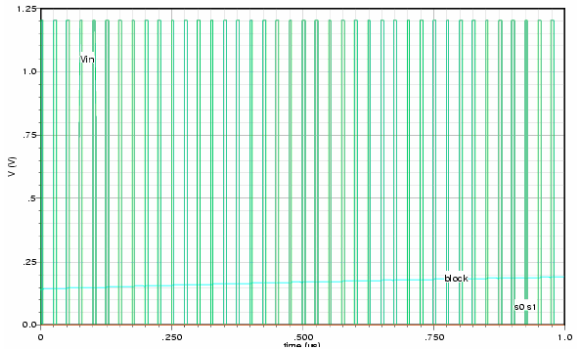

Fig. 9 Output for block signal operation

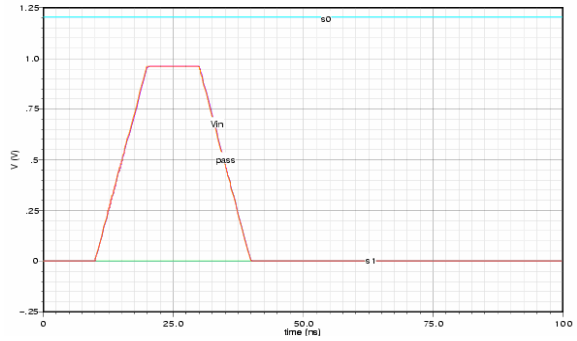

Fig. 10 Output for pass signal operation

4.a. Parametric Analysis

For this analysis, the value of Vddh is kept constant at 1.2V and the value of Vddl is varied from 0.1V to 1.02V with an increasing step of 0.1V and the transient response at the output terminals is plotted. It is observed that for the level up converter the circuit produces a stable output for a voltage as low as 0.60V. The same set-up is repeated for the down converter and it is observed that the circuit produces a stable voltage for voltages greater that 0.75V. The output plots for level up and down converters after the parametric analysis are shown in Fig. 11, Fig. 12 and Fig. 13.

4.b. Power Analysis

In this analysis the total power consumed by the entire level converter circuit is measured. The power consumed by each independent circuit in the universal level converter circuit is also observed. The total power of the universal level converter can be calculated using the following formula: P*ulc* = P*cclc* + P*dl* + P*block* + P*pass.*
In this power analysis, we have calculated the power consumed by the universal level converter for three different loads. The calculated results are shown in Table 3. From this we can conclude that the proposed universal level converter has very low power consumption as compared to other traditional level converters which have about 220.57 µW of power consumption [Yu 2001]. Our level converter has an average power consumption of 27.534 µW. This comparison proves that the universal level converter at 90nm technology has up to 87.2% lower consumption than traditional level converters at a larger technology node.

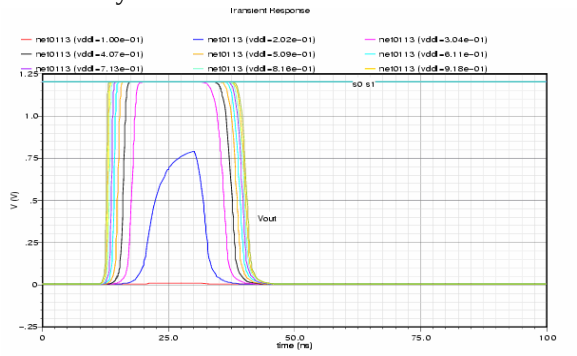

Fig. 11 Parametric analysis for up-converter circuit showing the output (Vout) waveforms when Vddl is varied from 0.1V to 1.02V with an increasing step of 0.1V and Vddh = 1.2V.

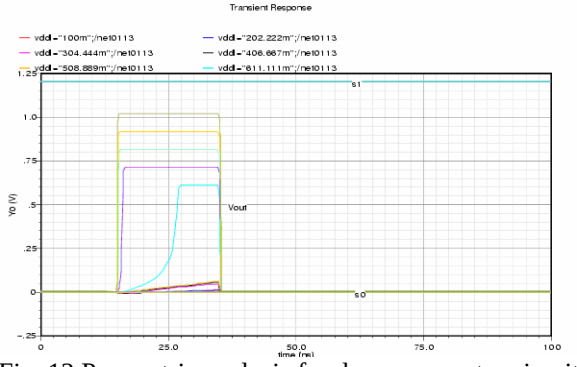

Fig. 12 Parametric analysis for down-converter circuit showing the output (Vout) waveforms when Vddl is varied from 0.1V to 1.02V with an increasing step of 0.1V and Vddh = 1.2V.

4.c. Load Analysis

In load analysis, the performance of the universal level converter is studied at various loads. The circuit is examined for its output by varying the load at the output from 1fF-200fF.

The results as shown in Fig. 14, Fig. 15, and Fig. 16 prove that the circuit produces a stable and expected output voltage for respective circuits under varying load conditions.

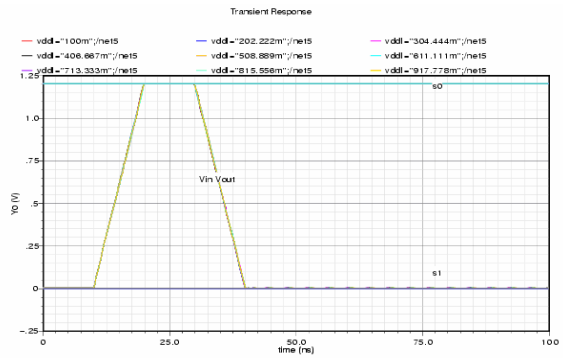

Fig. 13 Parametric analysis for down-converter circuit showing the output (Vout) waveforms when Vddl is varied from 0.1V to 1.02V with an increasing step of 0.1V and Vddh = 1.2V.

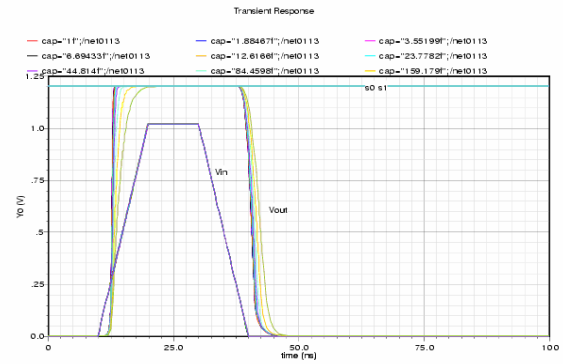

Fig. 14 Output for level up Conversion under different load conditions (load = 10fF to 200fF)

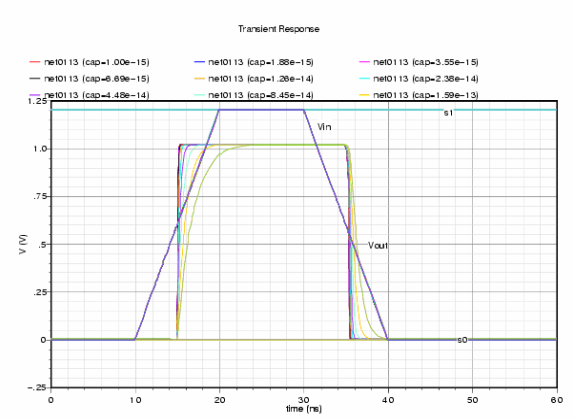

Fig. 15 Output for down-converter circuit under different load conditions (load – 10fF to 200fF)

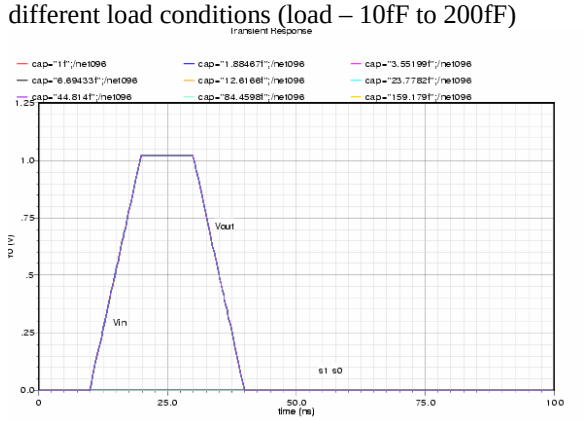

Fig. 16 Output for pass circuit under different load conditions (load – 10fF to 200fF)

5. Layout of the universal level converter

We have used the standard cadence process design kit called gpdk_90nm for the layout implementation of the proposed level converter. In this layout design, we have used two Vdd rails each representing Vddl and Vddh and one ground rail. The layout of the universal level converter (ULC) is shown in Fig. 17.

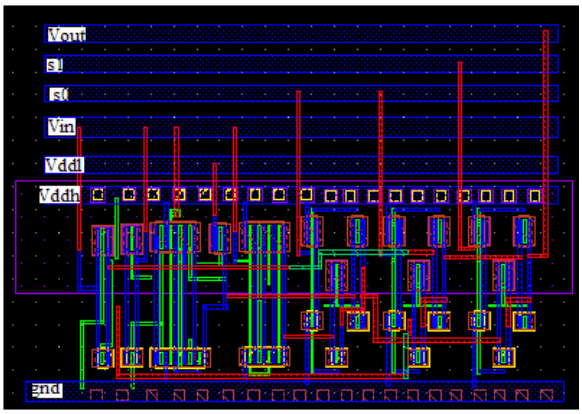

Fig. 17 Layout of the universal level converter (ULC)

6. Conclusion and Future Works

In this paper, we have proposed a unique level converter called universal level converter which is capable of performing four types of distinct level converting operations on the input signal. We have tested the schematic as well as the layout of the ULC at 90nm technology using the 90nm PTM models for schematic and generic pdk_90nm design kit for the layout, respectively. Keeping in mind the various design constraints of low power design, we have characterized our level converter design by performing parametric, power and load analyses on out design. These analyses prove that our design gives a very stable output even under varying load conditions and consumes very low power, thus making it an efficient low power design. Our design can be further extended by completing the post layout simulation for 90nm technology. The schematic as well as the layout simulations or the design can also be carried out further at lower technologies as a part of future work.

Table 3: Power analysis results for ULC under varying load conditions

Load	Circuit	Power Consumption (µW)	Total Power Consumption (µW)
10fF	Level-UP Converter	16.10	26.928
	Level-Down Converter	10.575	
	4:1 Mux	0.22426	
	Block Circuit	0.026244	
	Pass Circuit	0.002242	
45fF	Level-UP Converter	16.2702	27.4801
	Level-Down Converter	10.50702	
	4:1 Mux	0.613143	
	Block Circuit	0.024201	
	Pass Circuit	0.00256	
90fF	Level-UP Converter	16.477	28.1982
	Level-Down Converter	10.5725	
	4:1 Mux	1.12139	
	Block Circuit	0.0262963	
	Pass Circuit	0.002489	

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