Impact of Gate Leakage on Mixed Signal Design and Simulation of Nano-CMOS Circuits

Saraju P. Mohanty
smohanty@cse.unt.edu

Elias Kougianos
eliask@unt.edu

VLSI Design and CAD Laboratory (http://www.vdcl.cse.unt.edu)
Dept. of Computer Science and Engineering
P.O. Box 311366, University of North Texas, Denton, TX 76203.

Abstract*—Design optimization for performance enhancement in analog and mixed signal circuits is a major area of research as technology scaling is moving towards the nanometer scale. This paper presents an approach towards the characterization of mixed signal circuits using a 45nm CMOS Voltage Controlled Oscillator with frequency divider as the base line circuit. The performance characteristics of the analog and digital blocks in the circuit are simulated and the accuracy issues arising due to separate analog and digital simulation engines are considered. The tremendous impact of gate tunneling current on device performance is quantitatively analyzed with the help of an "effective tunneling capacitance" which also allows accurate modeling and simulation of digital blocks with almost analog accuracy.*

I. INTRODUCTION

Analog and mixed signal simulation is becoming an important issue that affects both the time-to-market and product cost of many modern electronic systems, particularly for system-on-chip (SoC) designs [1]. The operation of analog circuits is very sensitive on mismatches between the components and their dynamic range is limited by noise, offset and distortions. The situation will be further complicated when design will be performed using nanoscale CMOS transistors that are currently being used on the digital circuit side and eventually will be used in analog circuits to follow the semiconductor roadmap [2], [3].

The effects of decreasing the feature size and power supply due to aggressive technology scaling has resulted in the challenges related to mixed signal circuit design and simulation [2], [3]. Technology scaling in circuits increases the leakage current and as the scaling reaches the nanometer level, the leakage current cannot be ignored in the power consumption or the functionality of the circuits. In particular, as technology scales to 45nm and below, an added dimension of leakage current of traditional CMOS devices enters the picture: gate tunneling current. Its impact on the operation of digital circuits has received considerable attention [4], [5], but its effects on analog circuitry are still not well understood. Thus, there is a need to develop effective ways to maintain performance and solutions related to analog design and simulation issues in modern nanometer CMOS processes are discussed in this work.

Several VCO and PLL designs have been already presented in the literature [6]. High performance CMOS based VCO designs have been achieved using analog feedback control [7]. Low power PLL designs can be achieved by reducing V_{dd}, *which* is a new trend in analog CMOS system design [8]. In [9], a comparative analysis between NMOS and PMOS VCOs has been performed and it was concluded that NMOS based VCOs are beneficial in terms of high frequency and low voltage. Concepts related to jitter in ring oscillators are discussed in [10]. There are mainly two issues that were considered by the authors in [3] relating to technology scaling: gate leakage and decrease in supply voltage, which would lead to low performance of the circuit. As a solution to the above two issues,

the critical parts can be operated at high supply voltages by exploiting different combinations of thin and thick oxide transistors. In addition, the issue of gate leakage is addressed by using active cancellation techniques. They have also introduced a parameter called bias insensitive frequency f_{gate}, which is used for quick estimation of the effect of *gate* leakage. The authors in [11] examined the behavior of MOS devices with respect to gate leakage and analyzed the performance of common source amplifiers and current mirrors.

The paper is organized as follows: Section II presents the contributions of this paper. Section III gives a comparative perspective between the analog and mixed signal simulation approaches. Section IV presents the design and simulation of a VCO with frequency divider. Section V gives an overview of the approaches considered for improving the accuracy in mixed signal simulations and quantifies the gate leakage effect. The paper is concluded in Section VI.

II. CONTRIBUTIONS OF THIS PAPER

The contributions of the paper may be summarized as follows: we designed a 45nm CMOS voltage controlled oscillator (VCO) with frequency divider, performed analog simulations of the VCO and compared both analog and digital simulations of the frequency divider. We then present a way of quantifying the effect of gate leakage on the operation of the frequency divider as well as means of accurately incorporating this effect into digital behavioral simulations and we also provide quantitative measures of the relative magnitude of gate leakage versus traditional gate capacitive effects on system operation.

III. ANALOG VS MIXED SIGNAL SIMULATION: A COMPARATIVE PERSPECTIVE

The main goal of today's CMOS designs in terms of performance is low power and high frequency of operation. This can be achieved to a large extent by implementing mixed signal circuits, if the integration of both the analog and digital circuits is made efficient in terms of high frequency, low power, and small area. Analog circuit designs are usually considered for any electronic circuit design but digital circuits have become predominant due to their lower power consumption and reliability [12]. As scaling takes place digital circuits have advantages but analog circuits may still be considered for high precision processing [13]. As a compromise, mixed signal circuits are considered, but these are quite difficult to design as the analog portion of the circuit depends on various metrics, which are fundamentally different from the metrics of the digital circuits. Low power consumption and smaller area would be the main reasons to implement mixed signal circuits rather than considering purely analog or digital circuits. Mixed signal circuit designs are beneficial when various techniques to design, isolate noise, and interface the analog and digital components are considered and if the whole process is optimized [14].

Simulating an entire PLL or even subsystems of it, such as the VCO, using analog (SPICE) simulations is time consuming and CPU intensive, particularly at the post-layout stage. As a solution to this, some components are simulated as analog and some as digital blocks using both analog and digital simulation engines (mixed mode simulation.) Mixed signal circuits provide improved system reliability and flexibility [15] and are a combination of analog circuits where the analog signals are continuously varying voltages, currents, or frequencies and digital circuits, which are discrete in nature. Due to the difference in nature of the simulation techniques and engines used for each discipline, discrepancies can arise between the simulation results of a given block, depending on whether it is simulated in analog or digital mode. Analog simulation results are always superior but also very time consuming. A common compromise is to simulate a block in analog mode and use the

results to generate a more accurate digital model that includes loading and other second order effects. This approach is followed in the work presented in this paper.

IV. DESIGN AND SIMULATION OF A NANO CMOS VCO

Usage of nanometer CMOS VCO circuits is necessarily increasing due to their wide usage in many RF based communication systems. For different ranges of frequencies, different topologies can be used. In a PLL, the frequency from the VCO is changed either by changing the reference signal or the divide by ratio of the frequency divider. Due to the stability of the reference signal, a frequency divider is used which divides the frequency from the VCO, so that the frequency matches with the reference frequency from the phase detector. In this section we consider the design of a VCO with frequency divider along with the simulation approaches used to validate its performance.

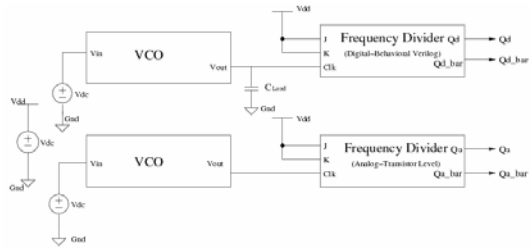

Figure 1: Block diagram of the VCO along with an analog frequency divider and a digital frequency divider. The role of the capacitor C_{Load} is to model capacitive loading effects, as explained in the text.

The design of a nanometer CMOS VCO should take into consideration different performance issues in terms of power consumption, noise, and frequency. Frequency performance is given importance in this paper. A basic block diagram of the VCO with frequency divider is shown in Fig. 1. Transistor level schematics of the VCO and the frequency divider are given in Figs. 2 and 3, respectively. The block diagram in Fig. 1 also has a purely digital block for the frequency divider, which is implemented using behavioral level Verilog. A loading capacitor C_{Load} is added at the input of the digital frequency divider and will be discussed in section V.

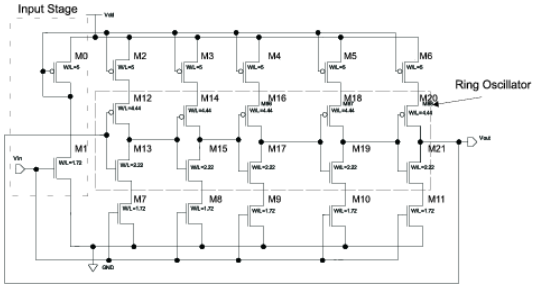

Figure 2: Transistor level diagram of the VCO.

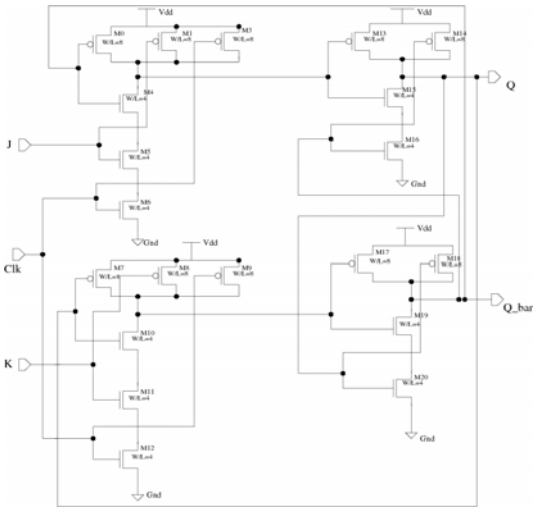

Figure 3: Transistor level diagram of the frequency divider.

A. Design of a base line VCO and Frequency Divider

The type of VCO considered in this work is of the current starved type, as other designs require large resistors and capacitors consuming a lot of area [16]. The design as shown in Fig. 2 comprises of two input stage transistors with high impedance, an odd numbered chain of inverters along with two current source transistors per inverter, which limit the current flow to the inverter, that is they are starved for current. The circuit has no stable operating point and it will oscillate at some frequency that is determined by the number of inverters, size of the transistors in the circuit, and the current flowing through the inverter, which is dependent upon the

input voltage to the VCO. The operating frequency of the VCO, f_o can be determined using the relation:

$$f_o = \frac{1}{N(T_{TOT})} = \frac{I_{inv}}{(N * C_{TOT} * V_{dd})}, \qquad (1)$$

where V_{dd} is the supply voltage, I_{inv} is the current flowing through the inverter, N is the odd number of inverters in the VCO circuit and T_{TOT} is the total time required to charge or discharge the capacitance of each stage of an inverter and is given by:

$$T_{TOT} = \frac{(C_{TOT} * V_{dd})}{I_{inv}}. \qquad (2)$$

The sum of the input and output capacitances C_I and C_O, respectively gives the total output capacitance C_{TOT} on the drains of the inverter transistors. The equation for C_{TOT} is:

$$C_{TOT} = C_O + C_I = \hat{C}_{ox}(W_p L_p + W_n L_n) + \frac{3}{2}\hat{C}_{ox}(W_p L_p + W_n L_n). \qquad (3)$$

This can be further simplified as

$$C_{TOT} = \frac{5}{2}\hat{C}_{ox}(W_p L_p + W_n L_n) \qquad (4)$$

Here $\hat{C}_{ox}$ is the gate oxide capacitance per unit area, W_n and W_p are the widths and L_n and L_p are the lengths of the NMOS and PMOS transistors, respectively. The operating frequency of the VCO can be mainly controlled by an applied DC input voltage, which adjusts the current I_{inv} through each inverter stage.

Next we consider the operation of the analog frequency divide, which is implemented via a JK flip-flop. This circuit was implemented using two 3– input NAND gates and two 2–input NAND gates as shown in Fig. 3. For simulation purposes, we can also consider the frequency divider in terms of behavioral Verilog, as shown in Fig. 1.

B. Analog Simulation of the Circuit

The analysis of reaching a state of minimum power consumption at a particular level of performance can be done either by finding a new absolute lower limit for power consumption and using it or by examining the process performance at different levels using different parameters like supply voltage and gate oxide thickness and optimizing the circuit [17]. The Analog simulation of the circuit is done by considering both the VCO and the frequency divider as analog components where the clock output of the VCO is fed to the frequency divider whose output is again a clock but with half the frequency of the input clock as shown in Fig. 4. The SPICE models used in this work are for a 45nm CMOS process with gate oxide thickness T_{ox} = 1.4nm and threshold voltage $|V_{th}|$ = 0.22V. The circuit has been simulated using Cadence's analog and mixed design environment and the SPECTRE and SPECTREVerilog circuit simulators.

C. Mixed Signal Simulation

An analog, transistor-level representation of the VCO along with a behavioral Verilog representation of the frequency divider which is digital in nature are considered for the mixed signal simulations. In this circuit the analog clock output of the VCO is fed to the digital frequency divider and a digital clock output with half the frequency is obtained at the output as shown in Fig. 4.

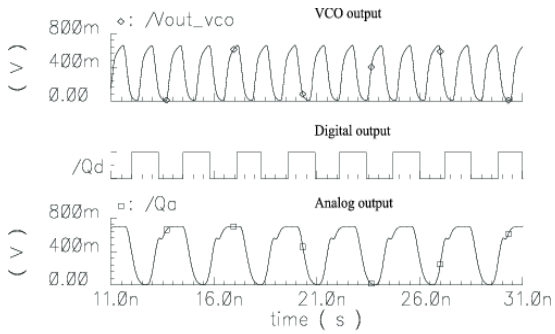

Figure 4: Output waveforms of the VCO, digital frequency divider, and analog frequency divider

To allow communication between the analog and digital components or vice versa in the mixed signal circuit, interface elements have been used and an analog to digital interface is created between the analog VCO and the digital frequency divider. The parameters

related to the interface elements can be further customized: the *a2d* interface used here considers two voltage levels, V_{low} and V_{high} below and above which the signal takes the values of LOW and HIGH, respectively and along with them is a timing parameter called TIMEX according to which a voltage level between V_{low} and V_{high} for longer than TIMEX yields a logic X (undefined). Similarly, the *d2a* interface also has different parameters like the voltage levels, rise and fall times that can be characterized in accordance with the output required.

V. ACCURACY IN MIXED SIGNAL SIMULATIONS: IMPACT OF GATE LEAKAGE AND PROPOSED REMEDY

Following the different simulation modes as presented in Section IV the following operating frequencies were obtained:

$$f_{VCO} = 717.96 \text{ MHz}, \quad (5)$$

$$f_a = 357.9 \text{ MHz}, \quad (6)$$

$$f_d = 394.03 \text{ MHz}, \quad (7)$$

where, f_{VCO} is the frequency at the output of the VCO, f_a is the frequency at the output of the analog frequency divider and f_d is the frequency at the output of the digital frequency divider.

It can be seen that there is a significant difference in the simulation results, depending on whether the frequency divider is considered as analog or digital. This discrepancy, $\Delta f = |f_d - f_a| = 36.13$ MHz, is quite large (approx. 10%) and is due to two factors: (i) regular capacitive loading of the VCO by the frequency divider and (ii) transient capacitive loading due to gate oxide tunneling current in the transistors of the frequency divider.

The nature of the transient capacitive loading can be explained by recognizing that gate leakage current is present during both ON and OFF states of a transistor. If these currents are I_{ON} and I_{OFF}, respectively, during an ON – OFF or OFF – ON transition, an effective tunneling capacitive load is then manifested, given by:

$$C_{eff}^{tun} = \left| \frac{I_{ON} - I_{OFF}}{dv_g / dt} \right| dt \,, \quad (8)$$

where v_g is the voltage applied on the gate.
In order to account for these capacitive loads, a capacitor C_{Load} is placed at the input of the frequency divider behavioral model, as shown in Fig. 1. The initial value used for the optimization is derived by monitoring the total gate current due to all the devices in the frequency divider, $i_g(t)$ and the gate voltage $v_g(t)$ and averaging over several periods of operation, $\hat{T}$:

$$C_{eff}^{tun} = \frac{1}{\hat{T}} \int_0^{\hat{T}} \left| \frac{i_g(t)}{dv_g / dt} \right| dt \quad (9)$$

This calculation yields C_{eff}^{tun} = 2.0 fF. Subsequently, an optimization was performed to minimize Δf and it was found that a value of C_{Load} = 2.49 fF satisfies the minimization criterion to within 1%.

It is seen, therefore, that 80% of the capacitive load is due to gate tunneling and only 20% due to traditional gate capacitance.

VI. CONCLUSIONS

As a result of technology scaling, there is degradation in the performance of purely analog circuits due to gate tunneling, as discussed in this paper. An analysis of mixed signal simulations over pure analog simulations for a 45nm voltage controlled oscillator and frequency divider was performed which clearly highlights issues in mixed signal simulations due to the additional leakage mechanism. An approach to equalize the frequency at the outputs of analog and digital blocks is given wherein a capacitive load is added before the digital block. The value of this capacitive load is predominantly determined by leakage considerations and not traditional gate capacitance. In traditional (> 45nm) CMOS designs its effect is minimal but at 45nm and below it rapidly becomes the dominant loading mechanism.

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