A 45*nm* Flash Analog to Digital Converter for Low Voltage High Speed System-on-Chips

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Abstract

In this paper, a 6-*bit* 1 *Gs/sec* flash analog-to-digital converter (ADC) for low voltage and high speed system-on-chip (SoC) applications is presented. Simulated with the 45*nm* Predictive Technology Model, the results demonstrate *INL* < 0.5*LSB*, *DNL* < 0.8*LSB* and a signal to noise and distortion ratio of 31.9*dB*. The Threshold Inverter Quantization (TIQ) technique is used with $W_{PMOS}/W_{NMOS} < 1$ for many transistors to keep the power consumption as low as possible. It is also observed that the ADC consumes 45.42μW of peak power and 8.8μW of average power at full speed while it operates on a power supply voltage of 0.7*V*. To best of the authors' knowledge, this is the first ADC designed at the 45*nm* technology node.

1. Introduction and Motivation

At present, analog to digital converters find applications in communications, TV and HDTV set top boxes, video projectors, etc. ADCs are interfaced with digital circuits in mixed signal chips, where digital signal processing is performed. The supply voltage for digital devices is decreasing rapidly as the technology scales. Analog to digital converters are required to be operating with these devices, preferably at the same voltages. If the analog and digital components on a chip are not operating at the same supply voltage, then level converters need to be incorporated.

There are two issues at hand. One is that the circuit should be able to operate at as low voltage as possible, to minimize the power consumption [ITRS 2003]. The other is that circuit design should be functional at nanometer feature sizes. At such low feature sizes, large device integration is possible. The proposed design meets both criteria.

The contributions of this paper are as follows. We have been able to successfully implement a working flash ADC at 45*nm* technology [Zhao 2006]. The comparators in the flash ADC have been designed using the threshold inverter quantization (TIQ) technique [Yoo 2001, Lee 2002]. While designing these comparators, many transistors have been sized such that $W_{PMOS}/W_{NMOS} < 1$ in order to keep the power consumption as low as possible. The advantage of using these TIQ based comparators over a conventional differential comparator is that a resistor ladder network is not required for providing the reference voltages for the comparators, and the comparison speed is faster. In addition, process matching issues are eliminated. This makes the proposed ADC ideal for use in low power high speed SoCs.

The rest of the paper is organized as follows: Section 2 discusses the related works. Section 3 describes the design of the Flash ADC and its various components. Section 4 discusses the simulation results and characterization of the ADC.

2. Related Research Works

The current literature contains numerous ADC designs. Some selected 6-bit flash ADC versions are discussed below.

In [Yoo 2001, Lee 2002], the TIQ technique has been used to design a flash ADC. In [Uyttenhove 2002], the focus is on low voltage and high speed design, with supply of 1.8*V* and a conversion rate of 1.3 *Gs/sec*. In [Sandner 2005], a capacitive interpolation technique is employed for a low power design which eliminates the need for a resistor ladder. In [Tseng 2004], a complementary average value (CAV) technique has been proposed in which the input signal is pre-processed before comparing it with a fixed voltage reference level in order to simplify the comparator design. The work in [Donovan 2002] presents use of digital techniques instead of analog techniques to overcome comparator offset. In [Scholtens 2002], an average termination circuit is proposed to reduce the number of over-range amplifiers, hence reducing the power consumption. The ADC in [Mehr 1999] is designed for disk-drive read-channel applications. In [Song 2000], the authors use a current interpolating technique to design an ADC operating at 1*V* power supply. In [Uyttenhove 2000], the authors have addressed the problem of meta-stability which becomes important when operating at high sampling speeds. They propose a gray encoded ROM as the solution. In [Srinivas 2006], it has been shown that the static nonlinearity present in the track and hold circuit can be reduced.

Table 1 compares our proposed ADC with the existing ones available in the literature. For fair comparison, only flash type architecture ADC's having a 6-bit resolution have been chosen. It can be seen that while other ADCs consume power in milliwatts, the proposed ADC consumes power in microwatts. The power supply voltage is also the lowest. The design has been carried out at 45*nm* technology, which is the minimum technology currently reported. The values of *DNL, INL* and *SNDR* are also comparable to the ADCs in other literature. The *DNL* is less than 1 *LSB* ensuring that the ADC is monotonic [Maxim 2000].

Table 1: Comparative perspective of existing 6-bit flash ADCs

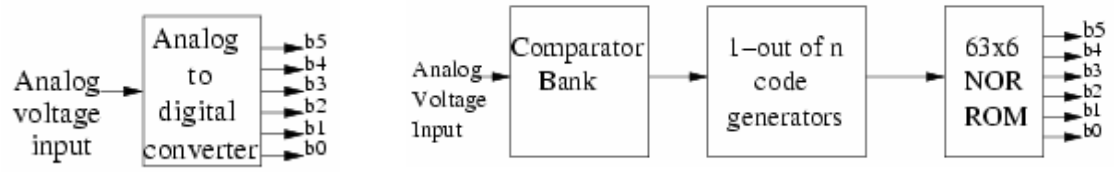
Reference	Resolution (bits)	Technology (nm)	DNL (LSB)	INL (LSB)	SNDR (dB)	VDD (V)	Power (mW)	Samples/ sec.
Choi 2001	6	350	<±0.3	<±0.3	32	3.3	545	1.3G
Donovan 2002	6	250	----	----	33	2.2	150	400M
Geelen 2001	6	350	<0.7	<0.7	5.6(ENOB)	3.3	300	1.1G
Lee 2002	6	250	1.04	0.81	---	2.5	59.91	1.11G
Mehr 1999	6	350	<0.32	<0.2	>5(ENOB)	3.3	225	500M
Sandner 2005	6	130	<0.4	<0.6	32.5	1.5	160	600M
Scholtens 2002	6	180	----	0.42	5.7(ENOB)	1.95	328	1.6G
Song 2000	6	350	-0.6	0.7	33.5	1	10	50M
Srinivas 2006	6	350	0.3	0.3	33.6	3.3	50	160M
Tseng 2004	6	250	<±0.1	<±0.4	32.7	2.5	35	300M
Uyttenhove 2000	6	350	---	---	32	3.3	---	1G
Uyttenhove 2002	6	250	0.42	0.8	32	1.8	600	1.3G
Yoo 2001	6	250	----	----	---	2.5	66.87	1G
This work	**6**	**45**	**0.7**	**0.46**	**31.9**	**0.7**	**45.42μW**	**1G**

3. Design of the Flash ADC

In this section we describe the design of the proposed 45*nm* based ADC. The flash ADC consists of three blocks: (1) comparator bank, (2) 1-out of n code generators, and (3) 63x6 NOR ROM.

3.1 Specifications

Figure 1 shows the black box diagram of a 6-bit analog to digital converter (ADC). It accepts an analog input such as voltage or current and gives out an n-bit binary number as the output. The flash ADC is the preferred architecture to choose when one is designing a high speed low resolution ADC. The ADC has been designed to meet the specifications shown in Table 2, where V_{LSB} is the quantization step.



(a) Block diagram of 6-bit ADC (b) Block diagram of 6-bit flash ADC

Figure 1. Schematic representation of Analog to digital converter

Table 2: Specifications of the 45*nm* Flash ADC

Parameter	Specification
Resolution	6-bit
Architecture	Flash
Power Supply	0.7V
V_{LSB}	500µV

3.2 Design Approach

The design of an n-bit flash ADC requires the design of 2^n – 1comparators, 1-out of n code generators and a 2^n – 1xn NOR ROM. As shown in figure 2, for a 3-bit ADC design we need 7 comparators, 1-out of 7 code generators and a 7x3 NOR ROM. Similarly, for a 6 bit ADC, we designed 63 TIQ based comparators, 1-out of 63 code generators and 63x6 NOR ROM. As discussed earlier, the TIQ based technique does not require a resistive ladder circuit like a conventional flash ADC circuit, because the switching voltages for the TIQ comparators are determined by the sizes of the PMOS and NMOS transistors in the comparator. Hence the design is much simpler, faster and suitable for low power, low voltage and high speed SoCs.

Figure 2 shows the circuit diagram for a 3-bit flash ADC based on the TIQ technique. Each of the comparators is designed to switch at a specific reference voltage. We need 2^3-1 comparators. As the input analog voltage increases, the comparators start turning on in succession, from comparator 0 (COMP_0) to comparator 6 (COMP_6). Thus, we get a thermometer code at the output of the comparators. The point where the code changes from one to zero is the point where the input signal becomes smaller than the respective comparator reference voltage levels. This is known as thermometer code encoding, so named because it is similar to a mercury thermometer, where the mercury column rises to the appropriate temperature and no mercury is present above that temperature. The thermometer code is converted to a binary code in two steps. First, the thermometer code is converted into a 1-out of n code using the 1-out of n code generators. This code is subsequently converted to binary code using a NOR ROM. Therefore the input analog voltage is represented by a binary code at the output.

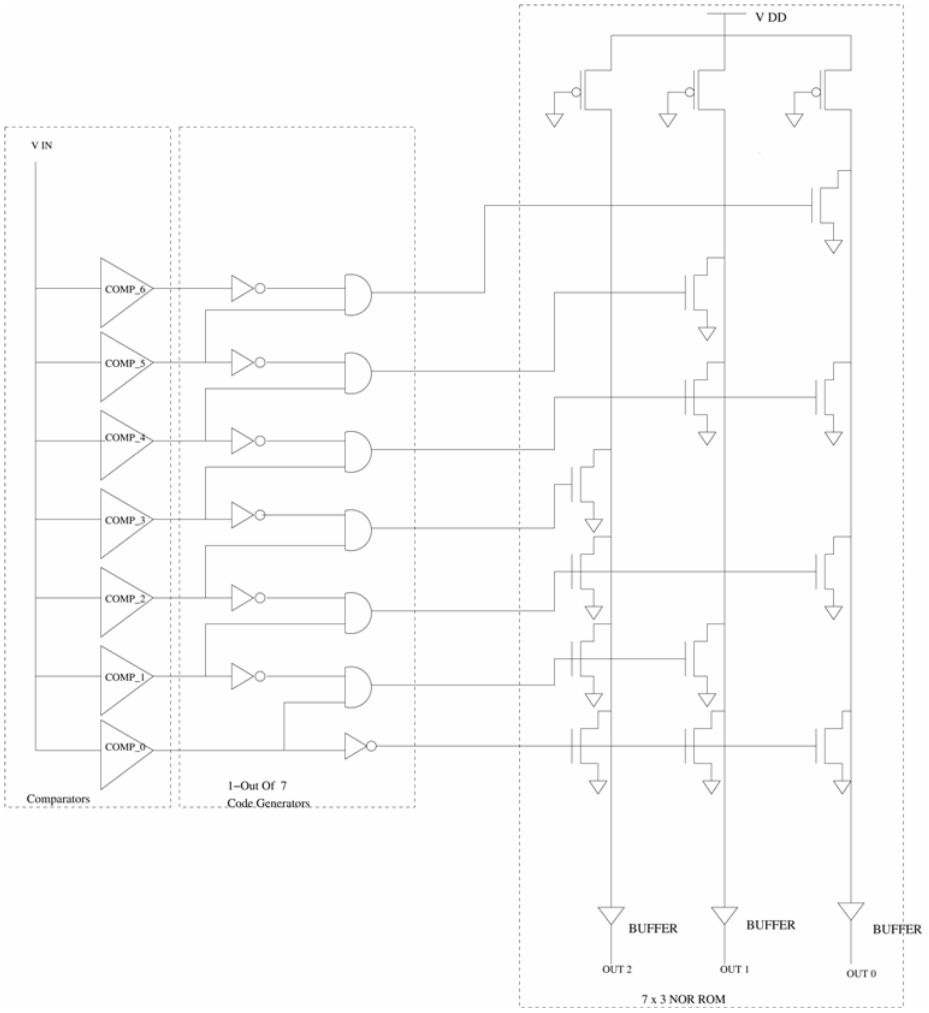


Figure 2. Circuit design of a 3-bit flash ADC (We carried out a 6-bit ADC design which has similar structure, but 3-bit has been shown for brevity.)

3.3 Design of the TIQ Comparator

The TIQ comparator circuit consists of four cascaded inverters, as shown in figure 3. There are four inverters in cascade in order to provide a sharper switching for the comparator and also provide a full voltage swing. The sizes of the PMOS and NMOS transistors in a comparator are the same, but they are different for different comparators. They depend upon the switching voltage they are designed for. The mathematical expression used for deciding these switching voltages is given as [Rabaey 2003, Segura 1998]:

$$Vswitching = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}(V_{DD} - |V_{tp}|) + V_{tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}} \quad , \quad \ldots \quad \ldots. \qquad (1)$$

where, Wp = PMOS width, Wn = NMOS width, V_{DD} = supply voltage, Vtn = NMOS threshold voltage, Vtp = PMOS threshold voltage, μ_n = electron mobility, μ_p = hole mobility, assuming that PMOS length = NMOS length.

The sizes of the NMOS and PMOS transistors used in the proposed ADC corresponding to the minimum and maximum switching voltages are shown in Table 3. For determining these sizes of the PMOS and NMOS transistors in the comparator, we used a DC parametric sweep. The DC voltage was varied from 0 to $0.7V$ in steps of $500\mu V$ with NMOS transistors having W/L=90nm/90nm. The length of PMOS transistor was also kept at 90nm, and the width was given a parametric sweep. We were thus able to obtain 63 switching voltage levels as shown in figure 4.

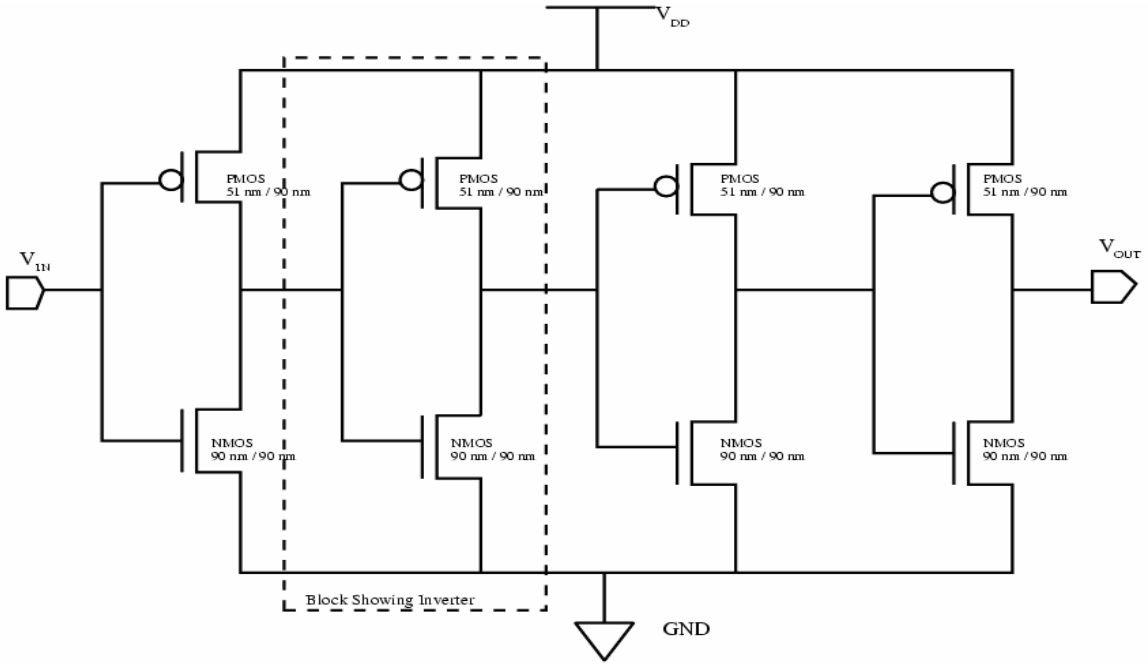


Figure 3. Four cascaded inverters form a TIQ comparator. The sizes of PMOS and NMOS in a comparator are the same, but they are different for 63 different comparators of the 6-bit ADC.

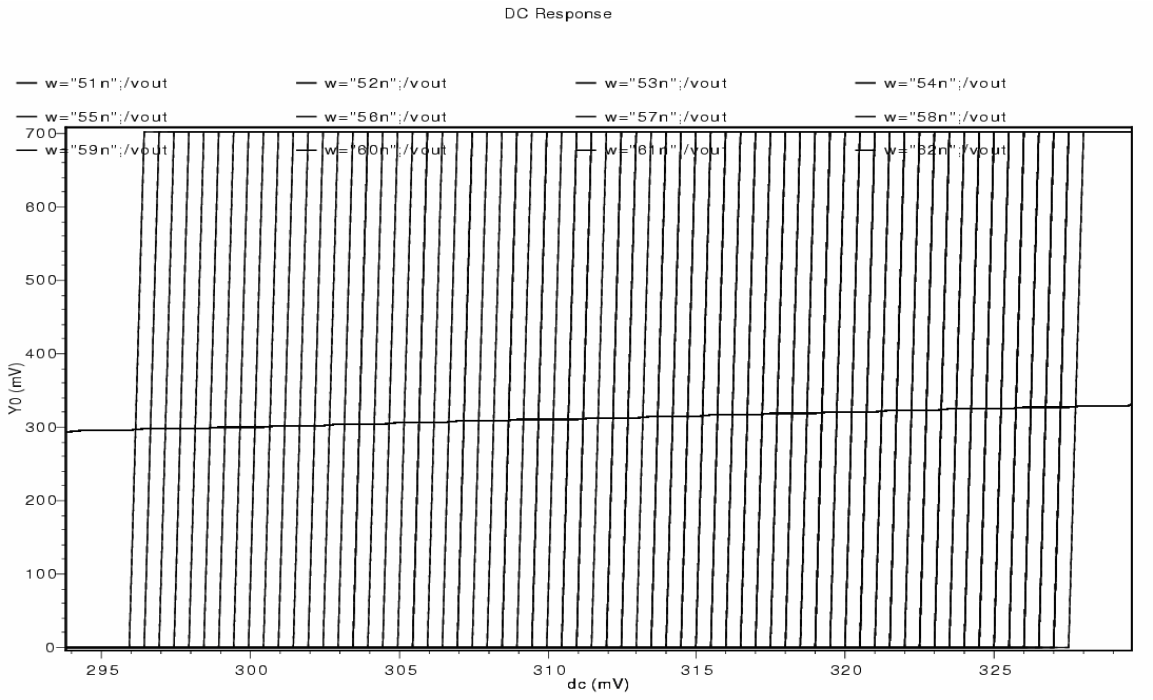


Figure 4. DC Sweep for determining the sizes of transistors in the TIQ Comparator

Table 3. Sizes of the transistors for maximum and minimum switching voltages

Value of Comparator switching Voltage	W/L of Transistors	
296.3*mV* (minimum)	PMOS = 51*nm*/90*nm*	NMOS = 90*nm*/90*nm*
327.8*mV* (maximum)	PMOS = 163*nm*/90*nm*	NMOS = 90*nm*/90*nm*

3.4 Design of the Encoder

The output of the comparators in a flash ADC is a thermometer code. This thermometer code is converted to a binary code using an encoder in two steps. The thermometer code is first converted into a 1-out-of-n code [Yoo2001] using 1-out of n code generators, which generates a '01' code. This '01' code is converted into a binary code using a NOR ROM. A NOR ROM consists of PMOS pull-up and NMOS pull-down devices [Rabaey 2003]. The PMOS and NMOS sizes for the NOR ROM are 75*nm*/90*nm* (W/L) and 90*nm*/90*nm*, respectively. We have taken $W_{PMOS} < W_{NMOS}$ to achieve a good voltage swing [Rabaey 2003], because a NOR ROM consists of pseudo NMOS NOR gates put together. The logic is that the pull-up transistor (PMOS) should be narrow enough so that the pull-down devices (NMOS) can still pull down the output safely.

4. Simulation and Characterization Results

This section discusses functional simulations of the flash ADC and its characterization to verify that it is suitable for high speed, low voltage applications. The design and characterization were done in the Cadence Analog Design Environment.

4.1 Functional Simulation

A transient analysis of the ADC was performed. A ramp was generated, going from 296.3*mV* to 327.8*mV* (which is the full scale range of the ADC). The digital codes were obtained correctly, going from 0 to 63 at the output, indicating that the ADC was functionally correct. The simulation results are shown in figure 5.

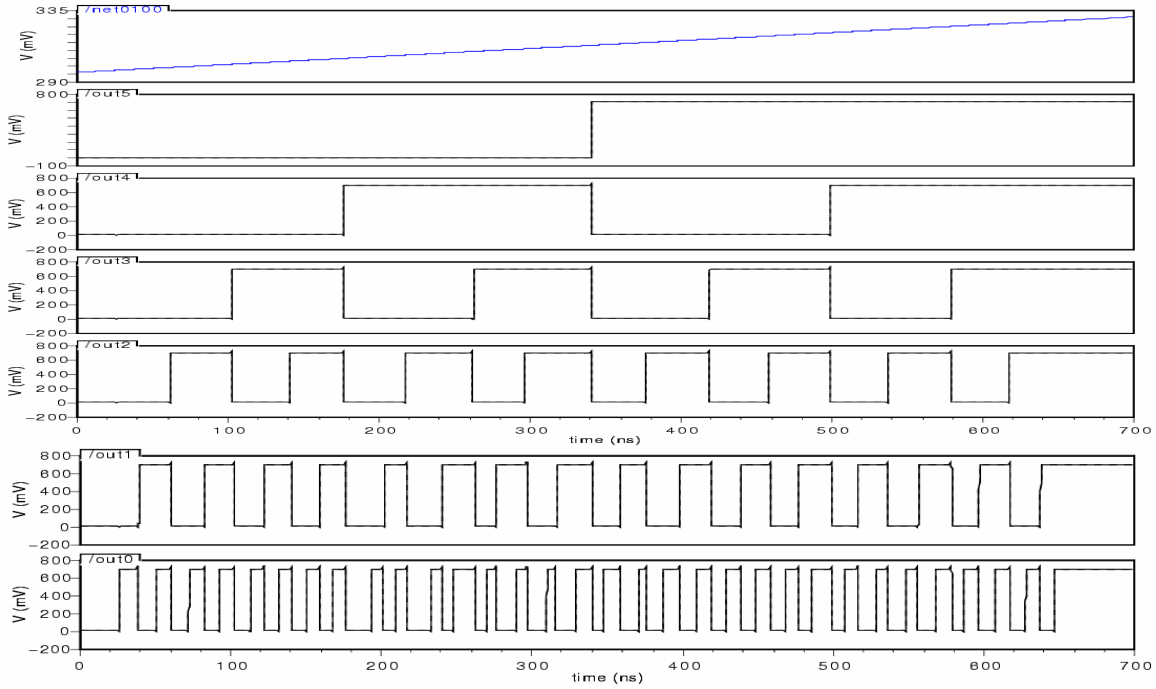


Figure 5. Transient analysis of the flash ADC to prove the functional correctness

4.2 Characterization

The proposed flash ADC has been characterized for the differential non-linearity (*DNL*), integral non-linearity (*INL*) and the signal to noise and distortion ratio (*SNDR*).

4.2.1 Differential Non-Linearity (DNL)

A Verilog-A block has been used to test the *DNL*. The Verilog-A block generates a slowly varying *full scale range* ramp to be given as input to the flash ADC, which completes the full scale range in 4096 steps. The flash ADC has 64 codes, so ideally there should be 64 hits per code. But for the transistor level implementation, this is typically not the case. The number of hits per code is recorded, and the *DNL* is calculated from that. The results show that the ADC exhibits a maximum *DNL* of 0.70*LSB*, which is within the acceptable limits. The *DNL* plot is shown in figure 6. A DNL error specification of less than or equal to 1*LSB* guarantees a monotonic transfer function with no missing codes. An ADC's monotonicity is guaranteed when its digital output increases (or remains constant) [Maxim 2000] with an increasing input signal, thereby avoiding sign changes in the slope of the transfer curve. The DNL is calculated from the formula:

$$DNL = \left| \frac{V_{D+1} - V_D}{V_{LSB-IDEAL}} - 1 \right| LSB, \qquad \ldots \quad \ldots \qquad (2)$$

where V_D is the analog value corresponding to the digital output code D, and $V_{LSB\text{-}IDEAL}$ is the ideal spacing for two adjacent digital codes. For an ideal ADC, DNL = 0*LSB*.

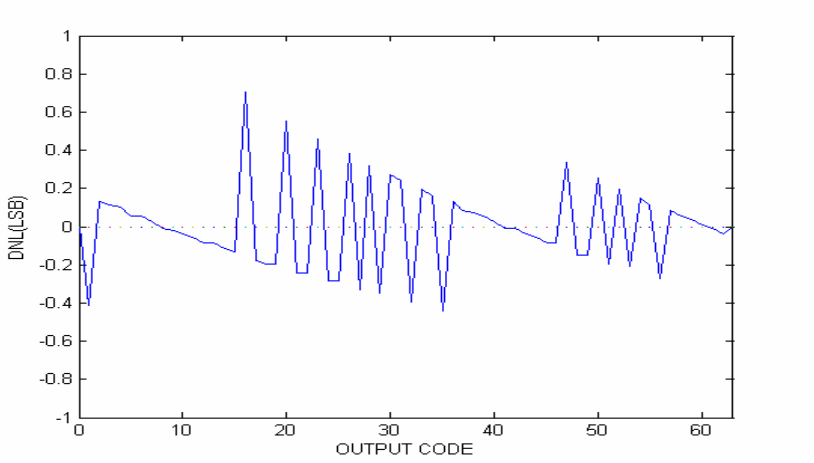


Figure 6. DNL plot of the flash ADC

4.2.2 Integral Non-Linearity (INL)

Similar to DNL, a Verilog-A block has been used to test the *INL* that generates a slowly varying *full scale range* ramp to be given as input to the flash ADC in 4096 steps. The *INL* is calculated from the number of hits per code, of course ideally there should be 64 hits per code. The results show that the ADC exhibits a maximum *INL* of 0.46*LSB*. The *INL* plot is shown in figure 7. The INL is calculated from the formula [Maxim 2000]:

$$INL = \left| \frac{V_D - V_{ZERO}}{V_{LSB-IDEAL}} - D \right| LSB, \qquad \ldots \quad \ldots \qquad (3)$$

where V_D is the analog value represented by the digital output code D, V_{ZERO} is the minimum analog input corresponding to an all-zero output code, and $V_{LSB\text{-}IDEAL}$ is the ideal spacing for two adjacent output codes.

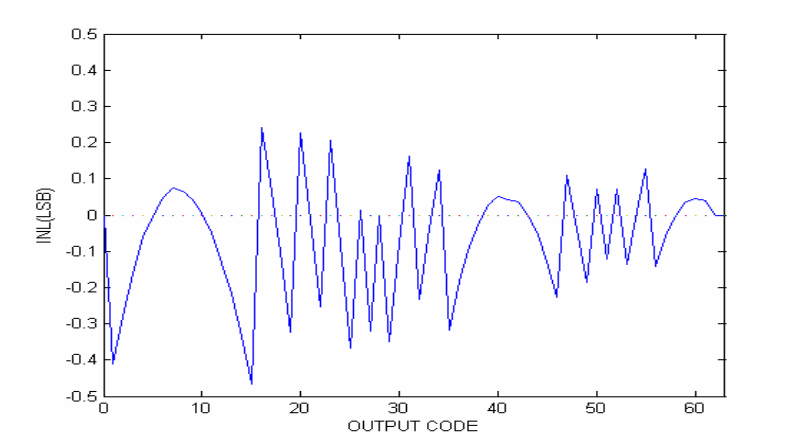


Figure 7. INL plot of the flash ADC

4.2.3 Signal to Noise and Distortion Ratio (SNDR)

The ideal formula for *SNDR* calculation for an ADC is [Maxim 2001]:

$$SNDR = 20 * \log_{10}\left(\frac{A_{RMS,Signal}}{A_{RMS,noise+harmonics}}\right) dB \quad \text{..... ... .} \quad (4)$$

where $A_{RMS,signal}$ and $A_{RMS,noise+harmonics}$ are the root mean square (RMS) amplitude for the signal and the noise, respectively. Here, signal means the fundamental amplitude signal, and the noise includes the significant harmonics, which are usually from the second to the fifth highest amplitudes. The signal to noise and distortion ratio *(SNDR)* of the designed ADC has been measured at an input frequency of 500*KHz*. The Flash ADC is fed a sinusoidal input (frequency: 500*KHz*) which covers the entire *full scale range*, and the output of the ADC if fed to an ideal digital to analog converter (DAC, modeled as a Verilog-A block). Thus, the output of the DAC is a reconstructed, digitized sine wave, at 500*KHz*. The FFT of this sine wave is plotted, from which the *SNDR* is calculated. The *SNDR* was found to be 31.9*dB*. The FFT plot is shown in figure 8. Figure 9 shows the power plot of the flash ADC. From the plot, we observe that peak power of 45.42μW and average power of 8.8μW is consumed.

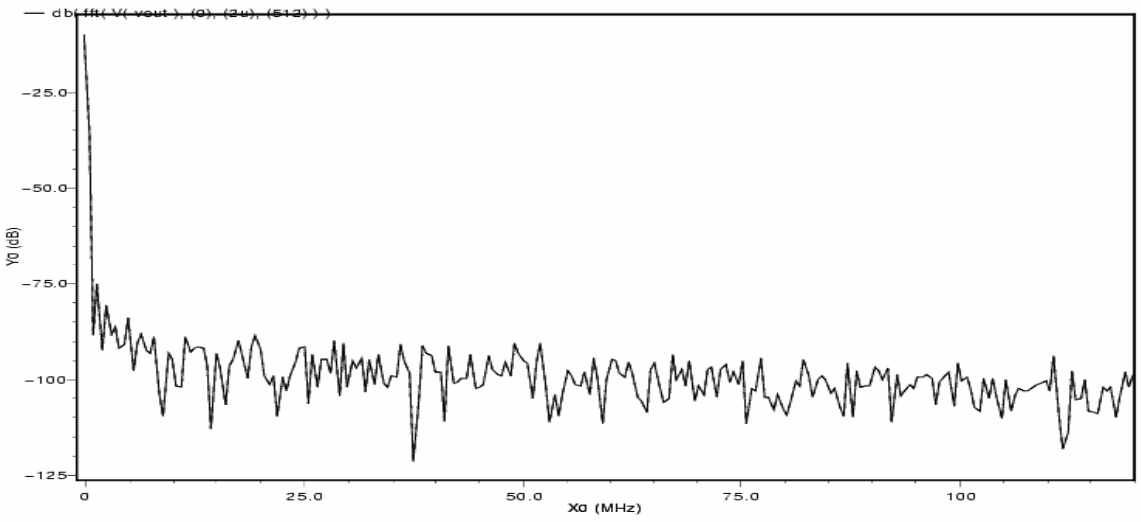


Figure 8. FFT plot of the flash ADC at input sine wave having frequency 500*KHz* (*SNDR* calculation from this plot)

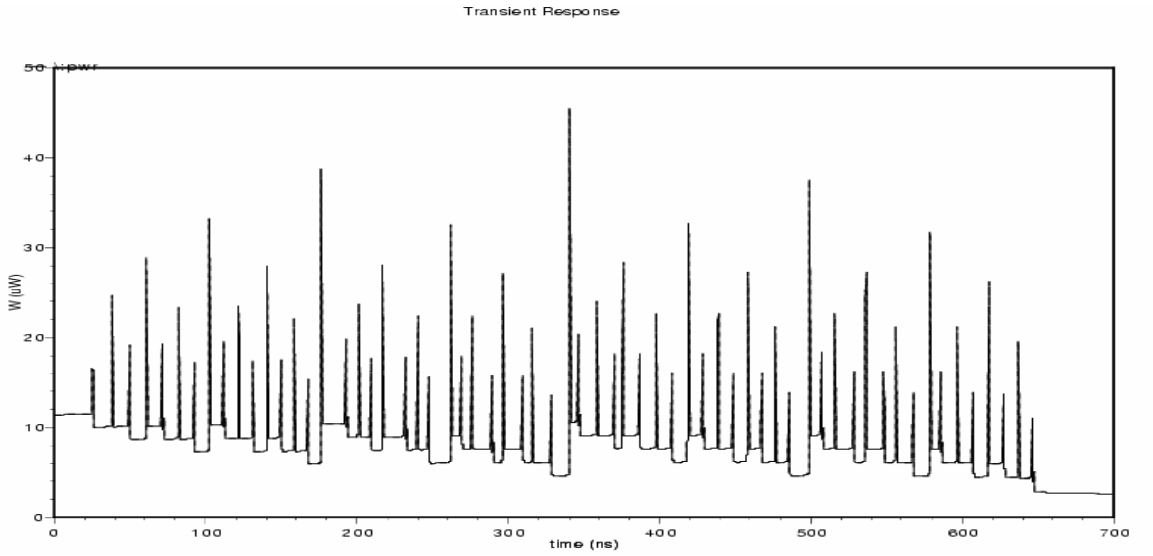


Figure 9. Instantaneous power plot of the flash ADC

5. Conclusion and Future Works

The design and simulation results of a 6-*bit* flash ADC using the 45*nm* Predictive Technology Model has been presented. The design is suitable for low voltages (0.7*V* supply) and high speed (1 *Gs/sec*) SoC applications. The maximum *DNL* and *INL* measured were 0.70*LSB* and 0.46*LSB* respectively, and the *SNDR* was calculated to be 31.9*dB*. The ADC consumes a peak power of 45.42μW and an average power of 8.8μW. Thus, we have successfully designed an ADC which is functional at nanoscale CMOS technologies. The layout of 45*nm* technology based design is under progress. We have completed a layout for a 90*nm* process. We then plan to scale the rules for 45*nm* and perform the 45*nm* layout.

References

[Choi 2001] M. Choi and A. Abidi, "A 6-b 1.3GSamples/s A/D Converter in 0.35µm CMOS", in *Proceedings of the International Solid State Circuits Conference*, pages 126-127, 2001.

[Donovan 2002] C. Donovan and M. P. Flynn, "A Digital 6-bit ADC in 0.25µm CMOS", *IEEE Journal of Solid State Circuits,* vol. 37, no. 3, pages 432-437, March 2002.

[Geelen 2001] G. Geelen , "A 6-b 1.1GSamples/s CMOS A/D Converter ", in *Proceedings of the International Solid State Circuits Conference*, pages 127-128, 2001.

[ITRS 2003] Semiconductor Industry Association, International Technology Roadmap for Semiconductors. http://public.itrs.net.

[Lee 2002] D. Lee, J. Yoo, and K. Choi, "Design Method and Automation of Comparator Generation for Flash A/D Converter", in *Proceedings of the International Symposium on Quality Electronic Design (ISQED),* pages 138-142, 2002.

[Maxim 2000] Maxim Integrated Products, INL/DNL Measurements for High-Speed Analog to-Digital Converters (ADCs).

[Maxim 2001] Maxim Integrated Products. Defining and Testing Dynamic Parameters in High-Speed ADCs, 2001.

[Mehr 1999] I. Mehr and D. Dalton, "A 500MSample/s, 6-bit Nyquist Rate ADC for Disk-Drive Read-Channel Applications", *IEEE Journal of Solid State Circuits*, vol. 34, no. 7, pages 912-920, July 1999.

[Rabaey 2003] J. M. Rabaey, A. Chandrakasan, and B. Nikolic′, "Digital Integrated Circuits", 2nd Edition, 2003.

[Sandner 2005] C. Sandner, M. Clara, A. Santner, T. Hartig, and F. Kuttner, "A 6-bit 1.2GS/s Low-Power Flash ADC in 0.13μm Digital CMOS", *IEEE Journal of Solid State Circuits*, Vol. 40, no.7, pages 1499-1505, July 2005.

[Scholtens 2002] P.C.S. Scholtens, and M. Vertregt, "A 6b 1.6 Gsample/s Flash ADC in 0.18μm CMOS Using Averaging Termination", *IEEE Journal of Solid State Circuits*, vol. 37, no. 12, pages 1599-1609, December 2002.

[Segura 1998] J. Segura, J. L. Rossello, J. Morra, and H. Sigg, "A Variable Threshold Voltage Inverter for CMOS Programmable Logic Circuits", *IEEE Journal of Solid-State Circuits*, vol. 33, no. 8, pages 1262-1265, August 1998.

[Song 2000] B.S. Song, P.L. Rakers, and S.F. Gillig, "A 1-V 6-b 50MSamples/s Current-Interpolating CMOS ADC", *IEEE Journal of Solid State Circuits*, vol. 35, no. 4, pages 647-651, April 2000.

[Srinivas 2006] V. Srinivas, S. Pavan, A. Lachhwani, and N. Sasidhar, "A Distortion Compensating Flash Analog-to-Digital Converter", *IEEE Journal of Solid State Circuits*, vol. 41, no. 9, pages 1959-1969, September 2006.

[Tseng 2004] H.C. Tseng , C. Lin, H. Ou, and B. Liu, "A Low-Power Rail-to-Rail 6-bit Flash ADC based on a Novel Complementary Average-Value Approach", in *Proceedings of the International Symposium on Low Power Electronics and Design (ISLPED),* pages 252-256, 2004.

[Uyttenhove 2000] K. Uyttenhove, A. Marques, and M. Steyaert, "A 6-bit 1GHz Acquisition Speed CMOS Flash ADC with Digital Error Correction", in *Proceedings of the Custom Integrated Circuits Conference,* pages 249-252, 2000.

[Uyttenhove 2002] K. Uyttenhove and M. Steyaert, "A 1.8V, 6-bit, 1.3 GHz CMOS Flash ADC in 0.25μm CMOS", in *Proceedings of the European Solid-State Circuits Conference*, pages 455-458, 2002.

[Yoo 2001] J. Yoo, K. Choi and A. Tangel, "A 1-GSPS CMOS Flash A/D Converter for System on-Chip Applications", in *Proceedings of the IEEE Computer Society Workshop on VLSI*, pages 135-39, 2001.

[Zhao 2006] W. Zhao and Y. Cao, "New Generation of Predictive Technology Model for sub-45nm Design Exploration", in *Proceedings of the International Symposium on Quality Electronic Design (ISQED)*, pages 585-590, 2006.