# Effective Tunneling Capacitance: A New Metric to Quantify Transient Gate Leakage Current

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***Abstract*— In this paper we propose a new metric called "effective tunneling capacitance" ($C^t_{eff}$) to quantify the transient swing in the gate leakage (gate oxide tunneling) current due to state transitions. $C^t_{eff}$, which is defined as the change in tunneling current with respect to the rate of change of input voltage is a unique metric and to our knowledge proposed here for the first time. This metric concisely encapsulates information about the swing in tunneling current during state transitions while simultaneously accounting for the transition rate and represents the capacitive load of the transistor due to tunneling. This capacitance can have impact on transistor characteristics being additive to its gate oxide and diffusion capacitances. We express $C^t_{eff}$ as functions of gate oxide thickness $T_{ox}$ and on-chip power supply $V_{DD}$ to make it useful for modeling in higher levels of design abstraction. We also statistically analyze the effects of process variations of $T_{ox}$ and $V_{DD}$ on its distribution.**

## I. Introduction

According to the ITRS roadmap, high performance CMOS circuits will require very low gate oxide thicknesses due to aggressive technology scaling [1]. Such ultra-thin oxide devices will be susceptible to new leakage mechanisms due to direct tunneling of charge carriers through gate oxide, which leads to gate oxide tunneling (gate leakage) current ($I_{ox}$) [2]. The gate oxide tunneling current is strongly dependent on the supply voltage of the transistor $V_{DD}$ and gate $SiO_2$ thickness $T_{ox}$ [3], [4]. It is projected that the gate leakage current will be a major component of the static power consumption and hence of the total power consumption of a low-end nanotechnology CMOS device. Thus, there is a critical need for analysis, explanation, and characterization of the various tunneling mechanisms, targeted towards design for manufacturing (DFM) and process variation modeling.

There are several research works available in the current literature that model and characterize the gate oxide tunneling current. In [5] a total leakage analysis method is proposed including gate tunneling. Authors in [6] study the effect of gate tunneling current in MOS devices of length of $25nm$ and $90nm$ using device simulation. An approach for modeling and analysis of gate-to-channel leakage in different DGFET structures is presented in [7]. In [8], analytical models are proposed to estimate the mean and the standard deviation in variation of different leakage components. A methodology for estimating the total amount of gate-tunneling current in CMOS combinatorial circuits is presented in [9].

We observe that none of the above currently available works investigate the transient behavior of the gate tunneling current; they only address steady-state conditions. We will demonstrate that current during state transitions is significant and comparable to ON and OFF state currents. We also observe that some of the above works do not consider the effect of both ON and OFF state gate oxide tunneling current. The contributions of the research work presented in this paper are as follows: We analyzed in detail the behavior of the CMOS device during its entire cycle of its operation. Guided by the results of the previous analysis and using additional simulations, we defined a novel metric $C^t_{eff}$, appropriate for a complete characterization of the gate oxide tunneling current of a CMOS transistor and its impact on device operation as far as leakage and capacitive effects are concerned. We studied the dependence of the metric on process parameter $T_{ox}$ and design parameter $V_{DD}$. Finally, we performed Monte Carlo simulations that clearly indicate that small process and power supply variations can have significant impact on $C^t_{eff}$ and consequently on the transistor's power and performance profile.

## II. Dynamics of Gate Oxide Tunneling

Here we discuss the physical mechanism of gate oxide tunneling with the help of an nanoscale NMOS transistor.

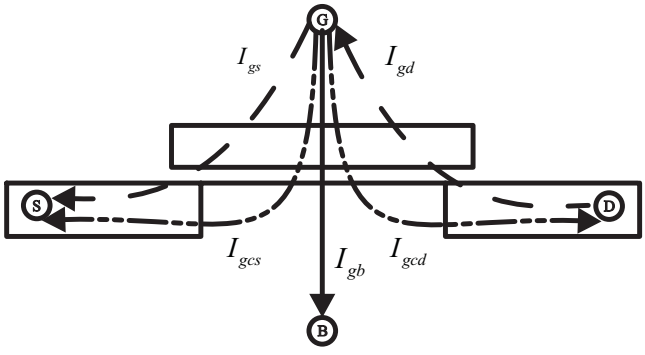



Fig. 1. Gate oxide tunneling current ($I_{ox}$) components in BSIM4.4.0 model.

### A. Tunneling Current SPICE Modeling

Fig. 1 identifies the various components of the gate tunneling current ($I_{ox}$), such as gate-to-diffusion ($I_{gs}$ and $I_{gd}$), gate-to-channel ($I_{gcs}$ and $I_{gcd}$) and gate-to-substrate ($I_{gb}$) currents, as modeled by the BSIM4 model. Since the objective of this work is to analyze the effect of these currents in future nanoCMOS technologies, especially in the $65nm$, $45nm$ and beyond range, no commercially available process data could be used. It is, however, expected that the Berkeley Predictive Technology Model (BPTM) [10] accounts for these effects correctly.

The BPTM model used in this work is for a $45nm$ NMOS device with $T_{ox} = 1.4nm$, threshold voltage $V_{Th} = 0.22V$, and $V_{DD} = 0.7V$. The width of the device was chosen to be very large ($W = 1\mu m$), thus eliminating any width-modulation effects in our analysis. Since we concentrate on the behavior of a single device and not a logic gate, no capacitive or resistive load was connected to the output. Cadence Design Systems' Analog Design Environment and Spectre circuit simulator are used [11].

### B. Tunneling Current Physical Mechanism

We now study the physical mechanism of the gate oxide tunneling in a CMOS transistor. We identify the regions of operations of a MOS device distinguishing its transient and steady states. We also provide physical explanation of the MOS transistor behavior during those states. From Fig. 2(a) and 2(b) we can identify distinct regions of operation of the transistor during a typical switching cycle: (i) steady-state region (ON and OFF), (ii) transition region [low-to-high (LH) and high-to-low (HL)].

It is evident that different mechanisms contribute to the overall current during different phases of the switching cycle. In the following discussion we refer to Fig. 3 which identifies the components active during each region of operation.

(i) *Steady-State*: In the steady-state OFF region (Fig. 3(a)), both gate and source are at ground while the drain is at high ($V_{DD}$) voltage. Since no channel is formed in this condition, the only active component is $I_{gd}$, due to the overlap of the drain diffusion and the gate. On the other hand, in the steady-state ON region (Fig. 3(b)), both gate and drain are held at high with the source being grounded. A well-formed channel exists in this case and three separate components are active: (i) $I_{gs}$ due to the overlap of the source diffusion with the gate, (ii) $I_{gcs}$ due to the flow of current from gate to the inversion layer in the channel and subsequently to the source, and (iii) $I_{gcd}$ due to the flow of current from gate to the channel and subsequent collection at the drain. The component $I_{gd}$ has been extinguished due to the almost zero electric field in that region of the oxide.

(ii) *Transient State*: Finally, during the LH and HL transitions, all four components become active as shown quantitatively in Fig. 2(b) and qualitatively in Fig. 3(c). In this case the source is at ground, the drain is at $V_{DD}$ and the gate is switched from low to high or high to low. In the LH transition, the channel gradually forms from source to drain and the components $I_{gs}$, $I_{gcs}$ and $I_{gcd}$ start becoming significant, in that order. Conversely, as the field across the oxide region over the drain is reduced, $I_{gd}$ is decreasing to almost total extinction. The situation is reversed in the HL transition.

## III. The Effective Tunneling Capacitance ($C^t_{eff}$)

It is apparent that the behavior of the device in terms of gate tunneling leakage current must be characterized not only during the steady-state but also during low-to-high (LH) and high-to-low (HL) transitions. Moreover, the OFF state current is comparable in magnitude to the ON state current and hence is a major source of leakage which needs to be accounted for in any characterization effort. The situation is more complex during the LH and HL transitions. In order to provide a meaningful metric during this transition period, we need to account for the change in magnitude and direction of the total gate tunneling current and also consider the time in which this transition takes effect.

Therefore, we define a new metric called effective tunneling capacitance as:

$$C^t_{eff} = \left| \frac{I_{ON} - I_{OFF}}{dV_g/dt} \right|, \tag{1}$$

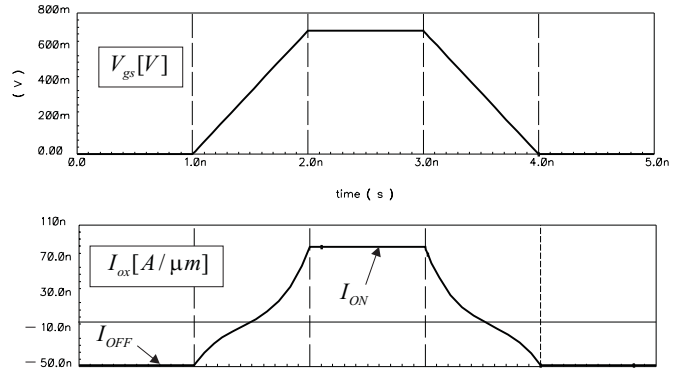
where $V_g$ is the voltage applied on the gate. For simplicity we can assume that the rise ($t_r$) and fall ($t_f$) times of the gate input voltage are equal which makes the two transition regions symmetric with respect to their behavior during switching. When the rise and fall times are identical, this simplifies to:

$$C^t_{eff} = \frac{|I_{ON} - I_{OFF}|}{V_{DD}} t_r. \tag{2}$$

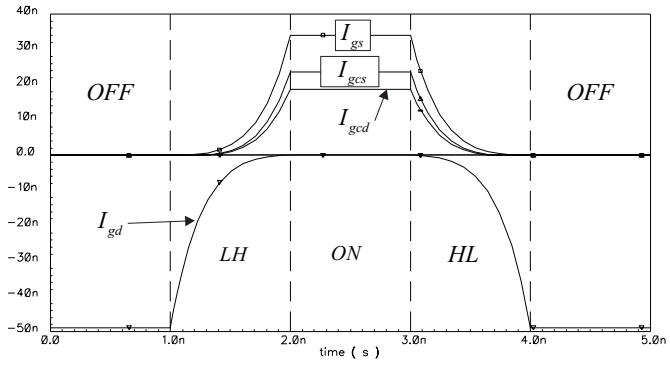
The metrics $C^t_{eff}$ along with $I_{ON}$ and $I_{OFF}$ provide a concise and complete mechanism for characterizing the gate tunneling leakage during the entire operational cycle of a MOS. We believe that $C^t_{eff}$ contains valuable information not only for the switching operation of the device but also for capacitive loading effects due to gate tunneling leakage as well as reliability studies since it can be directly related to transient charge flow through the gate oxide. This capacitance can have impact on a nanoscale MOS transistor's power and performance characteristics, similar to the parasitic capacitances, such as gate oxide capacitance and diffusion capacitance. All the capacitances, such as the proposed effective tunneling capacitance ($C^t_{eff}$), gate capacitance and diffusion capacitance will be additive, thus increasing the loading effect of the MOS transistor with direct consequences on the fan-out of logic gates.

## IV. Modeling for Process and Supply Variation

In Figs. 4(a) and 4(b) we show the dependence of the relevant metrics ($C^t_{eff}$, $I_{ON}$ and $I_{OFF}$) on process ($T_{ox}$) and design variation ($V_{DD}$.) We subsequently performed a least squares fit of the data presented in these figures to study the effects of $T_{ox}$ and $V_{DD}$. The fitting functions may in turn be




(a) $I_{ox}$ for a test input pulse. The rise and fall times of the input pulse are $t_r = t_f = 1ns$.




(b) $I_{ox}$ components. $I_{gs}$, $I_{gcs}$ and $I_{gcd}$are positive i. e. from the gate. $I_{gd}$ is negative i. e. towards the gate. $I_{gb}$ is negligible and is not shown.

Fig. 2. Tunneling current components during the switching operation of the transistor from the OFF to the ON state and then back to the OFF state.

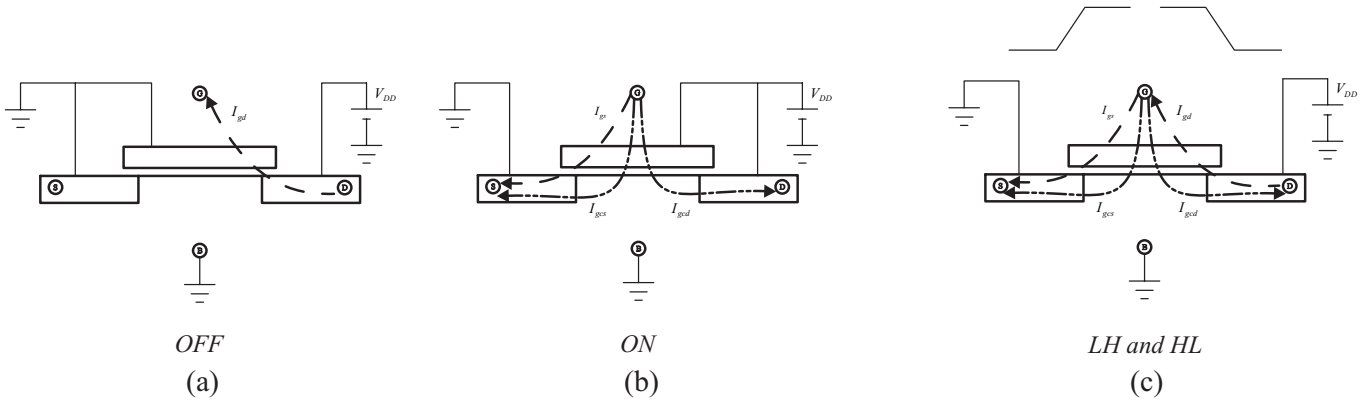
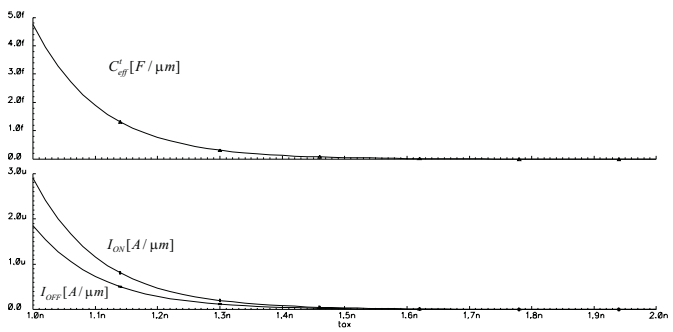
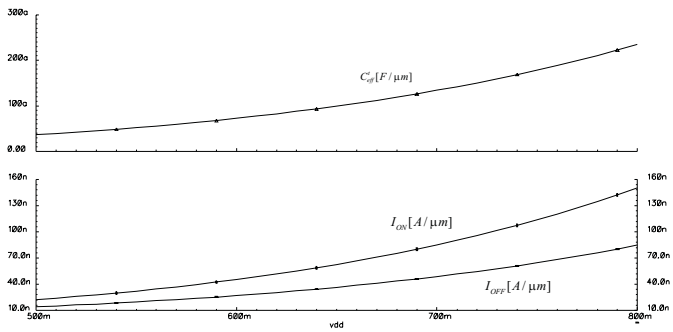



Fig. 3. Gate tunneling current component flow in the various regions of operation of an NMOS. $I_{gb}$ is negligible and not shown.




(a) Dependence on $T_{ox}$. The power supply is held fixed at $V_{DD} = 0.7V$.




(b) Dependence on $V_{DD}$. The oxide thickness is held fixed at $T_{ox} = 1.4nm$.

Fig. 4. Dependence of Effective Tunneling Capacitance ($C^t_{eff}$), Steady-State ON ($I_{ON}$) and Steady-State OFF ($I_{OFF}$) currents on oxide thickness ($T_{ox}$) and power supply ($V_{DD}$).

useful for modeling in higher levels of design abstraction, such as logic level and RTL level. The results are shown in Table I.

### A. Modeling for $T_{ox}$ Variation

The effect of varying oxide thickness ($T_{ox}$) was incorporated by varying the parameter $TOXE$ in the spice model deck directly. Initially, we held the power supply fixed at $V_{DD} = 0.7V$ and varied the oxide thickness from $T_{ox} = 1nm$ to $T_{ox} = 2nm$. From the Table I we observe that all metrics follow the theoretically expected variation very well as evidenced by the high correlation coefficient of the fit $(100\%)$.

### B. Modeling for $V_{DD}$ Variation

In this case, we held $T_{ox}$ to a nominal value of $1.4nm$, appropriate for a $45nm$ CMOS technology and investigated the dependence of the currents and $C^t_{eff}$ on power supply variation. Similarly, Table I indicates an almost perfect fit of the metrics to the theoretically expected form with a cross-correlation coefficient of $100\%$. It may be pointed out that the

TABLE I

CURVE FITTING USING DIFFERENT FUNCTIONS

| Variation | Metrics | Fitting Functions | Function Parameters | Corr. Coefficients |
|---|---|---|---|---|
| Process Parameter ($T_{ox}$) | $C^t_{eff}$ vs. $T_{ox}$ | $C^t_{eff} = \left(\frac{\alpha}{T^2_{ox}}\right) e^{(-\beta T_{ox})}$ | $\alpha = 6.86 \times 10^{-30}$ and $\beta = 7.2 \times 10^9$ | 100% |
| | $I_{ON}$ vs. $T_{ox}$ | $I_{ON} = \left(\frac{\alpha}{T^2_{ox}}\right) e^{(-\beta T_{ox})}$ | $\alpha = 3.89 \times 10^{-21}$ and $\beta = 7.2 \times 10^9$ | 99.9% |
| | $I_{OFF}$ vs. $T_{ox}$ | $I_{OFF} = \left(\frac{\alpha}{T^2_{ox}}\right) e^{(-\beta T_{ox})}$ | $\alpha = 2.55 \times 10^{-21}$ and $\beta = 7.2 \times 10^9$ | 99.9% |
| Design Parameter ($V_{DD}$) | $C^t_{eff}$ vs. $V_{DD}$ | $C^t_{eff} = (\alpha V_{DD})\, e^{\left(-\frac{\beta}{V_{DD}}\right)}$ | $\alpha = 1.78 \times 10^{-15}$ and $\beta = 1.29$ | 100% |
| | $I_{ON}$ vs. $V_{DD}$ | $I_{ON} = (\alpha V_{DD})\, e^{\left(-\frac{\beta}{V_{DD}}\right)}$ | $\alpha = 1.19 \times 10^{-6}$ and $\beta = 1.29$ | 99.5% |
| | $I_{OFF}$ vs. $V_{DD}$ | $I_{OFF} = (\alpha V_{DD})\, e^{\left(-\frac{\beta}{V_{DD}}\right)}$ | $\alpha = 6.43 \times 10^{-7}$ and $\beta = 1.29$ | 99.5% |

fitting factors $\alpha$ and $\beta$ for the metrics are different for the $T_{ox}$ and $V_{DD}$ fits. This demonstrates that the impact of $T_{ox}$ variation and $V_{DD}$ variation on them is different.

### C. Statistical Distribution of $C^t_{eff}$

Our ultimate objective in determining a functional relationship between the metric, $T_{ox}$ and $V_{DD}$ is to translate statistical information for the distributions of $T_{ox}$ and $V_{DD}$ to statistical information about the metric $C^t_{eff}$. We performed a statistical characterization of the devices using a Monte Carlo approach. In this method, we assume that the statistical distribution of process (represented by $T_{ox}$) and on-chip power supply factors (represented by $V_{DD}$) is known. For both variables we use a normal distribution with standard deviation ($\sigma$) equal to 10% of the mean ($\mu$). The mean value for $T_{ox}$ was $1.4nm$ and for $V_{DD}$ was $0.7V$. These results indicate that even though approximately 65% of the metrics follow the mean very closely, a significant number of them fall within the range from $2\sigma$ to $3\sigma$ of the mean. In addition, the distribution is lognormal with a strongly exponential shape and the $\sigma$ is almost 1.8 times the value of the mean.

*In summary, a small (10%) variation in process and supply parameters can influence $C^t_{eff}$ significantly due to the exponential nature of the dependence.* This influence can be manifested by a metric that is two or more times the mean value. Clearly, this wide distribution must be taken into account in the design and synthesis of next generation ICs.

## V. CONCLUSIONS

We presented a comprehensive analysis of the various gate tunneling current components present during the entire switching cycle of an NMOS for a realistic $45nm$ model. We used this information to identify a new metric for the characterization of the tunneling effect called $C^t_{eff}$. The data obtained from the fit can be further used to analyze the statistical distribution of the metric when the variations of $T_{ox}$ and $V_{DD}$ are known. In an alternative approach, we used directly the variations in $T_{ox}$ and $V_{DD}$ and performed Monte carlo simulations using a baseline BSIM4 model to obtain the statistical distribution of $C^t_{eff}$. This methodology can provide valuable information and estimates for the effect of gate tunneling leakage on power consumption and delay which can then be used to characterize entire cells and libraries leading ultimately to optimized synthesis algorithms for nanoCMOS circuit design.

## REFERENCES


[1] "Semiconductor Industry Association, International Technology Roadmap for Semiconductors," `http://public.itrs.net`.

[2] A. K. Sultania, D. Sylvester, and S. S. Sapatnekar, "Tradeoffs Between Gate Oxide Leakage and Delay for Dual $T_{ox}$ Circuits," in *Proceedings of Design Automation Conference*, 2004, pp. 761–766.

[3] N. S. Kim, T. Austin, D. Blaauw, T. Mudge, K. Flautner, J. S. Hu, M. J. Irwin, M. Kandemir, and N. Vijaykrishnan, "Leakage Current - Moore's Law Meets Static Power," *IEEE Computer*, pp. 68–75, December 2003.

[4] A. Chandrakasan, W. Bowhill, and F. Fox, *Design of High-Performance Microprocessor Circuits*, IEEE Press, 2001.

[5] D. Lee, D. Blaauw, and D. Sylvester, "Gate Oxide Leakage Current Analysis and Reduction for VLSI Circuits," *IEEE Transactions on VLSI Systems*, vol. 12, no. 2, pp. 155–166, February 2004.

[6] S. Mukhopadhyay, C. Neau, R. T. Cakici, A. Agarwala, C. H. Kim, and K. Roy, "Gate Leakage Reduction for Scaled Devices using Transistor Stacking," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, no. 4, pp. 716–730, Apr 2003.

[7] S. Mukhopadhyay, K. Keunwoo, K. J. J. Kim, L. S. Hsien, R. V. Joshi, C. C. Te, and K. Roy, "Modeling and Analysis of Gate Leakage in Ultra-Thin Oxide Sub-50nm Double Gate Devices and Circuits," in *International Symposium on Quality Electronic Design*, 2005, pp. 410–415.

[8] S. Mukhopadhyay and K. Roy, "Modeling and Estimation of Total Leakage Current in Nano-scaled-CMOS Devices Considering the Effect of Parameter Variation," in *International Symposium on Low Power Electronics and Design*, 2003, pp. 172–175.

[9] R. S. Guindi, "Gate-Leakage Estimation and Minimization in CMOS Combinatorial Circuits," in *Proceedings of the 15th International Conference on Microelectronics*, 2003, pp. 85–88.

[10] Y. Cao, T. Sato, D. Sylvester, M. Orshansky, and C. Hu, "New Paradigm of Predictive MOSFET and Interconnect Modeling for Early Circuit Design," in *Proceedings of the IEEE Custom Integrated Circuits Conference*, 2000, pp. 201–204.

[11] Cadence Design Systems Inc., *Spectre User's Guide*.