Peak Power Minimization Through Datapath Scheduling

Saraju P. Mohanty, N. Ranganathan and Sunil K. Chappidi
Department of Computer Science and Engineering
Nanomaterial and Nanomanufacturing Research Center
University of South Florida, Tampa, FL 33620
{smohanty,ranganat,chappidi}@csee.usf.edu

Abstract

In this paper, we describe new integer linear programming models and algorithms for datapath scheduling that aim at minimizing peak power while maintaining performance. The first algorithm, MVDFC combines both multiple supply voltages and dynamic frequency clocking for peak power reduction, while the second algorithm, MVMC explores multiple supply voltages and multicycling. The algorithms use the number and type of different functional units at different operating voltages as the resource constraints. The effectiveness of the proposed scheduling algorithms is studied by estimating the peak power consumption and the power delay product (PDP) of the datapath circuit being synthesised. The algorithms have been applied to various high level synthesis benchmark circuits under different resource constraints. Experimental results show that for the MVDFC, under various resource constraints using two supply voltage levels $(5.0V, 3.3V)$*, average peak power reduction around* 75% *and average PDP reduction of* 60% *can be obtained. For the MVMC scheme, average peak power reduction is around* 36% *and average PDP reduction is* 20%*, for similar resource constraints.*

1 Introduction

With the increase in chip densities and clock frequencies, the demand for the design of low power integrated circuits has increased. The literature is rich on methods to reduce total energy consumption and average power consumption of the CMOS circuits. However, the reduction of peak power consumption is essential to maintain supply voltage levels, to increase reliability, to reduce size of heat sinks and to minimize packaging cost [14] . The peak power is the maximum power consumption of the integrated circuit at any instance during its execution. High peak power can affect the supply voltage levels. The large current flow (large peak power) causes high IR drop in the power line, which leads to reduction of the supply voltage levels at different part of the circuit. High current flow can reduce reliability because of hot electron effects and high current density. The hot electrons may lead to runaway current failures and electrostatic discharge failures. High current density can cause electromigration failure. If the current (power) dissipation is large, then the heat generated out of the system is large. This in turn, results in the need for bigger sinks and costlier heat dissipation mechanisms in order to maintain the operating temperature of the ICs in its tolerance limit.

The use of multiple supply voltages for energy reduction is well researched and several works have appeared in the literature [4, 3, 5, 7]. In multiple supply voltage scheme the functional units can be operated at different supply voltages. The energy savings in this scheme is often accompanied by degradation of performance because of increase in critical path delay. The degradation in performance can be compensated using dynamic frequency clocking [7, 8], multicycling and chaining [9], and variable latency components [1]. In case of multicycling an operation is scheduled in more than one consecutive control step and the control steps are of equal length. On the other hand, in dynamic frequency clocking, an operation is scheduled in one unique control step, but all the control steps of a schedule may not be of equal length. The clock frequency may be changed on the fly. The variable latency components can change the number of cycles required for completion of computation based on the input data.

In [6], peak power reduction is achieved through simultaneous assignment and scheduling. The authors demonstrate the use of power minimization at one level to achieve optimization at another level. Specifically, the simultaneous use of SPICE and behavioral synthesis tools is demonstrated. The authors use genetic algorithms for optimization of average and peak power. In [12], ILP based scheduling and modified force directed scheduling have been proposed to minimize peak power under latency constaints. ILP based

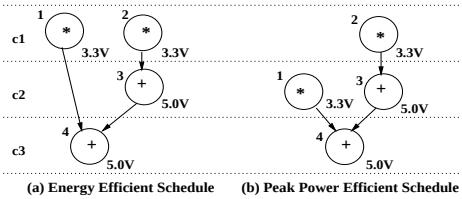

Figure 1: Energy Vs peak power efficient schedule

models to minimize peak power and peak area have been proposed in [13] for latency constraint scheduling. In [10], the authors propose the use of data monitor operations for simultaneous peak power reduction and peak power differential.

In this work, we propose two scheduling schemes to reduce peak power at behavioral level using ILP models. One scheme uses multiple supply voltages and dynamic frequency clocking (MVDFC) and the other scheme uses multiple supply voltages and multicycling (MVMC). To have a clear understanding of the scheduling for energy minimization and peak power minimization, let us refer to data flow graph (DFG) in Fig. 1. The figure shows two different possible schedules of the same DFG using multiple supply voltage scheme. Since, in both cases there are two multiplers operating at $3.3V$ and two adders operating at $5.0V$, the energy and average power consumption of both scheduled DFGs is the same. But, the peak power consumption of the schedule in Fig. 1(b) is less than that of Fig. 1(a). Our approach is to generate peak power efficient schedules similar to the one in Fig. 1(b).

2 ILP Formulations

In this section, we formulate the ILP models for peak power minimization for both MVDFC and MVMC scenario. The ILP models ensure that the dependency constraints and resource constraints are satisfied. The level converters are considered as resources operating in the control step in which it needs to step up signal. The dynamic clocking unit (DCU) that generates dynamic frequency is considered as a resource operating in all the control steps. The power dissipation of the level converters and DCU are included. To measure the performance of the scheduled DFG, we estimate the power delay product (PDP). The PDP for both cases, MVDFC and MVMC is estimated as the product of average power consumption and critical path delay.

For a DFG, let us assume : (i) c = any control step or clock cycle in DFG, (ii) N = total number of control steps in the DFG, (iii) R_c = number of resources active in step c, (iv) f_c = cycle frequency for control step c, (v) $\alpha_{i,c}$ = switching at resource i operating in step c, (vi) $C_{i,c}$ = load capacitance of resource i operating in control step c and (vii) $V_{i,c}$ = operating voltage of resource i operating in control step c. The power consumption for any control step c is given by,

$$P_c = \sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c \quad (1)$$

The peak power consumption of the DFG is the maximum power consumption over all the control steps which can be expressed as below.

$$P_{peak} = Max\big(P_c\big)_{\forall c=1,2,....N} \quad (2)$$

Using Eqn. 1 we rewrite Eqn. 2 as follows.

$$P_{peak} = Max\Big(\sum_{i=1}^{R_c} \alpha_{i,c} C_{i,c} V_{i,c}^2 f_c\Big)_{\forall c=1,2,....N} \quad (3)$$

This would serve as an objective function for the scheduling algorithm. It may be noted that for single frequency and single frequency mode of operation, $V_{i,c}$ and f_c are the same for any clock cycle (c) and resource (i).

In order to formulate an ILP based model for Eqn. 3 and hence a scheduling scheme for the DFG, we use the following notations :
O : total number of operations in the DFG excluding the source and sink nodes (NO-OPs),
o_i : any operation i, $1 \leq i \leq O$,
$F_{k,v}$: functional unit of type k operating at voltage level v,
$M_{k,v}$: maximum number of functional units of type k operating at voltage level v,
S_i : as soon as possible time stamp for the operation o_i,
E_i : as late as possible time stamp for the operation o_i,
$P(i,v,f)$: power consumption of operation o_i at voltage level v and operating frequency f,
$x_{i,c,v,f}$: decision variable which takes the value of 1 if operation o_i is scheduled in control step c using the functional unit $F_{k,v}$ and c has frequency f_c,
$y_{i,v,l,m}$: decision variable which takes the value of 1 if operation o_i is using the functional unit $F_{k,v}$ and scheduled in control steps $l \rightarrow m$ and
$L_{i,v}$: latency for operation o_i using resource operating at voltage v (in terms of number of clock cycles).

2.1 Multiple Supply Voltages and Dynamic Frequency Clocking (MVDFC)

In this subsection, we describe the ILP formulation for peak power minimization using multiple supply voltages and dynamic frequency clocking. In dynamic frequency

clocking [2, 11], the clock frequency is varied on-the-fly based on the functional units active in that cycle. The frequency reduction creates an opportunity to operate the different functional units at different voltages, which in turn, helps in further reduction of power.

(a) *Objective Function* : The objective is to minimize the peak power consumption of the whole DFG over all control steps. This is already described above in Eqn. 3.

$$Minimize : P_{peak} \tag{4}$$

(b) *Uniqueness Constraints* : These constraints ensure that every operation o_i is scheduled to one unique control step within the mobility range (S_i, E_i) with a particular supply voltage and operating frequency. We represent them as, $\forall i$, $1 \leq i \leq O$,

$$\sum_{c} \sum_{v} \sum_{f} x_{i,c,v,f} = 1 \tag{5}$$

(c) *Precedence Constraints* : These constraints guarantee that for an operation o_i, all its predecessors are scheduled in an earlier control step and its successors are scheduled in an later control step. These are modelled as, $\forall i, j, o_i \in Pred_{o_j}$,

$$\sum_{v} \sum_{f} \sum_{d=S_i}^{E_i} d\, x_{i,d,v,f} - \sum_{v} \sum_{f} \sum_{e=S_j}^{E_j} e\, x_{j,e,v,f} \leq -1 \tag{6}$$

(d) *Resource Constraints* : These constraints make sure that no control step contains more than $F_{k,v}$ operations of type k operating at voltage v. These can be enforced as, $\forall c$, $1 \leq c \leq N$ and $\forall v$,

$$\sum_{i \in F_{k,v}} \sum_{f} x_{i,c,v,f} \leq M_{k,v} \tag{7}$$

(e) *Frequency Constraints* : This set ensures that if a functional unit is operating at higher voltage level then it can be scheduled in a lower frequency control step, whereas, a functional unit is operating at lower voltage level then it can't be scheduled in a higher frequency control step. We write these constraints as, $\forall i$, $1 \leq i \leq O$, $\forall c$, $1 \leq c \leq N$, if $f < v$, then $x_{i,c,v,f} = 0$.

(f) *Peak Power Constraints* : These constraints ensure that the maximum power consumption of the DFG does not exceed P_{peak} for any control step. We enforce these constraints as follows, $\forall c$, $1 \leq c \leq N$ and $\forall v$,

$$\sum_{i \in F_{k,v}} \sum_{f} x_{i,c,v,f}\ P(i,v,f) \leq P_{peak} \tag{8}$$

2.2 Multiple Supply Voltages and Multicycling (MVMC)

In this subsection, we describe the ILP formulation for peak power minimization using multiple supply voltages and multicycling. In this scheme, the functional units are operated at multiple supply voltages and the lower operating voltage functional units are scheduled in consecutive control steps.

(a) *Objective Function* : The objective is to minimize the peak power consumption of the whole DFG over all control steps. This is already described above in Eqn. 3.

$$Minimize : P_{peak} \tag{9}$$

(b) *Uniqueness Constraints* : These constraints ensure that every operation o_i is scheduled in appropriate control steps within the mobility range (S_i, E_i) with a particular supply voltage. Depending on the supply voltage it may be operated at more than one clock cycle. We represent them as, $\forall i, 1 \leq i \leq O$,

$$\sum_{v} \sum_{l=S_i}^{S_i+E_i+1-L_{i,v}} y_{i,v,l,(l+L_{i,v}-1)} = 1 \tag{10}$$

When the operators are operating at highest voltage, they are scheduled in one unique control step, whereas, when they are to be operated at lower voltages they need more than one clock cycle for completion. Thus, for lower voltage the mobility is restricted.

(c) *Precedence Constraints* : These constraints guarantee that for an operation o_i, all its predecessors are scheduled in an earlier control step and its successors are scheduled in an later control step. These constraints should also take care of the multicycling operations. These are modelled as, $\forall i, j, o_i \in Pred_{o_j}$,

$$\sum_{v} \sum_{l=S_i}^{E_i} (l + L_{i,v} - 1)\, y_{i,v,l,(l+L_{i,v}-1)} - \sum_{v} \sum_{l=S_j}^{E_j} l\, y_{j,v,l,(l+L_{j,v}-1)} \leq -1 \tag{11}$$

(d) *Resource Constraints* : These constraints make sure that no control step contains more than $F_{k,v}$ operations of type k operating at voltage v. These can be enforced as, $\forall v$ and $\forall l$, $1 \leq l \leq N$,

$$\sum_{i \in F_{k,v}} \sum_{l} y_{i,v,l,(l+L_{i,v}-1)} \leq M_{k,v} \tag{12}$$

(e) *Peak Power Constraints* : These constraints ensure that the maximum power consumption of the DFG does not exceed P_{peak} for any control step. We enforce these constraints as follows, $\forall l$, $1 \leq l \leq N$,

$$\sum_{i \in F_{k,v}} \sum_{v} y_{i,v,l,(l+L_{i,v}-1)}\ P(i,v,f_{clk}) \leq P_{peak} \tag{13}$$

Step 1: Find ASAP schedule of the UDFG.
Step 2: Find ALAP schedule of the UDFG.
Step 3: Determine the mobility graph of each node.
Step 4: Modify the mobility graph for MVMC.
Step 5: Construct the ILP formulations.
Step 6: Solve the ILP formulations using LP-Solve.
Step 7: Find the scheduled DFG.
Step 8: Determine the cycle frequencies for MVDFC.

Figure 2: Scheduling for peak power minimization

3 ILP-Based Scheduler

In this section, we will discuss the solutions for the ILP formulations obtained in the previous section. The target architecture and characterised datapath components are from [7]. The ILP based scheduler which minimizes peak power consumption of the DFG is outlined in Fig. 2. The first step is to determine the as soon as possible (ASAP) time stamp of each operation. The second step is the determination of the as late as possible (ALAP) time stamp of each vertex for the DFG. The ASAP time stamp is the start time and the ALAP time stamp is the finish time of each operation. These two times provide the mobility of a operation and the operation must be scheduled in this mobile range. This mobility graph needs to be modified for the MVMC scheme. Then the scheduler determines the ILP formulations based on the models described in section 2. After the ILP formulation is solved (using LP-Solve) the scheduled DFG is obtained. The scheduler determines the cycle frequencies for the scheduled DFG for the MVDFC scheme.

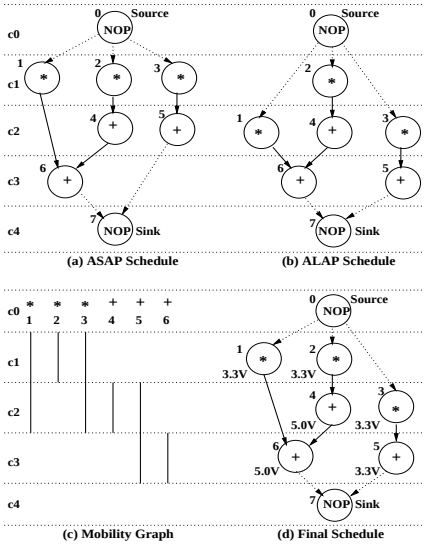

Figure 3: Example DFG (for RC1) (MVDFC)

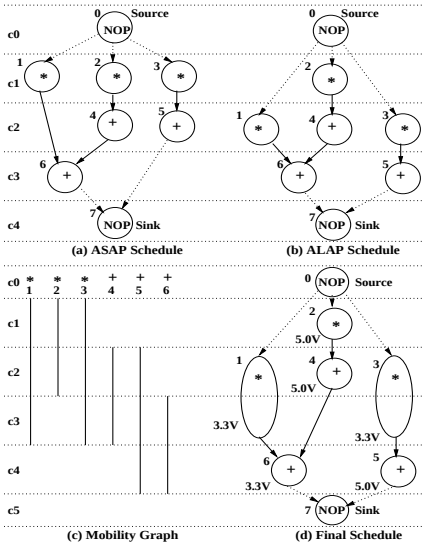

Figure 4: Example DFG (for RC1) (MVMC)

3.1 Scheduling for MVDFC

We illustrate the solution for the ILP formulation in the MVDFC case, using the DFG shown in Fig. 3. The ASAP schedule is shown in Fig. 3(a) and the ALAP schedule is shown in Fig. 3(b). From the ASAP and ALAP schedules we obtain the mobility graph as in Fig. 3(c). Using this mobility graph, we get the ILP formulations. We solved the formulation using LP-solve and based on the results, we obtained the scheduled DFG shown is Fig. 3(d) for the resource constraint (RC1), two multipliers at $3.3V$, one multiplier at $5.0V$, one ALU at $3.3V$ and one ALU operating at $5.0V$.

3.2 Scheduling for MVMC

We illustrate solution for the ILP formulation of the MVMC case, with the help of the DFG shown in Fig. 4. The ASAP schedule is shown in Fig. 4(a) and the ALAP schedule is shown in Fig. 4(b). From the ASAP and ALAP schedules we obtain the mobility graph which is Fig.4(c). This mobility graph is different from that shown in Fig. 3(c). In the MVMC case, the mobility graph considers multicycle operations. We assume that two operating voltage levels, and also that when the multipliers are operated at lower voltage, they take two clock cycles. For the characterised cells used in our experiment [7], the operating clock frequency, f_{clk} is $18MHz$. Using this mobility graph, we get the ILP formulations. We solved the formulation using LP-solve and obtained the scheduled DFG shown is Fig. 4(d) for the resource constraint (RC1).

4 Experimental Results

The ILP based MVDFC and MVMC schedulers were tested with five benchmark circuits : (1) Example circuit (exp), (2) FIR filter, (3) IIR filter, (4) HAL differential equation solver and (5) Auto-Regressive filter (arf). The characterised datapath cells are used from [7]. The following notations are used to express results :
P_S : the peak power consumption (in mW) for single supply voltage and single frequency operation,
P_{DFC} : the peak power consumption (in mW) for multiple supply voltages and dynamic frequency operation,
P_{MC} : the peak power consumption (in mW) for multiple supply voltages and multicycle operation,
PDP_S : the power delay product (in nJ) for single supply voltage and single frequency operation,
PDP_{DFC} : the power delay product (in nJ) for multiple supply voltage and dynamic frequency clocking operation,
PDP_{MC} : the power delay product (in nJ) for multiple supply voltage and multicycle operation,
$\Delta P_{DFC} = \frac{(P_S - P_{DFC})}{P_S} * 100$: the percentage peak power reduction due to MVDFC operation,
$\Delta P_{MC} = \frac{(P_S - P_{MC})}{P_S} * 100$: the percentage peak power reduction due to MVMC operation,
$\Delta PDP_{DFC} = \frac{(PDP_S - PDP_{DFC})}{PDP_S} * 100$: the percentage PDP reduction due to MVDFC operation, and
$\Delta PDP_{MC} = \frac{(PDP_S - PDP_{MC})}{PDP_S} * 100$: the percentage PDP reduction due to MVMC operation.

The ILP-based scheduler was tested using the different sets of resource constraints shown in Table 1. The experimental results for various benchmark circuits are reported in Table 2. The power estimation includes the power consumption of the overheads, such as level converters and dynamic clocking unit. It is assumed that each resource has equal switching activity ($\alpha_{i,c}$). The results are reported for two supply voltages and for switching = 0.5. Table 2 also shows the average reductions for different benchmarks averaged over all resource constraints. It is obvious from the average data that the reductions are appreciable. To get a general idea of relative performance, the peak power reductions for the proposed scheduling schemes are listed alongwith other scheduling algorithms dealing with peak power reduction in Table 3.

Table 1: Resource constraints

Resource Constraints Details				Resource Constraint Labels
Multipliers		ALUs		
3.3 V	5.0 V	3.3 V	5.0 V	
2	1	1	1	RC1
3	0	1	1	RC2
2	0	0	2	RC3
1	1	0	1	RC4
2	0	0	1	RC5

5 Conclusions

This paper addresses the peak power reduction at behavioral level using low power datapath scheduling techniques based on ILP-models. Two datapath scheduling schemes, one using multiple supply voltage and dynamic clocking and another using multiple supply voltage and multicycling have been introduced. In both cases, the proposed scheduling schemes could achieve significant amount of peak power reduction over the single supply voltage and single frequency scenario. It is observed that for MVDFC case, using two supply voltage levels an average peak power reduction is 75% and average PDP reduction is 60%. Similarly, for MVMC case, the average peak power reduction is 36% and average PDP reduction is 20%. *The results clearly indicate that the dynamic frequency clocking is a better scheme than the multicycling approach for peak power minimization.*

References

[1] L. Benini, E. Macii, M. Pnocino, and G. D. Micheli. Telescopic units : A new paradigm for performance optimization of VLSI design. *IEEE Trans. on CAD*, 17(3):220–232, Mar 1998.

[2] I. Brynjolfson and Z. Zilic. Dynamic clock management for low power applications in FPGAs. In *Proc. of IEEE Custom Integrated Circuits Conference*, pages 139–142, 2000.

[3] J. M. Chang and M. Pedram. Energy minimization using multiple supply voltages. *IEEE Trans. on VLSI Systems*, 5(4):436–443, Dec 1997.

[4] M. Johnson and K. Roy. Datapath scheduling with multiple supply voltages and level converters. *ACM Trans. on Design Automation of Electronic Systems*, 2(3):227–248, July 1997.

[5] Y. R. Lin, C. T. Hwang, and A. C. H. Wu. Scheduling techniques for variable voltage low power design. *ACM Trans. on Design Automation of Electronic Systems*, 2(2):81–97, Apr 1997.

[6] R. S. Martin and J. P. Knight. Using spice and behavioral synthesis tools to optimize ASICs' peak power consmpution. In *Proc. of 38th Midwest Symposium on Circuits and Systems*, pages 1209–1212, 1996.

Table 2: Power and PDP estimates for benchmarks using MVDFC and MVMC schemes (α=0.5)

	R	Peak Power (mW)					PDP Estimates (nJ)				
	C	P_S	P_{DFC}	ΔP_{DFC}	P_{MC}	ΔP_{MC}	PDP_S	PDP_{DFC}	ΔPDP_{DFC}	PDP_{MC}	ΔPDP_{MC}
1	2	3	4	5	6	7	8	9	10	11	12
ex(1)	1	79.2	17.3	78.2	35.6	55.1	20.3	7.8	61.9	17.0	16.1
	2	79.2	17.3	78.2	51.8	34.6	20.3	7.8	61.9	12.0	41.1
	3	79.2	17.3	78.2	34.6	56.4	20.3	7.6	62.5	15.3	24.8
	4	40.7	9.2	77.5	40.7	0	27.1	10.5	61.4	27.1	0
	5	40.7	9.2	77.5	34.6	15.1	27.1	10.5	61.4	15.1	44.3
	Average values			**77.9**		**32.2**			**61.8**		**25.3**
fir(2)	1	79.2	17.3	78.2	40.7	48.6	56.2	21.8	61.1	51.8	7.8
	2	79.2	17.3	78.2	51.3	35.2	56.2	21.8	61.1	49.3	12.3
	3	79.2	17.3	78.2	35.6	55.1	56.2	22.0	60.9	34.3	39.0
	4	79.2	40.6	48.7	40.7	48.61	56.2	46.6	17.1	67.5	-20.1
	5	79.2	17.3	78.2	35.6	55.1	56.2	22.1	60.7	35.2	37.4
	Average values			**72.3**		**48.5**			**52.2**		**15.3**
iir(3)	1	118.9	37.1	68.8	74.2	37.6	45.0	17.8	60.5	43.3	3.8
	2	118.9	25.9	78.2	51.9	56.4	45.0	14.4	68.0	29.8	33.8
	3	79.3	17.3	78.2	34.6	56.4	56.2	19.4	65.5	40.2	28.5
	4	80.3	29.0	63.9	56.9	29.1	56.2	34.0	39.4	60.0	6.8
	5	80.3	17.8	77.9	34.6	56.9	56.2	18.8	66.5	40.2	28.5
	Average values			**73.4**		**47.2**			**60.0**		**20.3**
hal(4)	1	80.3	17.5	78.2	56.9	29.1	54.0	21.0	61.1	73.0	-35.2
	2	80.3	17.5	78.2	51.8	35.5	54.0	21.0	61.1	35.9	33.5
	3	80.3	17.8	77.8	35.6	55.7	54.0	20.8	61.5	42.3	21.7
	4	80.3	29.0	63.9	58.0	27.8	67.5	45.7	32.2	73.5	-8.9
	5	80.3	17.8	77.9	35.6	55.7	67.5	26.4	60.9	48.4	28.3
	Average values			**75.2**		**40.8**			**55.4**		**7.9**
arf(5)	1	40.7	8.9	78.2	35.0	14.0	114.7	31.5	72.5	66.2	42.3
	2	40.7	8.9	78.2	35.0	14.0	114.7	31.5	72.5	66.7	41.8
	3	40.7	9.1	77.5	35.6	12.5	114.7	38.2	66.7	68.3	40.5
	4	40.7	9.1	77.5	39.6	2.7	114.7	39.0	66.0	132.9	-15.9
	5	40.7	9.1	77.5	35.6	12.5	114.7	38.2	66.7	68.3	40.5
	Average values			**77.8**		**11.1**			**68.9**		**29.8**
Average over all benchmarks				**75.3**		**36.0**			**59.7**		**19.7**

Table 3: Peak power reduction for various scheduling schemes

Benchmark Circuits	MVDFC (This Work)		MVMC (This Work)		Shiue [12]	Martin [6]	Raghunathan [10]
	ΔP_{DFC}	ΔPDP_{DFC}	ΔP_{MC}	ΔPDP_{MC}	ΔP	ΔP	ΔP
(2)fir	72.3	52.2	48.5	15.3	63.0	40.3	23.1
(4)hal	75.2	55.4	40.8	7.9	28.0	-	-
(5)arf	77.8	68.9	11.1	29.8	50.0	-	-

[7] S. P. Mohanty and N. Ranganathan. Energy efficient scheduling for datapath synthesis. In *Proc. of Intl. Conf. on VLSI Design (to appear)*, Jan 2003.

[8] S. P. Mohanty, N. Ranganathan, and V. Krishna. Datapath scheduling using dynamic frequency clocking. In *Proc. of ISVLSI'2002*, pages 65–70, Apr 2002.

[9] S. Park and K. Choi. Performance-driven high-level synthesis with bit-level chaining and clock selection. *IEEE Trans. on CAD*, 20(2):199–212, Feb 2001.

[10] V. Raghunathan, S. Ravi, A. Raghunathan, and G. Lakshminarayana. Transient power management through high level synthesis. In *Proc. of ICCAD*, pages 545–552, 2001.

[11] N. Ranganathan, N. Vijaykrishnan, and N. Bhavanishankar. A linear array processor with dynamic frequency clocking for image processing applications. *IEEE Trans. on CSVT*, 8(4):435–445, August 1998.

[12] W. T. Shiue. High level synthesis for peak power minimization using ILP. In *Proc. of IEEE International Conference on Application Specific Systems, Architectures and Processors*, pages 103–112, 2000.

[13] W. T. Shiue and C. Chakrabarti. ILP based scheme for low power scheduling and resource binding. In *Proc. of ISCAS*, pages III.279–III.282, 2000.

[14] D. Singh, J. M. Rabaey, M. Pedram, F. Catthoor, S. Rajgopal, N. Sehgal, and T. J. Mozdzen. Power conscious cad tools and methodologies : A perspective. *Proceedings of the IEEE*, 83(4):570–594, Apr 1995.