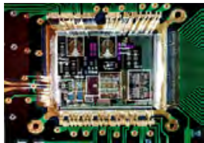
Lecture 10: Efficient Design of Current-Starved VCO

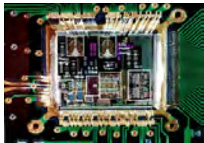
CSCE 6933/5933
Advanced Topics in VLSI Systems

Instructor: Saraju P. Mohanty, Ph. D.

NOTE: The figures, text etc included in slides are borrowed from various books, websites, authors pages, and other sources for academic purpose only. The instructor does not claim any originality.

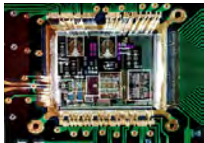


Unified P4 (Power-Performance-Process-Parasitic) Fast Optimization of a Nano-CMOS VCO



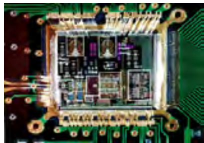
Outline of the Talk

- Introduction
- Novel Contributions
- Related Prior Research
- Proposed Novel RFIC P4 Optimal Design Flow
- Design of 90nm CMOS VCO
- Process Variation Analysis of VCO
- P4 Optimization of VCO
- Conclusions and Future Research



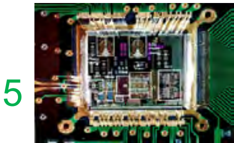
Introduction

- Radio Frequency Integrated Circuits (RFICs) are becoming performance-oriented. The battle to deliver maximum performance has taken center stage. (Performance)
- Power-aware design is required to maximize some performance metric, subject to a power budget. (Power)
- Also, potential yield loss is caused by increasing process variations. Impact of process variations on the performance factors of a design is much higher for today's nanometer. (Process)
- In high frequency application circuits, the exact performance prediction is challenging due to many parasitic effects. It is crucial to be able to predict parasitic effects for accurate performance. (Parasitic)



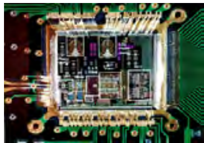
Novel Contributions

- A P4 (Power-Performance-Parasitic-Process) optimal design flow for RF circuits is proposed.
- Nano-CMOS current starved VCO subjected to design flow.
- P4 optimization of the VCO is carried out using a dual-oxide process technique.
- A dual-oxide physical design of the VCO is presented for 90nm CMOS technology.
- A novel *process variation analysis* technique called Design of Experiments-Monte Carlo (DOE-MC) approach is proposed, offering up to 6.25X computational time savings over traditional Monte-Carlo (TMC).



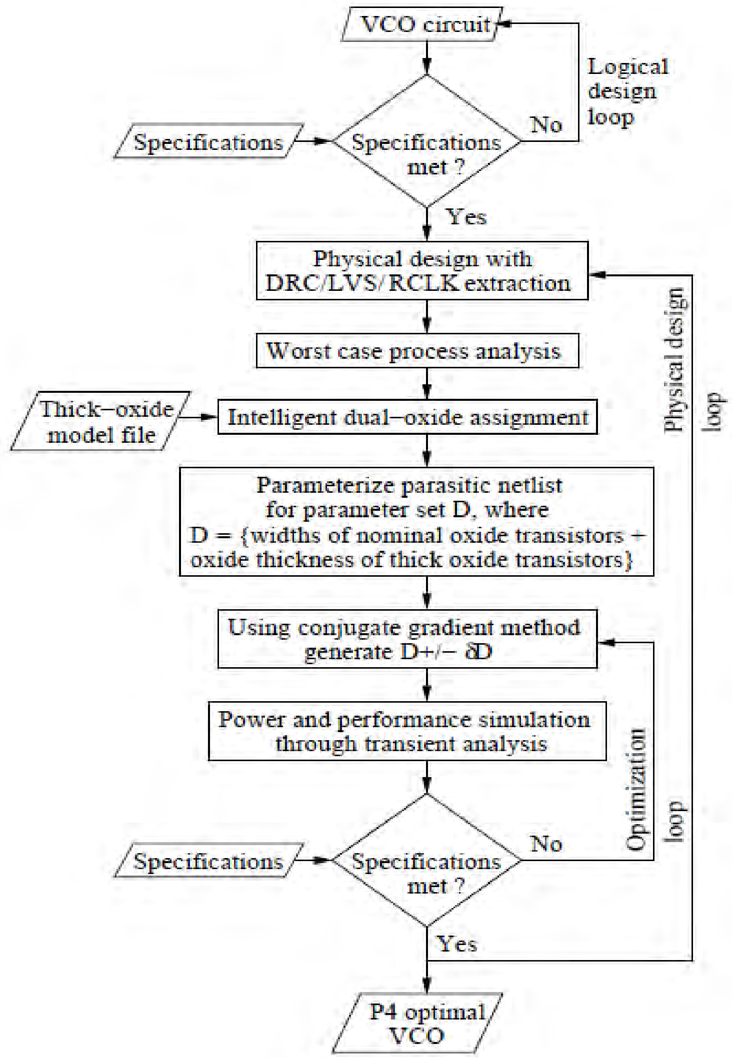
Related Prior Research

Reference	Technology	Performance	Power
Tiebout et. al.	250nm	1.8GHz	20mW
Dehghani et.al.	250nm	2.5GHz	2.6mW
Long et. al.	180nm	2.4GHz	1.8mW
Kwok et. al.	180nm	1.4GHz	1.46mW
This Design	**90nm dual-oxide**	**2.3GHz**	**158μW**



Proposed Novel RFIC P4 Optimal Design Flow

- The logical design is done to meet the required specifications.
- Initial physical design is subjected to DRC/LVS/RCLK extraction.
- Worst case process variation analysis of the physical design is done with respect to performance (center frequency).
- Intelligent dual-oxide assignment (*Toxpth, Toxnth*) to the power-hungry transistors of the VCO using a *thick oxide model file.*
- Parasitic netlist is parameterized for parameter set D (widths of transistors and *Toxpth, Toxnth*). The parameterized parasitic netlist is subjected to a optimization loop to meet the specifications (performance, power) in a *worst case process* environment.
- Parameter values for which the specifications are met are obtained, and a final physical design of the VCO is created using these parameter values.

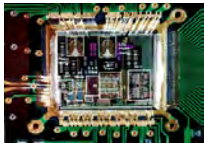


Design of 90nm CMOS VCO

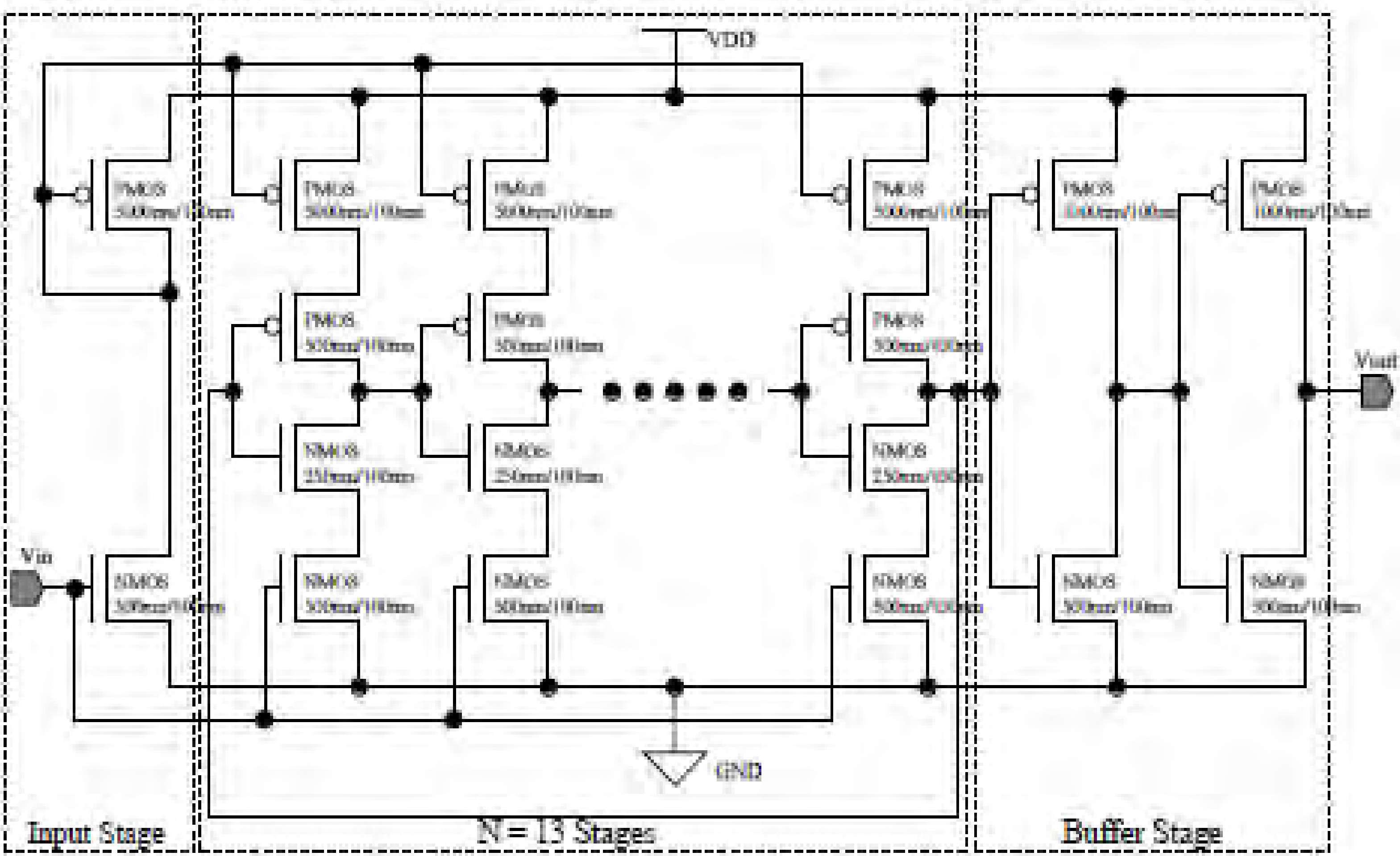
- Current starved VCO design performed using 90nm generic process. Target oscillation frequency $(f_0) \geq 2\text{GHz}$.

$$f_0 = \frac{I_D}{N * C_{tot} * V_{DD}}, \quad C_{tot} = \frac{5}{2} C_{ox}(W_p L_p + W_n L_n), \quad C_{ox} = \frac{\varepsilon_{r_{ox}} \varepsilon_0}{T_{ox}},$$

- V_{DD} : supply voltage, I_D: current flowing through inverter, N: odd number of inverters, C_{tot}: total capacitance of each inverter stage, C_{ox}: gate oxide capacitance per unit area, {Wp, Lp}: inverter PMOS width (500nm) and length (100nm), {Wn, Ln}: inverter NMOS width (250nm) and length (100nm), {Wpcs, Lpcs}: current starved PMOS width (5um) and length (100nm), {Wncs, Lncs}: current starved NMOS width (500nm) and length (100nm).

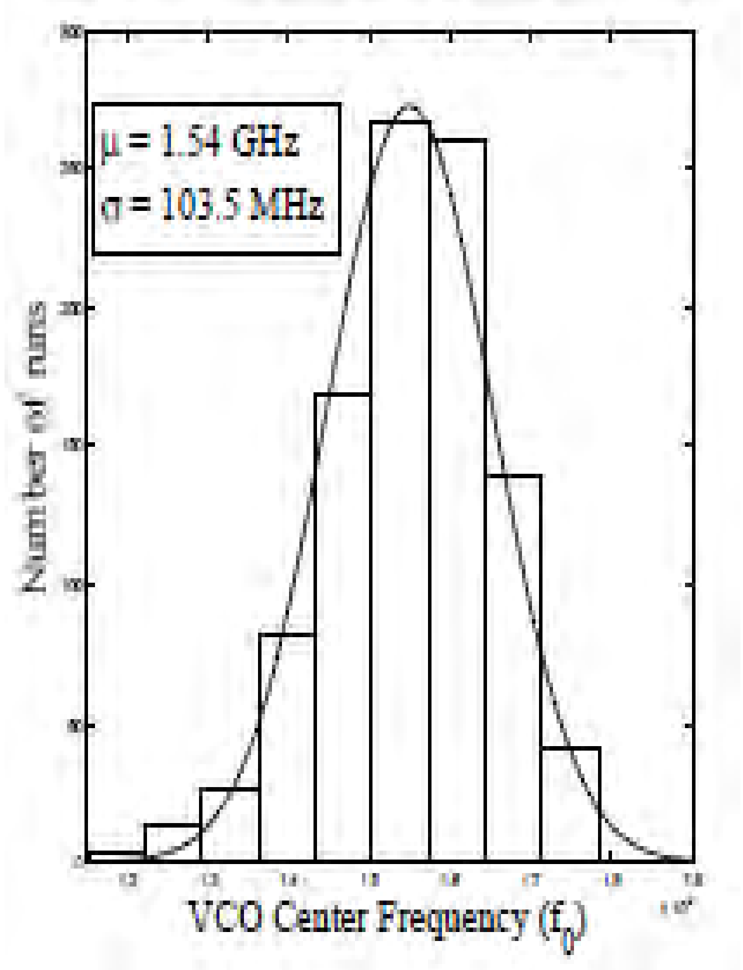


Design of 90nm CMOS VCO



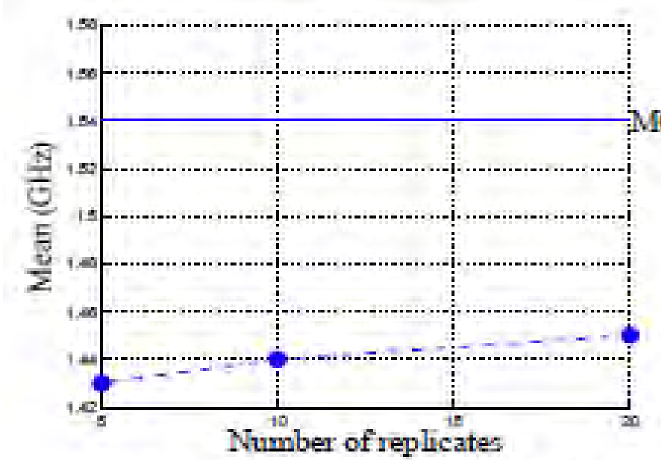
Process Variation Analysis of VCO: TMC

- Process variation analysis has been carried out on the initial physical design with parasitics extracted (RLCK).
- Variation in 5 parameters:
  - VDD: Supply voltage,
  - Vtn: NMOS threshold voltage,
  - Vtp: PMOS threshold voltage,
  - Toxn: NMOS gate oxide thickness,
  - Toxp: PMOS gate oxide thickness.
- Process parameters assumed to have a Gaussian distribution with mean (μ) as the nominal value in the process design kit, and a standard deviation (σ) as 10% of the mean. TMC with 1000 runs gives the oscillation frequency (f_0) having a Gaussian distribution with μ = 1.54 GHz, σ = 103.5 MHz.

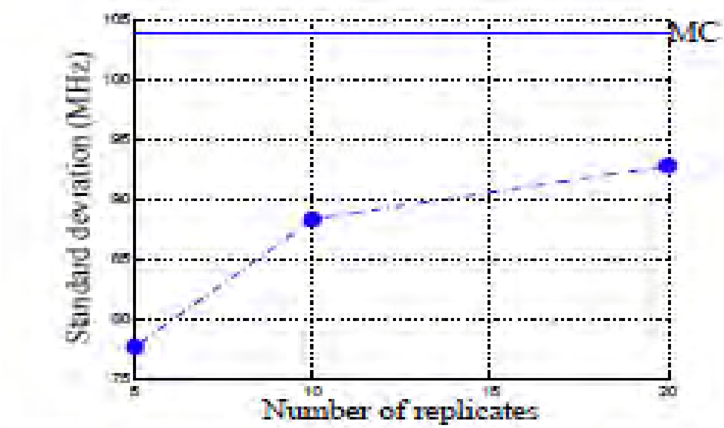


Process Variation Analysis of VCO: DOE-MC

- The DOE-MC methodology offers the advantage of faster computation over TMC.
- A ***two level full factorial design*** is run for the 5 process parameters, where:
  - **Level 1:** $\mu - 2 \times \sigma$,
  - **Level 2:** $\mu + 2 \times \sigma$.
- A full factorial run requires $2^5 = 32$ trials. 5 MC replicate runs are run for every trial. $\mu(f_0)$ and $\sigma(f_0)$ are recorded. We obtain 32 values of $\mu(f_0)$ and $\sigma(f_0)$.
- The final $\mu(f_0)$ and $\sigma(f_0)$ are recorded as the average of the 32 trials. Considering 5 replicates per trial, we get a total of $32 \times 5 = 160$ runs (compared to 1000 TMC runs).



(a) Mean of f_0 distribution



(b) Standard deviation of f_0 distribution

Process Variation Analysis of VCO: DOE-MC

- The DOE-MC technique is less accurate than traditional MC, but saves on computing time.
- The results for MC replicates per trial = 10 and 20 and the percentage error in μ and σ is also presented.
- Worst case process for f_0 identified where VDD reduced by 10%, and all the other process parameters (Vtn, Vtp, Toxn, Toxp) are increased by 10%.

MC runs per trial	Total runs	% error (μ)	% error (σ)	Time saving over TMC
5	160	7.47	25.1	6.25X
10	320	6.78	14.7	2X
20	640	5.78	10.3	1.5625X

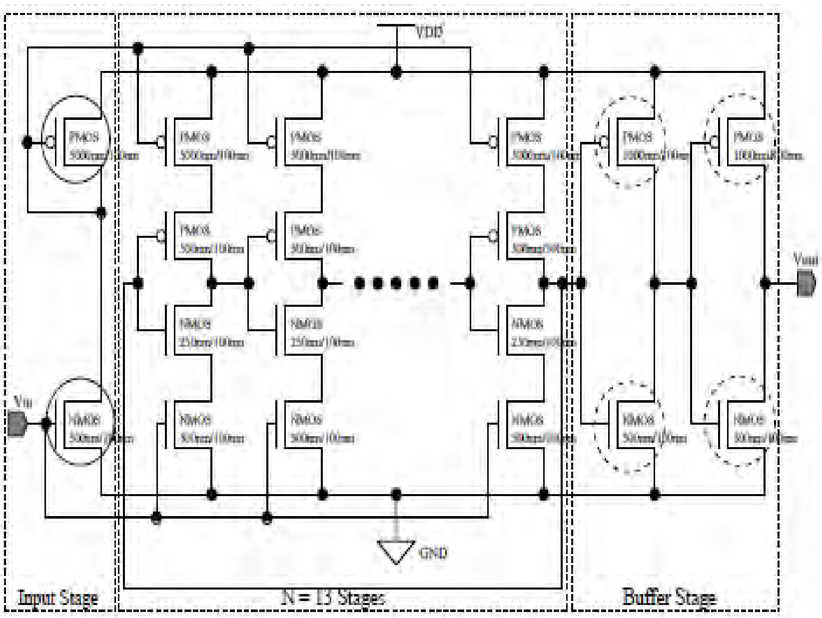
P4 Optimization of VCO

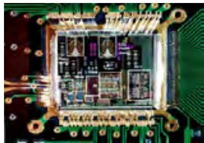
- Logical design center frequency f_0 = 2 GHz.
- Initial physical design center frequency f_{0p} = 1.56 GHz (25% degradation).
- Initial physical design center frequency in a *worst case process* variation environment f_{0p-p} = 1.13 GHz (43.5% degradation).
- Initial average power consumption (including leakage) (P_{VCO}) = 212μW.

Parameter	Initial Physical Design	Initial Physical Design + Process Variation	Final Physical Design + Process Variation
f_0	$1.56GHz$	$1.13GHz$	$1.98GHz$
discrepancy	25%	43.5%	1%
V_{DD}	$1.2V$ (nominal)	$1.08V$ (-10%)	$1.08V$
V_{tn}	$0.1692662V$ (nominal)	$0.186193V$ ($+10\%$)	$0.186193V$
V_{tp}	$-0.1359511V$ (nominal)	$-0.149546V$ ($+10\%$)	$-0.149546V$
T_{oxn}	$2.33nm$ (nominal)	$2.563nm$ ($+10\%$)	$2.563nm$
T_{oxp}	$2.48nm$ (nominal)	$2.728nm$ ($+10\%$)	$2.728nm$

Intelligent Dual-Oxide Assignment

- Average power consumed by all the transistors is measured.
- Input stage transistors (shown by solid circles) consume 48% of total average power of the VCO circuit. Most suitable candidates for higher thickness oxide assignment (*Toxpth, Toxnth*).
- The buffer stage transistors (shown by dashed circles) consume 11.5% of the total average power. May be treated to higher thickness oxide, for further power minimization.
- Input stage transistors follow *thick-oxide model file,* other transistors follow *baseline model file.*





Conjugate Gradient Optimization

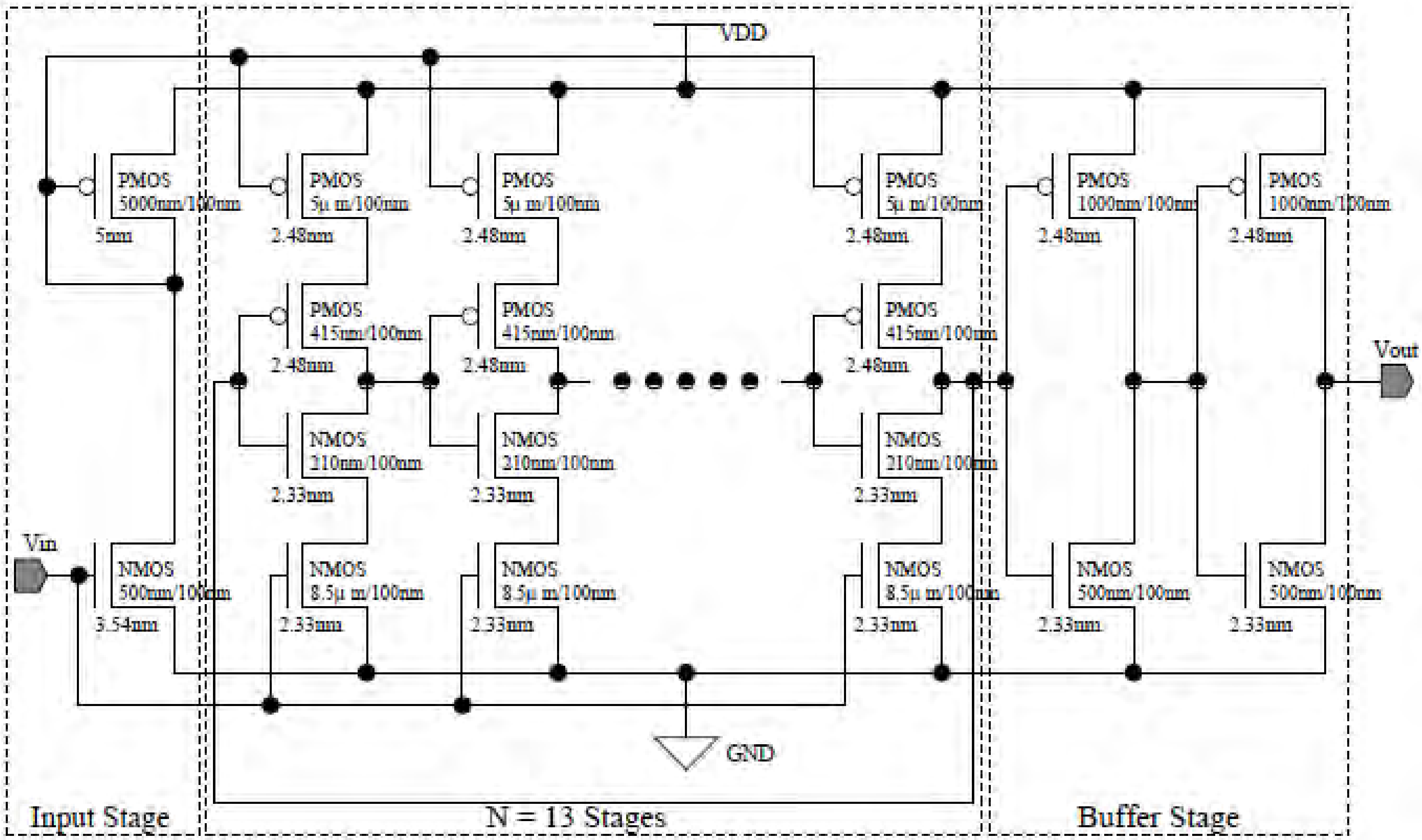
- **Input:** Parasitic parameterized netlist, Baseline model file, Thick oxide model file, Objective set $F = [\, f_0, P_{VCO}]$, Stopping criteria S, design variable set $D = [\, Wn, Wp, Wncs, Wpcs, Toxpth, Toxnth \,]$, Lower design constraint C_{low}, Upper design constraint C_{up}.
- **Output:** Optimized objective set F_{opt}, Optimal design variable set D_{opt} for $S = \pm \beta$, {where $1\% \leq \beta \leq 5\%$}.
- Run initial simulation in order to obtain feasible values of design variables for the given specifications.
- **while** ($C_{low} < D < C_{up}$) **do**
- Using conjugate gradient, generate new set of design variables $D' = D \pm \delta D$.
- Compute objective set $F = [\, f_0, P_{VCO}]$.
- **if** ($S == \pm \beta$) **then**
- **return** $D_{opt} = D'$.
- **end if**
- **end while**
- Using D_{opt}, construct final physical design and simulate.
- Record F_{opt}.

Conjugate Gradient Optimization

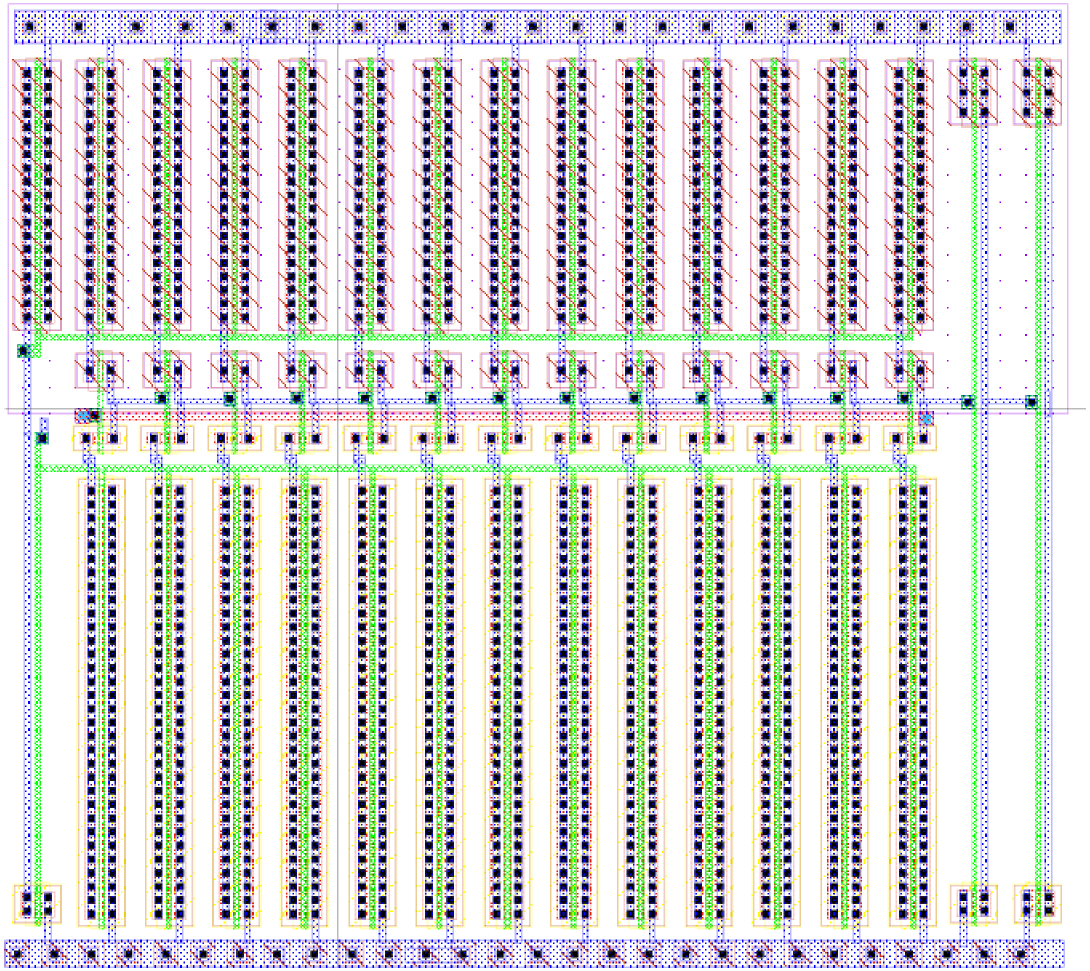
- Target center frequency f_0 = 2GHz.
- Final Physical design center frequency f_{0p} = 2.3GHz.
- Final Physical design center frequency in a worst case process variation environment f_{0p-p} = 1.98GHz (1% discrepancy).
- Final average power consumption (including leakage) (P_{VCO}) = 158µW (25% reduction).

D	C_{low}	C_{up}	D_{opt}
Wn	200nm	500nm	210nm
Wp	400nm	1µm	415nm
Wncs	1µm	10µm	8.5µm
Wpcs	5µm	10µm	5µm
Toxpth	2.48nm	5nm	5nm
Toxnth	2.33nm	5nm	3.54nm

P4 Optimal Dual-Oxide Logical Design

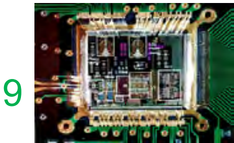


P4 Optimal Dual-Oxide Physical Design

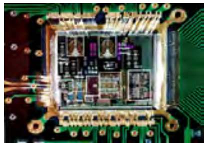


Conclusions and Future Research

- Design of a P4 (Power-Performance-Parasitic-Process) optimal nano-CMOS VCO is proposed. The presented design flow may be used for optimization of nanoscale circuits in general.
- The center frequency treated as the target specification. The degradation of the center frequency due to parasitic and process variation effects narrowed down from 43.5% to 1%, along with 25% power minimization using dual-oxide technique.
- The end product of the proposed design flow is a P4 optimal dual-oxide VCO physical design.
- For future research, we plan to consider thermal effects in the VCO design as well.
- Alternative optimization techniques such as simulated annealing and genetic algorithms are also being explored for a fair comparison of the P4 design flow with other approaches.

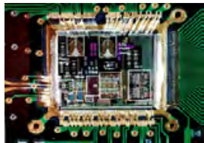


A P4VT (Power-Performance-Process-Parasitic-Voltage-Temperature) Aware Dual-V_{Th} Nano-CMOS VCO



Outline of the Talk

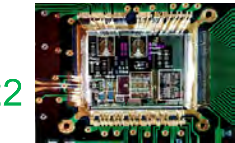
- Introduction
- Novel Contributions of this paper
- Related Prior Research
- Proposed Novel P4VT Aware Design Flow
- Logical Design of VCO
- PVT Variation Analysis of VCO
- P4VT Optimization of VCO
- Conclusions and Future Research



Introduction …

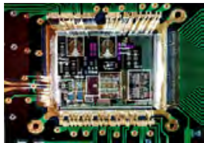
- **Power-Performance:** Radio Frequency Integrated Circuits (RFICs) must be simultaneously:
  - Low power consuming
  - High performance
- **Process-Voltage:** Impact of process and supply voltage variations on the performance factors of a design is much higher for nanometer technologies.

UNIVERSITY OF NORTH TEXAS
Discover the power of ideas



Introduction

- **Parasitics:** In high frequency application circuits, the exact performance prediction is challenging due to many parasitic effects. It is crucial to be able to account parasitic effects for accurate performance.
- **Temperature:** There is a need for temperature-aware design methodologies in order to produce properly functioning and reliable silicon.

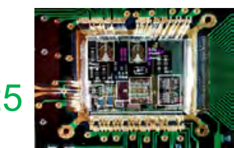


Novel Contributions of This Paper

- A Power-Performance-Parasitic-Process-Voltage-Temperature (called P4VT) aware optimization flow for nanoscale CMOS analog circuits is introduced.
- The design of a P4VT-aware RF nano-CMOS circuit, VCO is discussed.
- For power optimization of the VCO, a dual-threshold process level technique is discussed.
- A dual-threshold physical design of the optimized VCO is presented.

Prior Research: VCO Design

Research	Tech. Node	Performance	Power	Area
Tiebout et al.	250nm	1.8GHz	20mW	1.1mm^2
Troedsson et al.	250nm	2.4GHz	5.5mW	0.874µm^2
Long et al.	180nm	2.4GHz	1.8mW	--
Kwok et al.	180nm	1.4GHz	1.46mW	0.76mm^2
This Paper	90nm Dual-V_{Th}	2.4GHz	137.5µW	547.7µm^2



Prior Research: PVT Tolerance

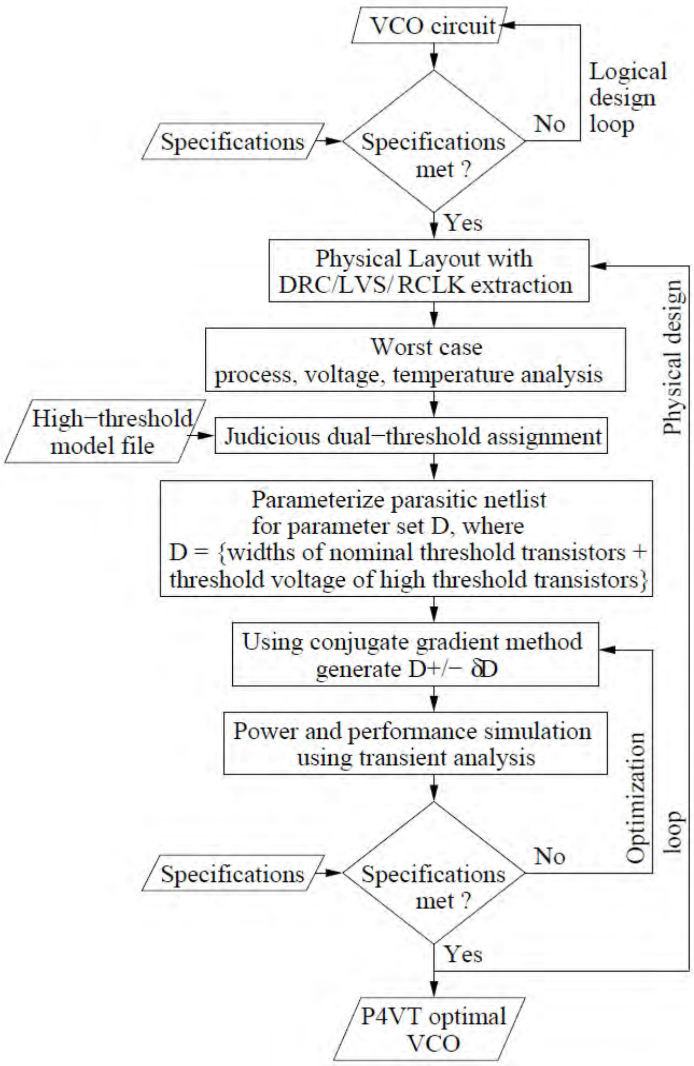
- **Kim 2009**: PVT-tolerance using supply/body-bias voltage generation.
- **Charan 2008**: Corner analysis used for PVT-tolerant humidity sensor.
- **Miyashita 2005**: Automatic amplitude control is used to reduce PVT variation in LC-VCO.
- **Kondou 2007**: Two on-chip digital calibration circuits are used for PVT-tolerant PLL.

Prior Research: Parasitic Tolerance

- **Park 2003**: Parasitic-Aware optimization of CMOS wideband amplifier.
- **Choi 2006**: Simulated annealing optimization for parasitic-aware RF power amplifier.
- **Choi 2003**: Particle swarm optimization techniques for parasitic-aware CMOS RF circuits.

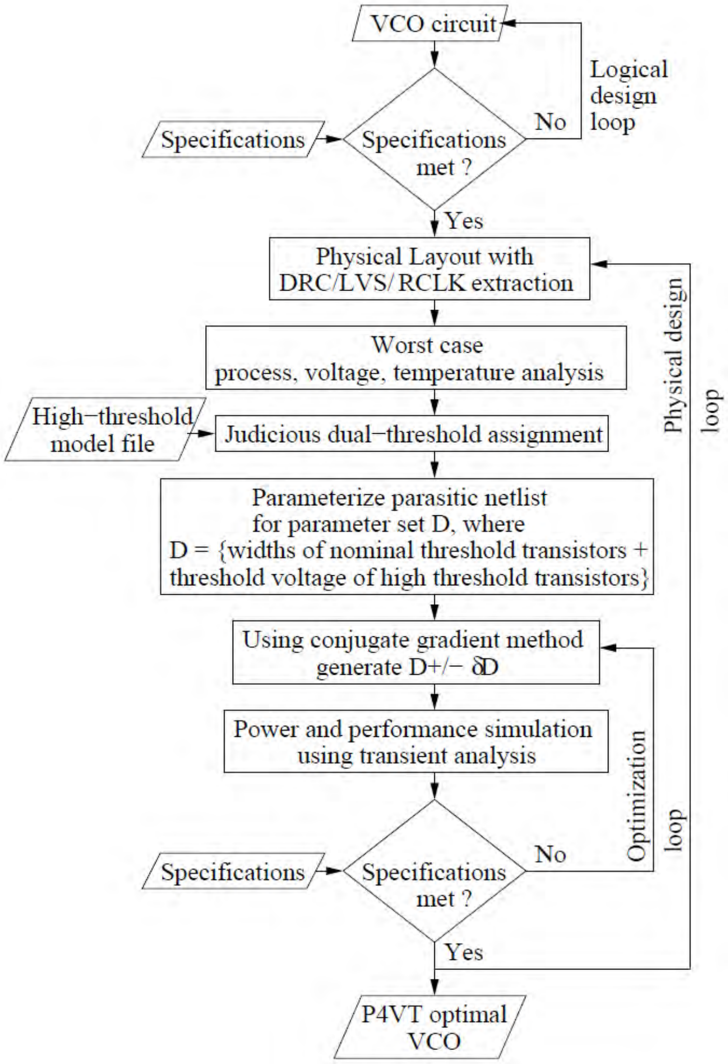
Proposed Novel P4VT Aware Design Flow …

- Logical design performed to meet the specifications.
- Preliminary physical layout subjected to DRC/LVS/RCLK.
- RCLK extracted physical design is subjected to process, voltage and temperature variation analysis.
- Dual-threshold assignment (HV_{Thn} , HV_{Thp}) to the power-hungry transistors of the VCO.

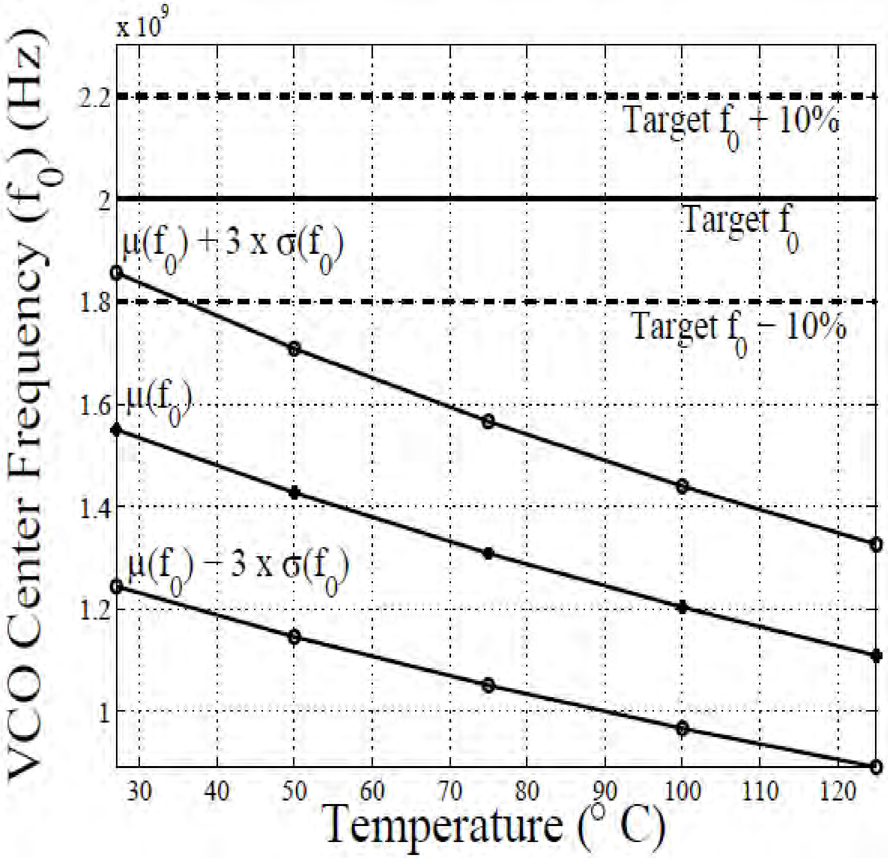


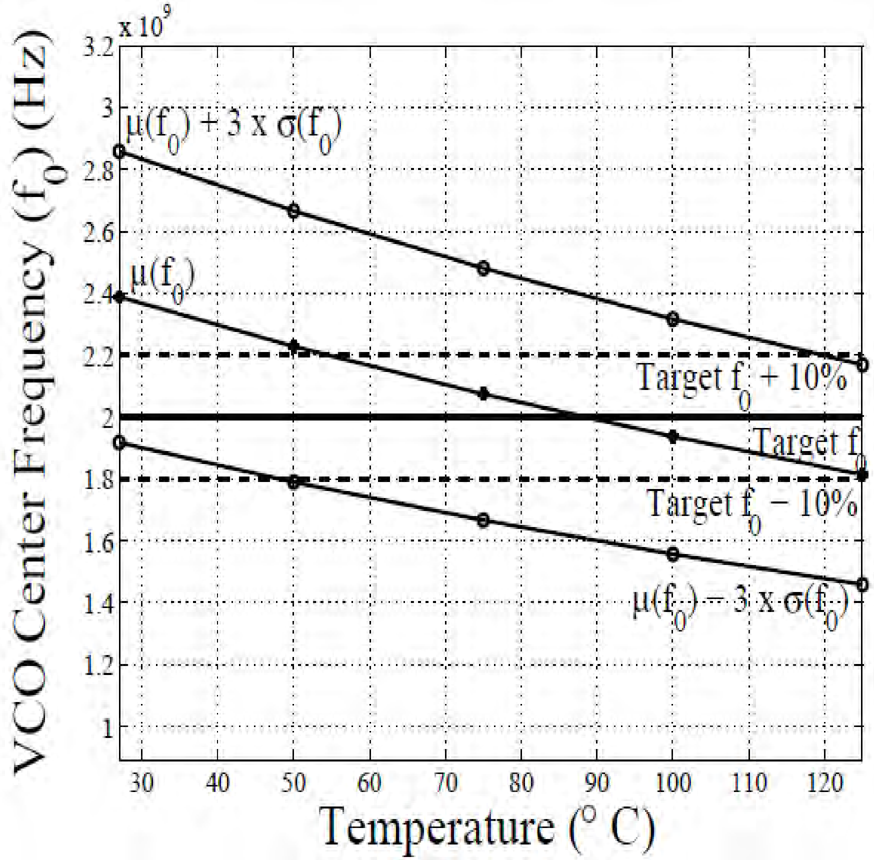
Proposed Novel P4VT Aware Design Flow

- Parasitic netlist is parameterized for parameter set D (widths of transistors and HV_{Thn}, HV_{Thp}).
- Parameterized netlist is subjected to optimization for *worst case PVT* variations.
- Parameter values for which the specifications are met are determined.
- Final physical design of the VCO is performed using these parameter values.



Center Frequency (f_0) vs. Temperature





- Non-Optimized VCO
- P4VT Optimized VCO

Logical Design of 90nm CMOS VCO

- Current starved VCO design performed using 90nm process. Following equations are used:

$$f_0 = \frac{I_D}{N * C_{tot} * V_{DD}}$$

$$C_{tot} = \frac{5}{2} C_{ox} (W_p L_p + W_n L_n)$$

$$C_{ox} = \frac{\varepsilon_{r_{ox}} \varepsilon_0}{T_{ox}}$$

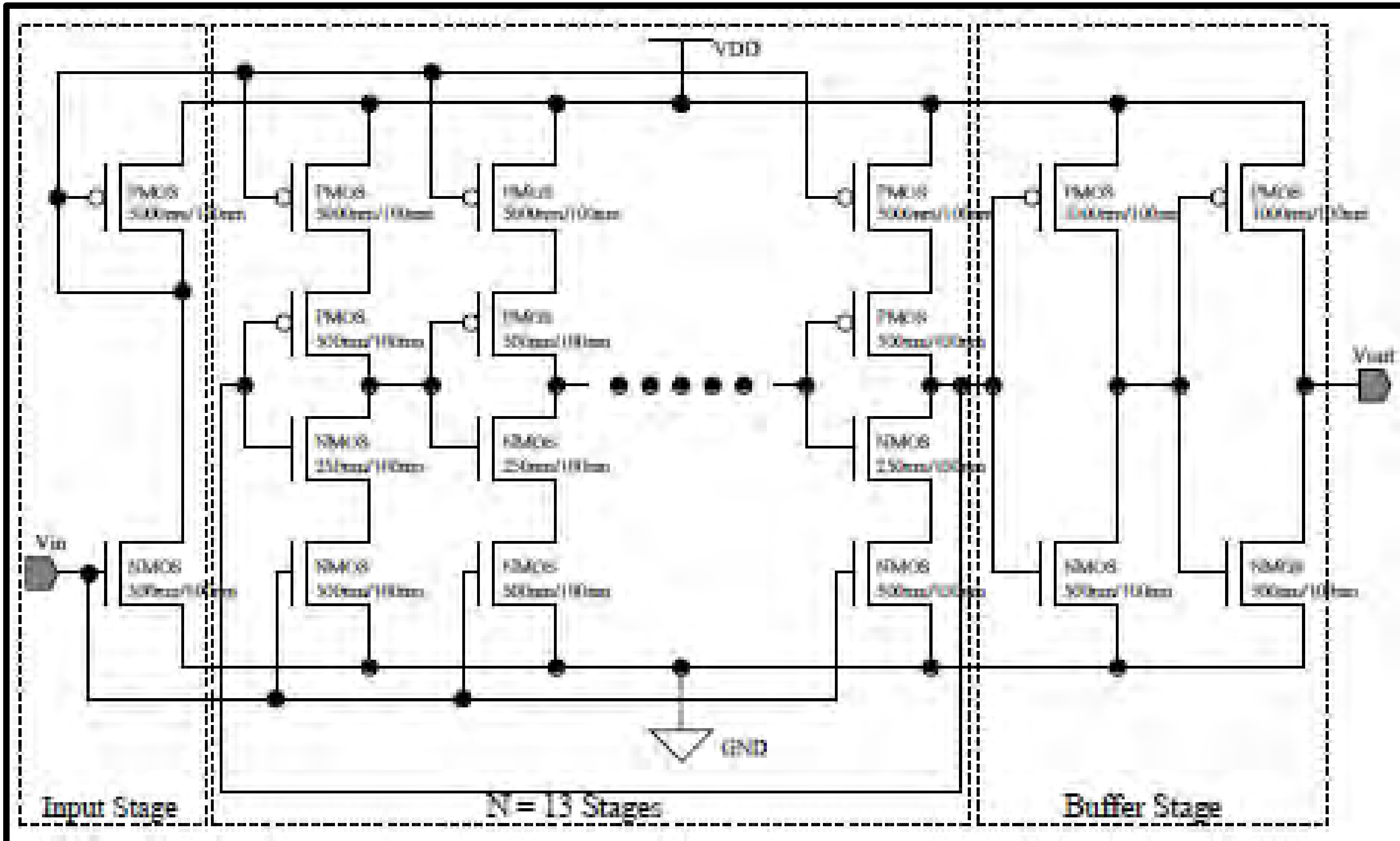
- V_{DD} : supply voltage, I_D: current flowing through inverter, N: odd number of inverters, C_{tot}: total capacitance of each inverter stage, C_{ox}: gate oxide capacitance per unit area.

Logical Design of 90nm CMOS VCO

- For a target oscillation frequency $(f_0) \geq$ 2GHz for 90nm node:

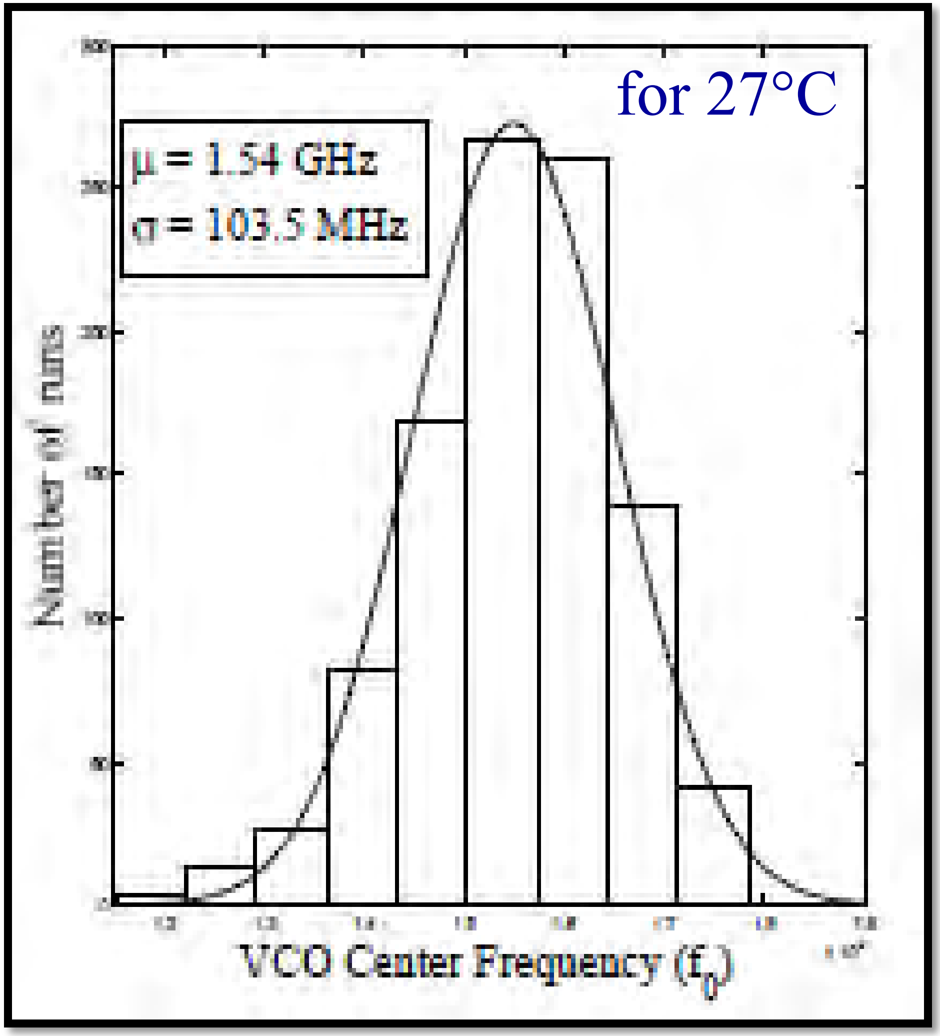
- {Wp, Lp}: inverter PMOS width (500nm) and length (100nm).
- {Wn, Ln}: inverter NMOS width (250nm) and length (100nm)
- {Wpcs, Lpcs}: current starved PMOS width (5um) and length (100nm)
- {Wncs, Lncs}: current starved NMOS width (500nm) and length (100nm).

Logical Design of 90nm CMOS VCO



PVT Variation Analysis of VCO

- Process-voltage variation analysis has been carried out on the initial physical design with parasitics (RLCK) extracted netlist.
- Monte Carlo simulation for 1000 runs performed for variation in 5 parameters:
  - V_{DD}: Supply voltage
  - V_{Thn}: NMOS threshold voltage
  - V_{Thp}: PMOS threshold voltage
  - Toxn: NMOS gate oxide thickness
  - Toxp: PMOS gate oxide thickness.
- for temperatures = 27°C, 50°C, 75°C, 100°C, 125°C.



PVT Variation Analysis of VCO

- The worst-case process variation is where V_{Thn}, V_{Thp}, Toxn, Toxp) are increased by 10%.
- The worst-case voltage variation is where VDD is reduced by 10%.
- The worst-case temperature variation is 125°C.

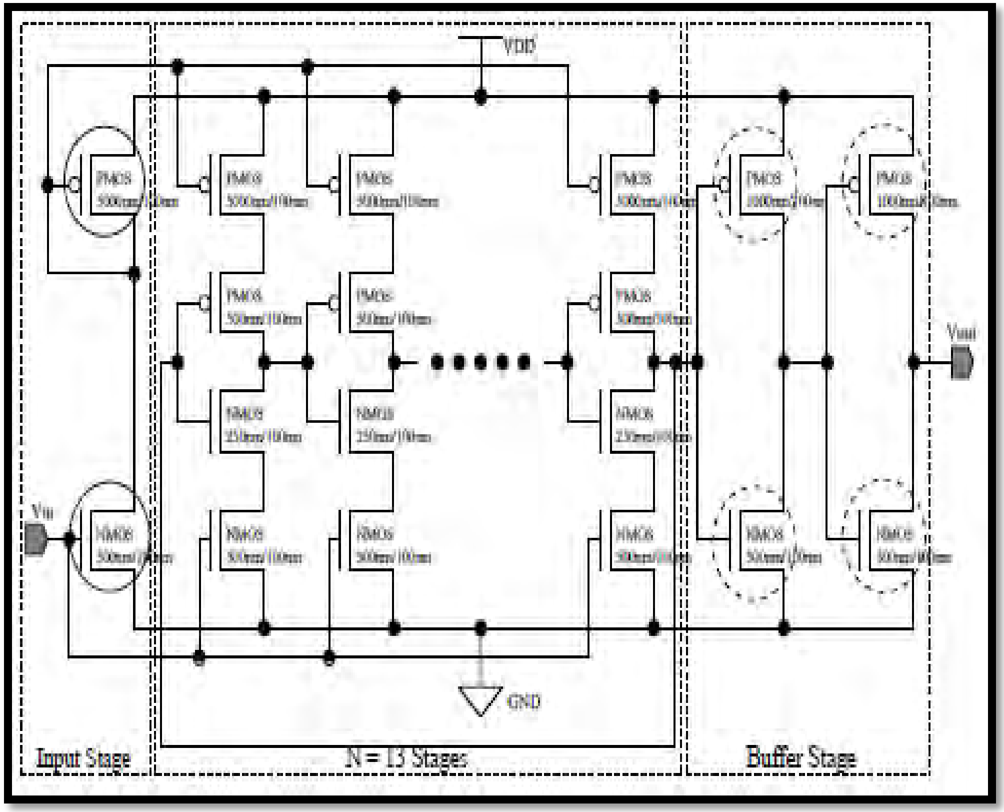
P4VT Optimization of VCO

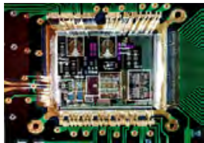
- Logical design center frequency $f_0 \geq 2$ GHz.
- Preliminary physical design center frequency f_{0p} = 1.56 GHz (25% degradation).
- Preliminary physical design center frequency in *worst case PVT* conditions f_{0pvt} = 1 GHz (50% degradation).
- Initial average power consumption (including leakage) (P_{VCO}) = 164.5μW.

Parameter	Initial Physical Design	Initial Physical Design + Process Variation	Final Physical Design + Process Variation
f_0	$1.56GHz$	$1.13GHz$	$1.98GHz$
discrepancy	25%	43.5%	1%
V_{DD}	$1.2V$ (nominal)	$1.08V$ (−10%)	$1.08V$
V_{tn}	$0.1692662V$ (nominal)	$0.186193V$ (+10%)	$0.186193V$
V_{tp}	$-0.1359511V$ (nominal)	$-0.149546V$ (+10%)	$-0.149546V$
T_{oxn}	$2.33nm$ (nominal)	$2.563nm$ (+10%)	$2.563nm$
T_{oxp}	$2.48nm$ (nominal)	$2.728nm$ (+10%)	$2.728nm$

Dual-Threshold Assignment in VCO …

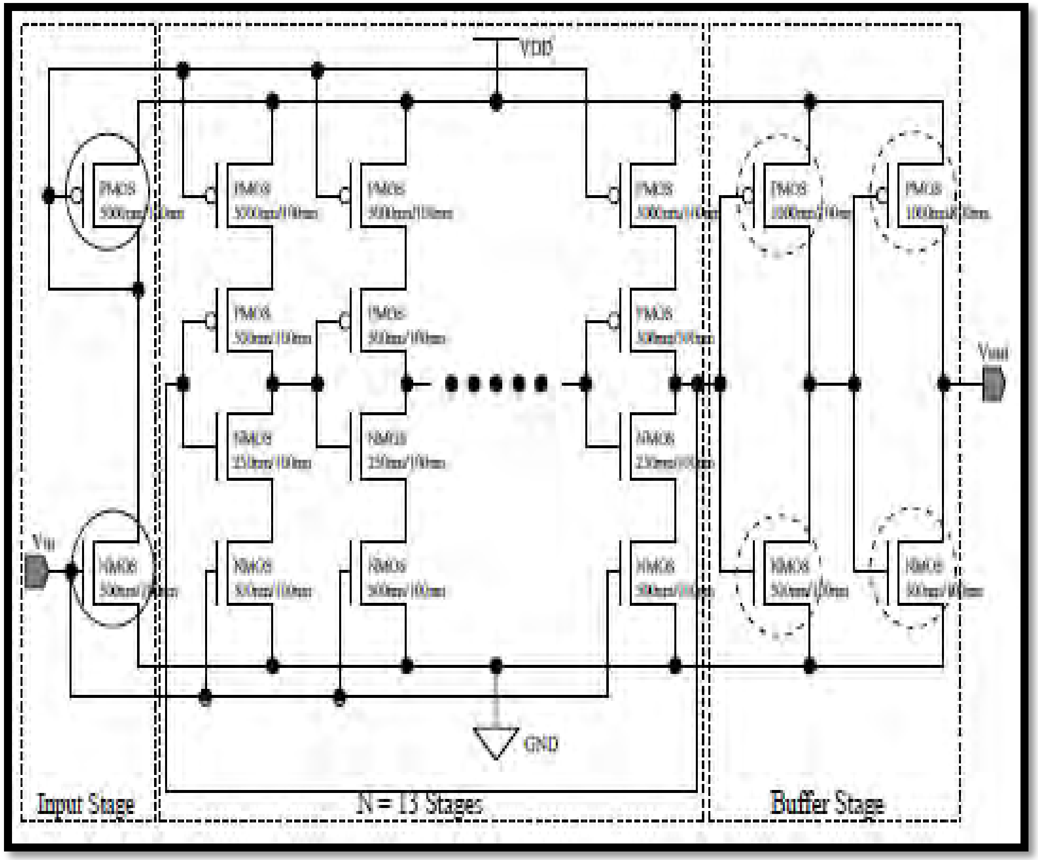
- Average power consumed by all the transistors is measured.
- Input stage transistors (shown by solid circles) consume 48% of total average power of the VCO circuit.
- Most suitable candidates for higher threshold voltage assignment (HV_{Thn}, HV_{Thp}).





Dual-Threshold Assignment in VCO

- The buffer stage transistors (shown by dashed circles) consume 11.5% of the total average power.
- May be treated to higher threshold voltage, for further power minimization.
- Input stage transistors follow *high threshold model file,* other transistors follow *baseline model file.*



Power-Performance Optimization in VCO …

- The parasitic aware netlist generated from the preliminary layout is parameterized with respect to the optimization parameter set D, which includes:
  - Widths of PMOS and NMOS devices in the inverter (Wn,Wp),
  - Widths of PMOS and NMOS devices in the current-starved circuitry (Wncs,Wpcs),
  - HV_{Thn}, HV_{Thp}.

Power-Performance Optimization

- The parameterized netlist is subjected to power-performance optimization using a conjugate gradient method.
- Our objective set are $f_0 \geq 2\text{GHz}$, and $P_{VCO} =$ minimum.
- S is the stopping criteria for the optimization to stop when the objective set is within $\pm\varepsilon$.
- ε is a designer specified error percentage.

One Optimization Algorithm

- **Input:** Parasitic aware netlist, Baseline model file, High threshold model file, Objective set $F = [f_0, P_{VCO}]$, Stopping criteria S, parameter set $D = [Wn, Wp, Wncs, Wpcs, HV_{Thn}, HV_{Thp}]$, Lower design constraint C_{low}, Upper design constraint C_{up}.
- **Output:** Optimized objective set F_{opt}, Optimal parameter set D_{opt} for $S \leq \pm\varepsilon$, {where ε=10%}.
- Perform first iteration with initial guess of D.
- **while** ($C_{low} < D < C_{up}$) **do**
- Using conjugate gradient, generate $D' = D \pm \Delta D$ in the direction of travel of $F_{opt} \pm \varepsilon$.
- Compute objective set $F(D') = [f_0, P_{VCO}]$.
- Compute S as the difference of target objective set and current objective set.
- **if** $S \leq \varepsilon$ **then**

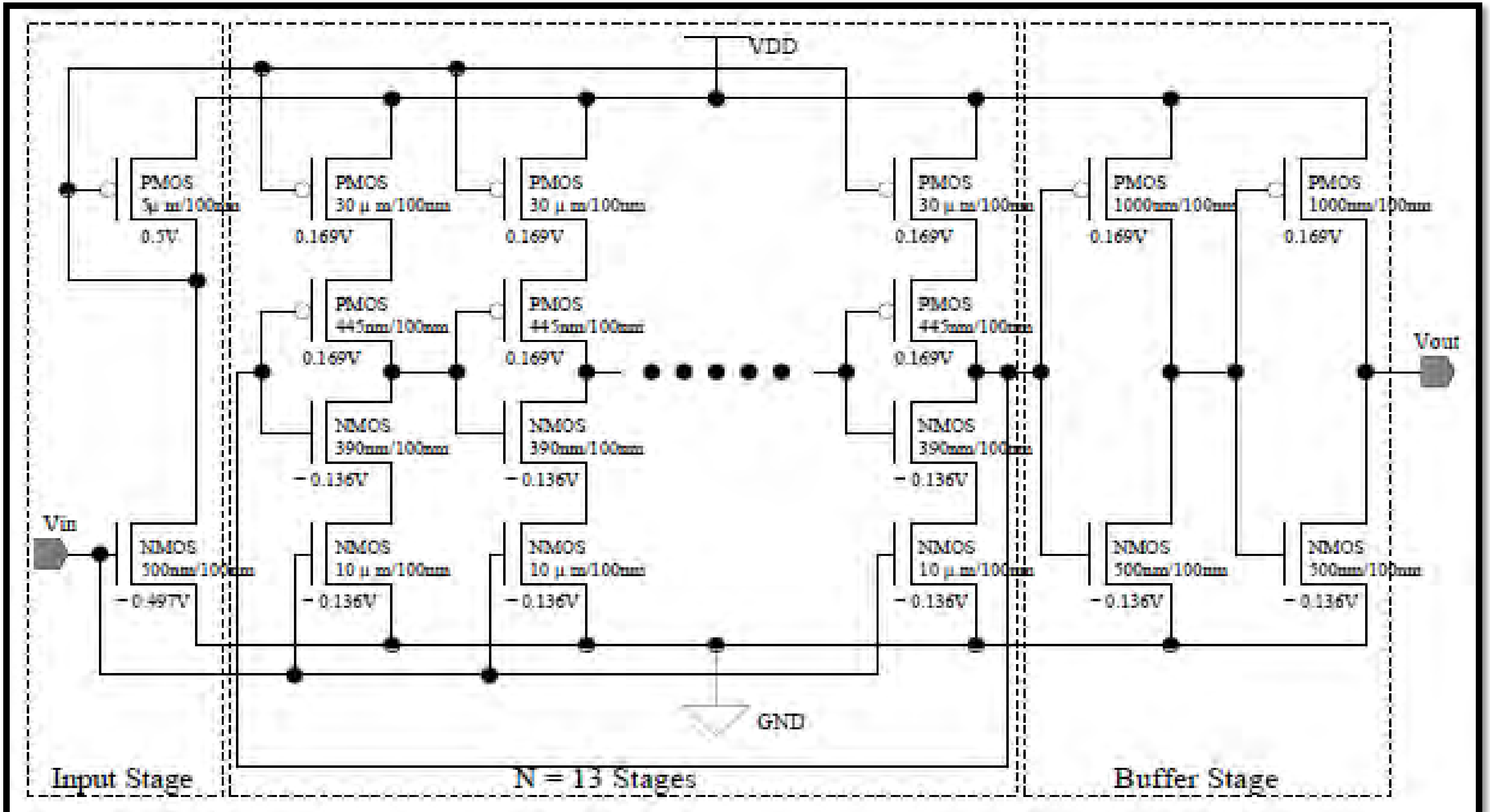
  {stopping criteria is within the error margin}
- **return** $D_{opt} = D'$.
- **end if**
- **end while**
- Using D_{opt}, construct final physical design and simulate.
- Record F_{opt} accounting the full-blown parasitics.

Optimization Results

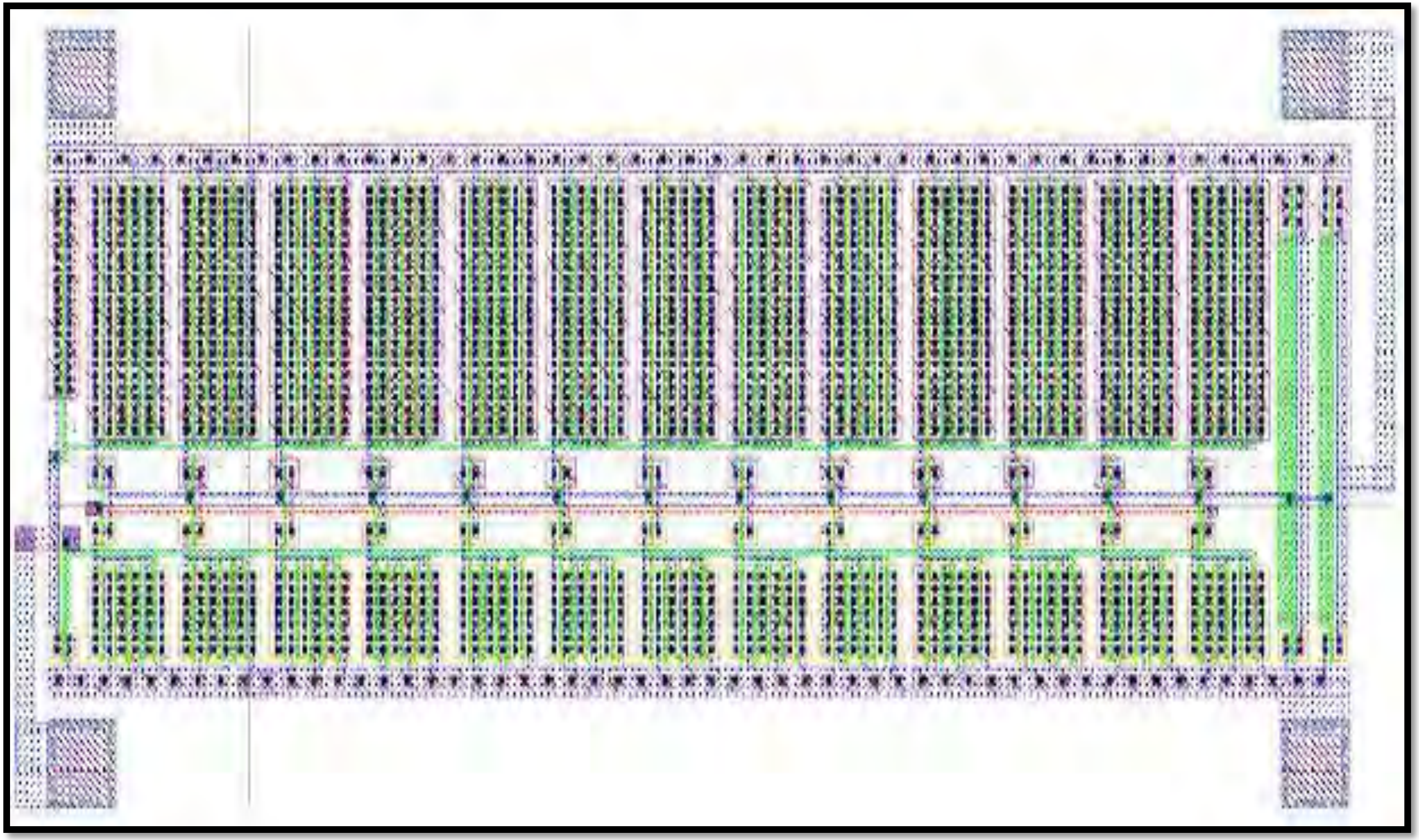
- Target center frequency $f_0 \geq 2GHz$.
- Final Physical design center frequency $f_{0p} = 2.4GHz$.
- Final Physical design center frequency in a worst case PVT conditions $f_{0pvt} = 1.8GHz$ (10% discrepancy).
- Final average power consumption (including leakage) (P_{VCO}) = 137.5μW (16.4% reduction).

D	C_{low}	C_{up}	D_{opt}
Wn	200nm	500nm	390nm
Wp	400nm	1μm	445nm
Wncs	1μm	50μm	10μm
Wpcs	5μm	50μm	30μm
Toxpth	0.1692662V	0.5V	0.5V
Toxnth	-0.5V	-0.1359511V	-0.4975V

P4VT Optimal Dual-Threshold VCO Circuit



P4VT Optimal Dual-Threshold VCO Layout



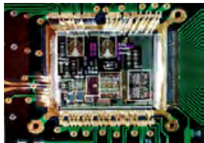
P4VT-Aware Performance of VCO

Parameter	Value
Technology	$90nm$ CMOS $1P$ $9M$
Supply Voltage (V_{DD})	$1.2V$
Center frequency (Nominal PVT)	$2.4GHz$
Worst case PVT	V_{Th} (+10%), T_{ox} (+10%), V_{DD} (−10%), $125^{\circ}C$
Center frequency (worst case PVT)	$1.8GHz$
Parameter set	6 (W_n, W_p, W_{ncs}, W_{pcs}, HV_{Thn}, HV_{Thp})
Number of objectives	2 ($f_0 \geq 2GHz$, P_{VCO}=$minimum$)
Area occupied	$547.74\mu m^2$ (58.3% penalty)

UNT
UNIVERSITY OF NORTH TEXAS
Discover the power of ideas

Summary and Conclusions …

- Design of a Power-Performance-Parasitic-Process-Voltage-Temperature (P4VT) optimal nano-CMOS VCO is proposed.
- The presented design flow is used on top of existing physical design tools.
- The center frequency treated as the target specification.
- The degradation of the center frequency due to worst-case PVT effects narrowed down from 50% to 10%.



Summary and Conclusions

- 16.4% power minimization is achieved using dual-threshold technique.
- The end product of the proposed design flow is a P4VT optimal dual-threshold VCO physical design that meets the functional specifications across entire temperature range.
- For future research, we plan to incorporate additional performance criteria to the optimization set, such as phase noise.