Lecture 8: Process Variation Tolerant Sense Amplifier Design

CSCE 6933/5933
Advanced Topics in VLSI Systems

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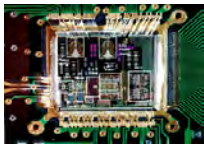
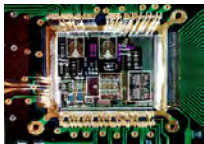


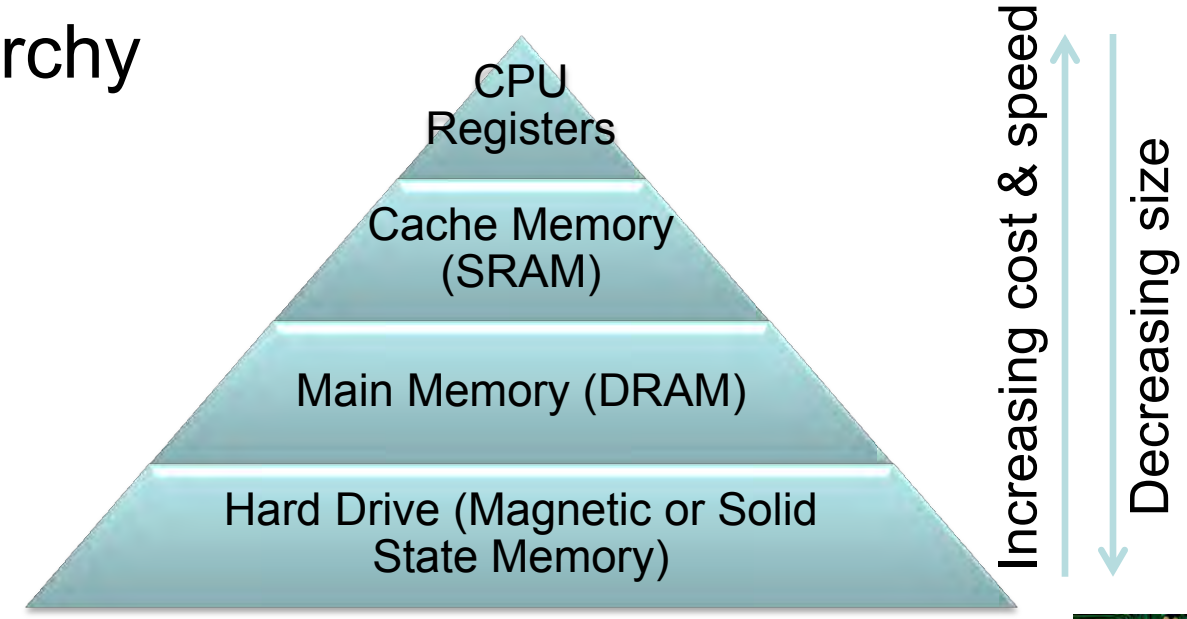
Outline

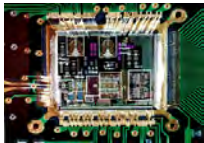
- Introduction
- Related Prior Research
- Functional Design of Sense Amplifier Circuits
- Design Optimization – Dual Oxide Technique
- Design Optimization – Dual Threshold Voltage Technique
- Conclusions



Introduction

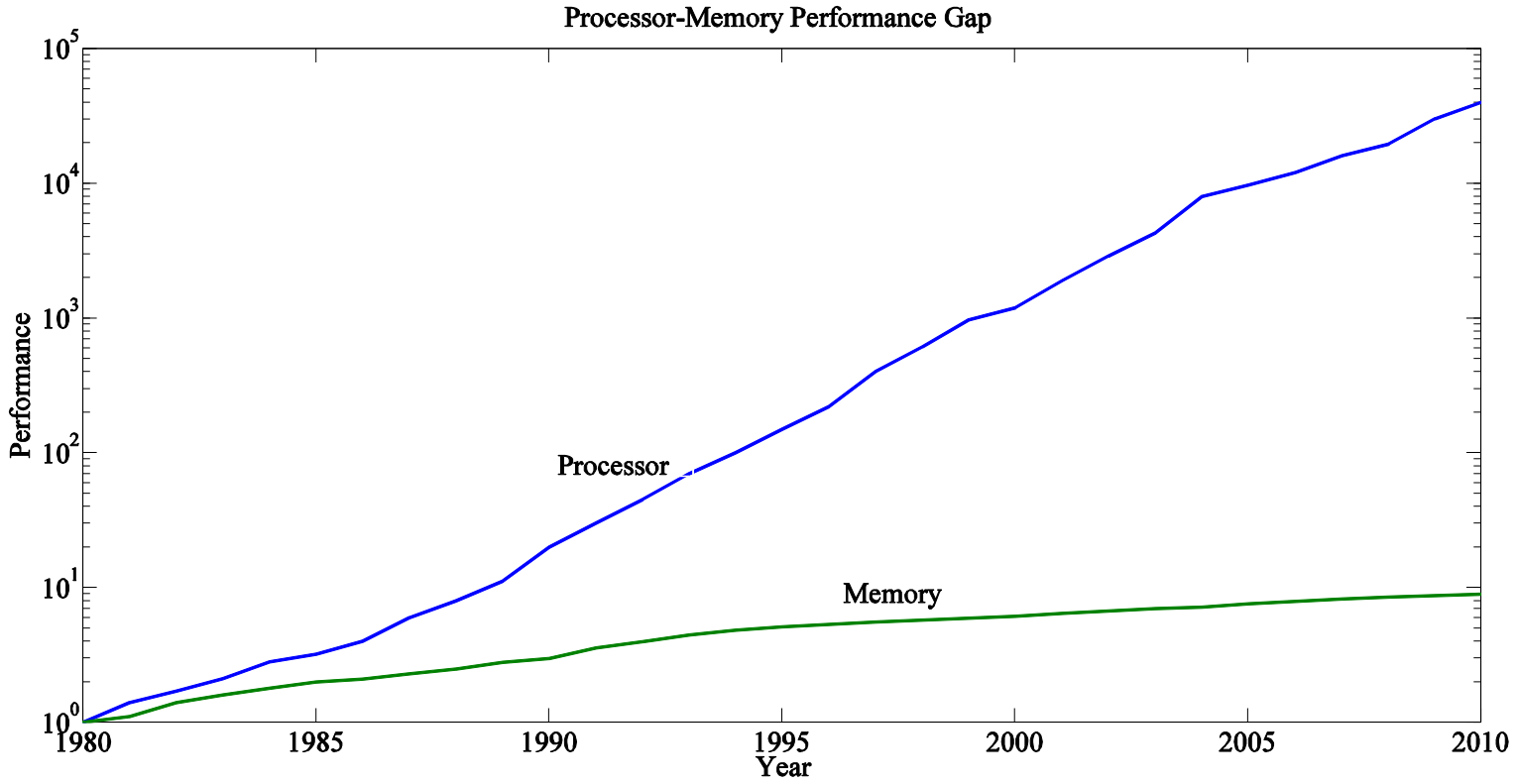
- Dynamic Random Access Memories (DRAMs) are important parts of computing systems
- Relatively fast but not as fast as SRAMs
- Densely Packed
  - 4 times denser than SRAM
- Memory Hierarchy

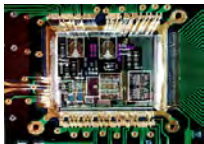




Motivation

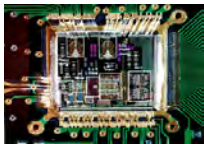
- Memory keeps lagging CPU speed performance





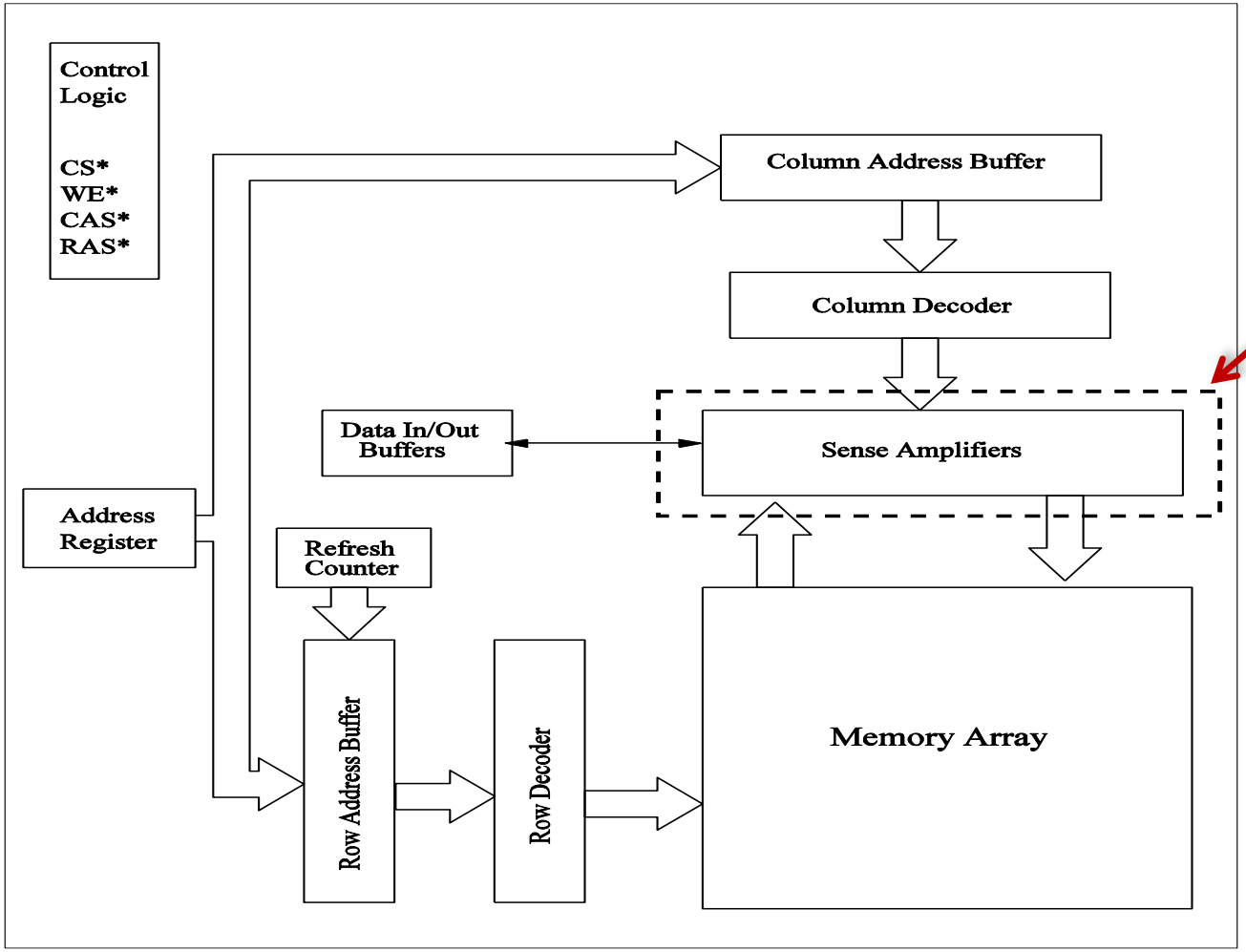
Introduction: Background

- Historical background
- 1K DRAM designed in 1970
  - Used 3-T cells
- 4Kb – 64Mb DRAM
  - Used 1T-1C cells
  - CMOS technology
  - Multiplexed addressing
- Gb-SDRAM Era (Current Technology)
  - Access synchronized with master clock

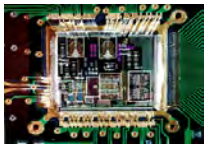


Background

- Basic Organization of DRAM

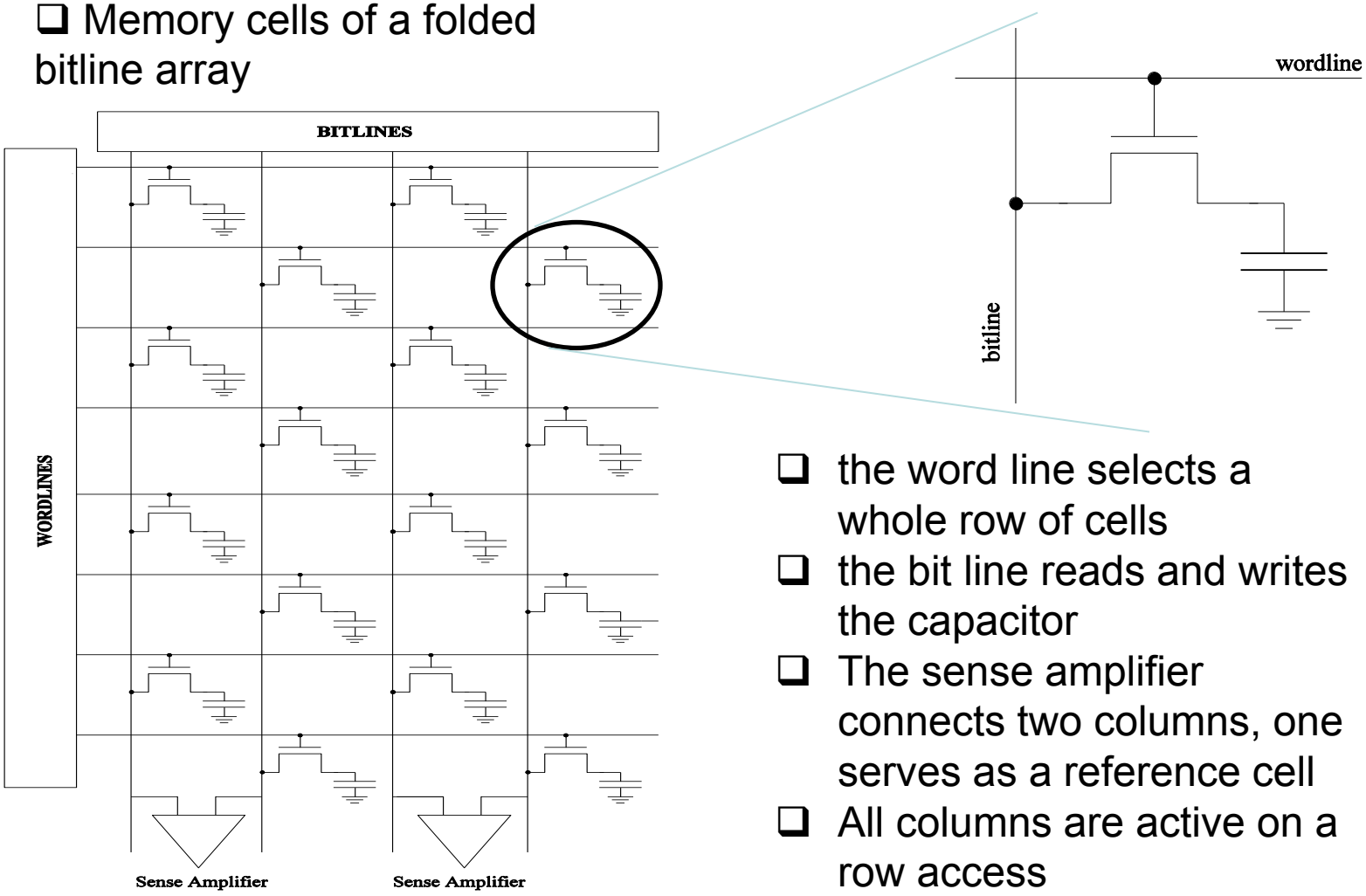


Focus of this thesis

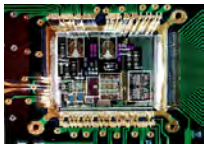


Memory Array

- Memory cells of a folded bitline array

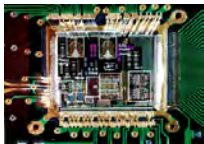


- the word line selects a whole row of cells
- the bit line reads and writes the capacitor
- The sense amplifier connects two columns, one serves as a reference cell
- All columns are active on a row access



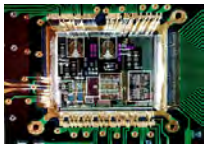
Sense Amplifier: Background and Operation

- Major Functionality:
  - Detect and amplify voltage change
  - Refresh circuit
  - Act as column buffers
- Basic Access Operations
  - To access (read or write to a cell) there are three basic operations performed – the precharge, row and column access.
  - The precharge phase charges all bitlines to a determined voltage, usually $V_{DD}/2$.



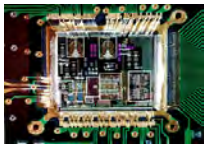
Sense Amplifier: Background and Operation

- For a read operation,
  - The row access activates the wordline of the cell and all the capacitors begin to share charge with the bitlines.
  - Sense amplifiers sense and magnify voltage changes.
  - The data from the sense amplifier is selected by the column bit during the column access.
- Write Operation.
  - The row access activates the wordlines.
  - The bitline drives the the cell to a “0” or “1” depending on the value to be written.
- Refresh Operation: This is done by reading every address of the DRAM.



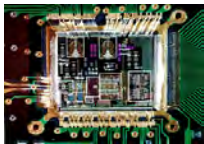
Issues in Nanoscale DRAM Circuit Design

- Variability: Variability in process and design parameters becomes more acute due to scaling technologies and processes
- Leakage: Leakage is increasing due to scaling of oxide thickness
- Power Consumption : current leakage increases the static power consumption



Process Variation

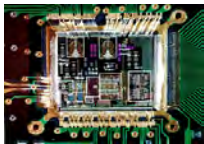
- Process variations occur due to different manufacturing environments and process difficulty
- The effects of the process variation result in varying device parameters including:
  - supply voltage,
  - threshold voltages,
  - oxide thickness,
  - transconductance,
  - channel lengths,
  - channel widths, and
  - source and drain doping concentration



Process Variations Classifications

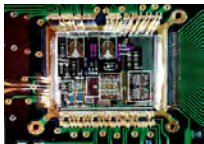
Global Variations

Fabrication Process	Lot Process	Wafer Process
From plant to plant	From lot to lot in a plant	From wafer to wafer in a lot



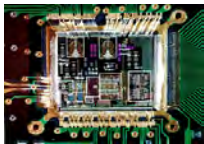
Salient Points of this Design Flow

- Analysis of effects of device parameters on FoMs of a sense amplifier.
- Analysis of effect of process variation on the performance of full latch sense amplifier.
- Design process to limit the effects of process variations with optimizations to FoMs.
- Exploring dual-Tox and dual-Vth for sense amplifier optimization.



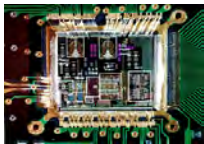
Related Prior Research

Research	Parameter	Feature	Approach	Result Improvement
Sherwin	V_{DD}	Voltage gain	Physical measurements	-
Chow	C_{BL}	Sense Speed	Spice simulations	Sense speed – 40%
Laurent	C_{BL}, V_{th}, β	Signal Margin	Spice Simulations	-
Vollrath	C_{BL}, V_{th}, β	Signal Margin	Physical measurements	-
Choudhary	V_{th}, L, W	Yield	Monte Carlo analysis	Improved Yield
Hong	-	Sense scheme	Spice simulations	Improved sense amplifier cell ration
Singh		SE rise time	Spice simulations	Eliminated offset voltage
This research	Dual-V_{th}	Process variability	Optimization	Sense delay – 80.2% Sense margin – 61.9%



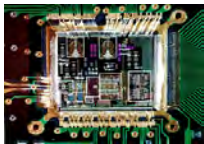
Sense Amplifiers Topologies

- Voltage Based Sense Amplifiers
  - Sense and amplify a small differential voltage
  - Variations include cross couple and full latch cross couple
- Current Based Sense Amplifiers
  - Sense and amplify small differential currents
  - Lower input capacitance
  - Includes current-mirror, clamped bitline current amplifier



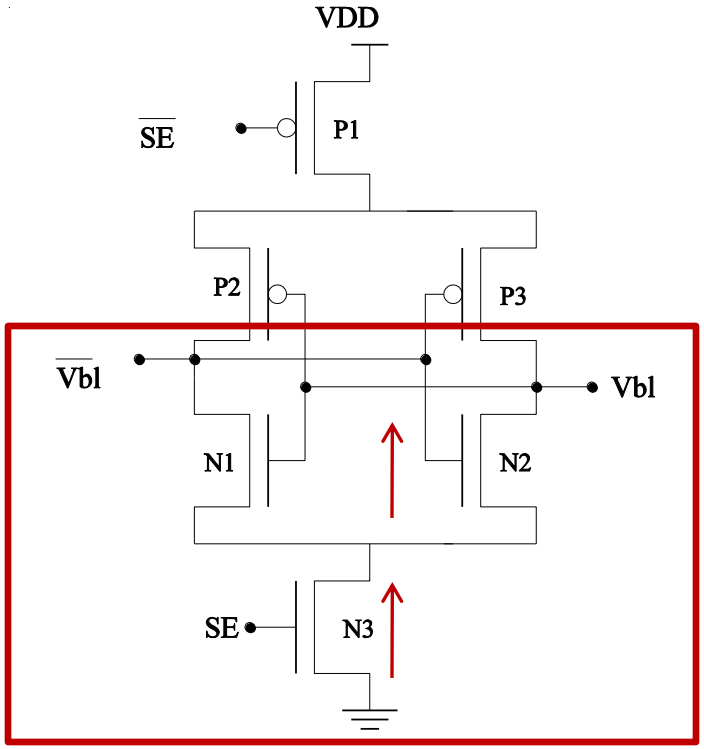
Functional Design of Sense Amplifier

- Two cross coupled inverters
- The major parts of the full latch voltage sense amplifier are
  - Nsense Amps
  - Psense Amps
  - Precharge and Equalization Circuits



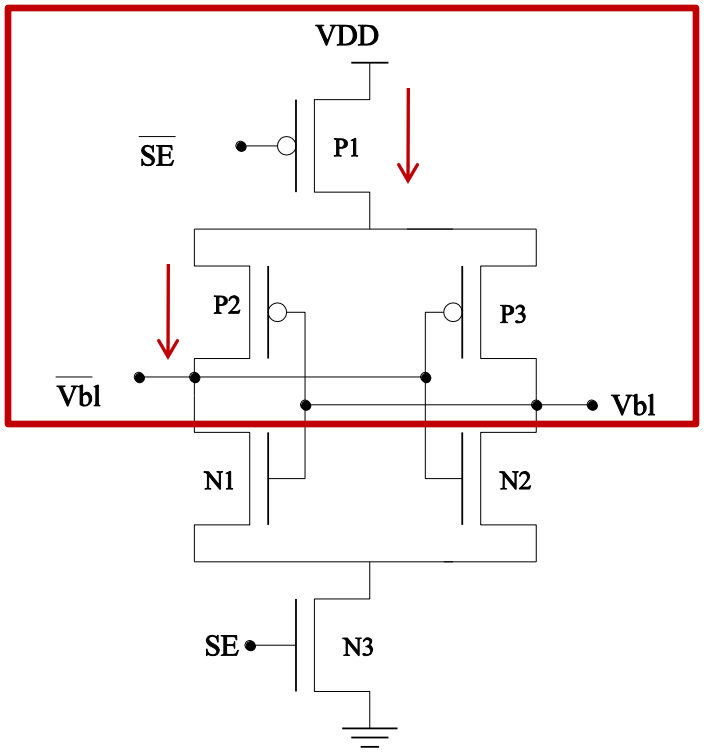
Nsense and Psense Amplifiers

- Nsense amplification

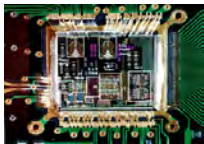


- Nsense amplifiers activated by SE through N3
- N2 begins to conduct and eventually pulls V_{bl} to ground

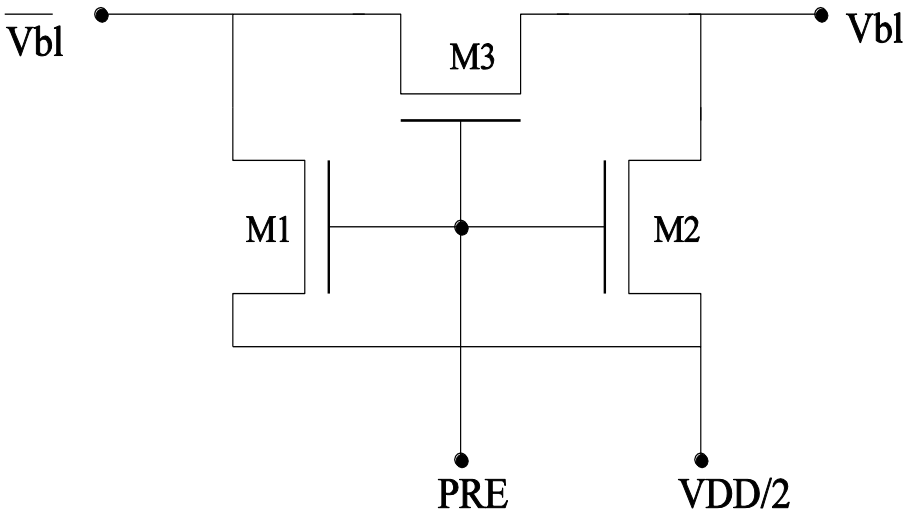
- Psense amplification



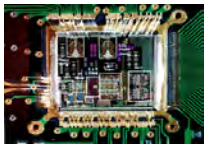
- Psense amplifiers activated by SEbar through P1
- P2 begins to conduct and eventually pulls V_{bl}bar to ground



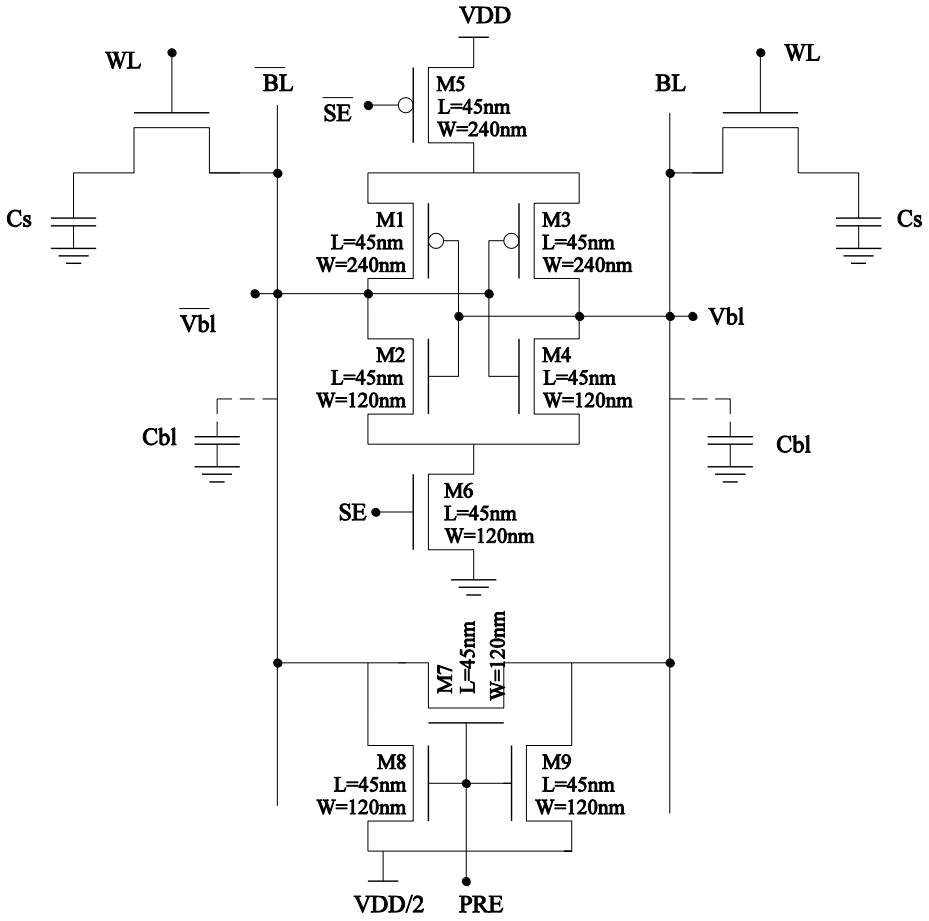
Precharge Circuit



- When PRE signal goes high, Vbl and Vblbar are charged to VDD/2 through M1 and M2 Psense amplifiers activated by P1
- M3 Helps to speed up the process



Functional Design of Sense Amplifier



Equations for Charge Sharing

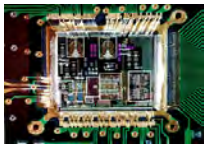
$$\Delta V = \frac{C_S}{C_S + C_{BL}}\left(V_{CS} - \frac{V_{DD}}{2}\right)$$

when bit cell value is 1, $V_{CS} = V_{DD} - V_{th}$

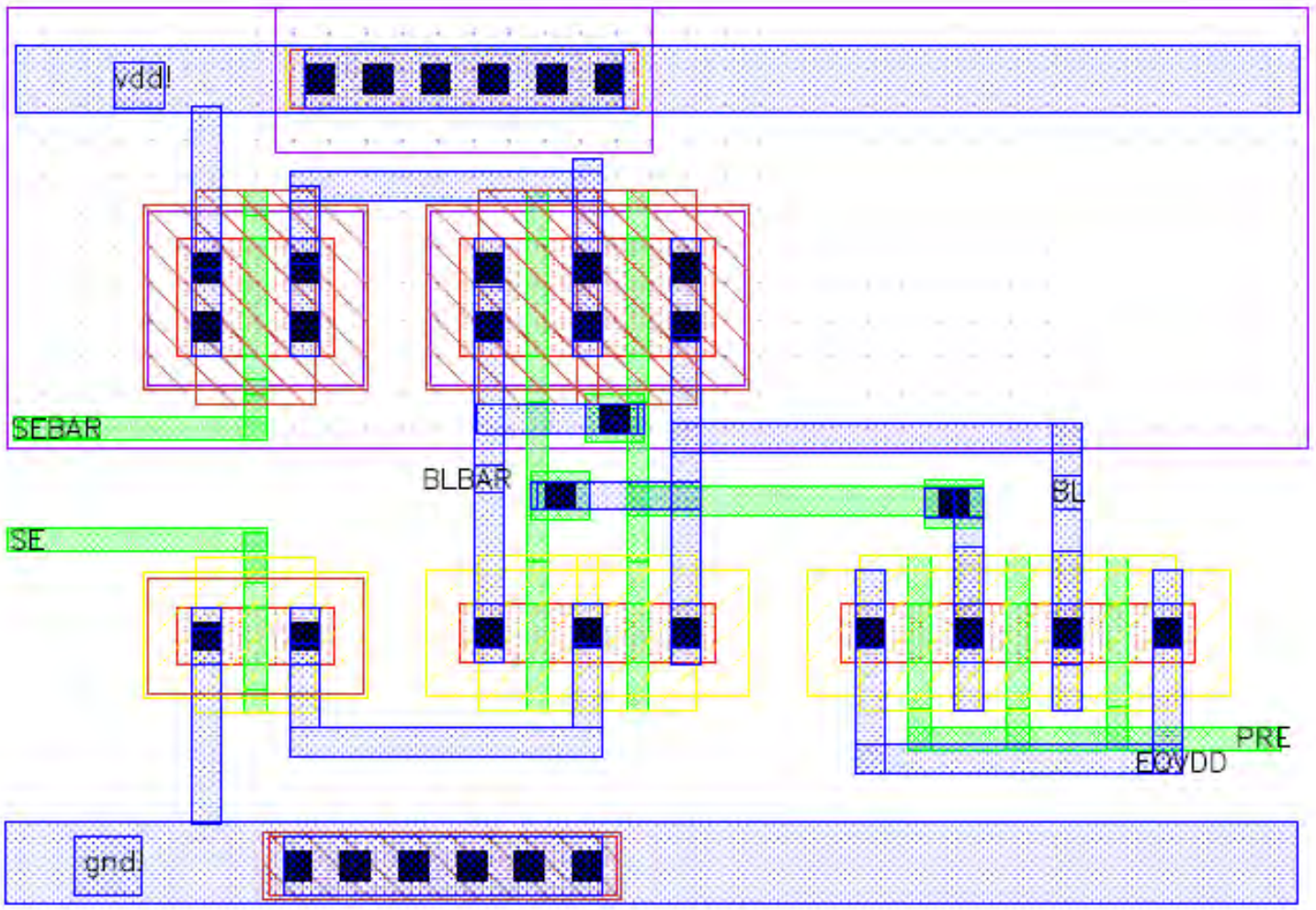
$$\Delta V \approx \frac{C_S}{C_{BL}}\left(\frac{V_{DD}}{2} - V_t\right)$$

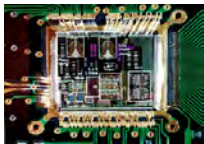
when bit cell value is 1, $V_{CS} = 0$

$$\Delta V \approx -\frac{C_S}{C_{BL}}\left(\frac{V_{DD}}{2}\right)$$

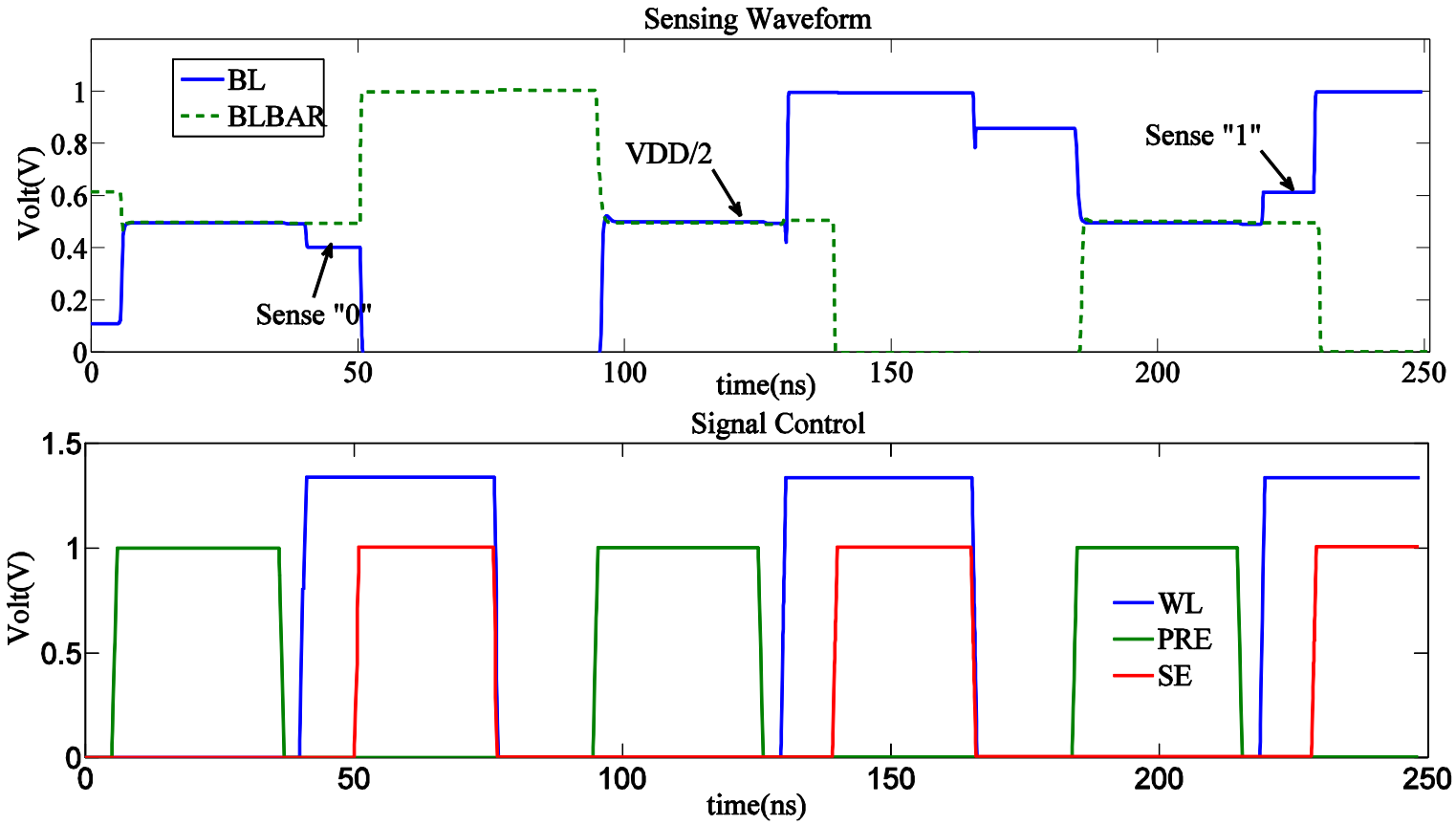


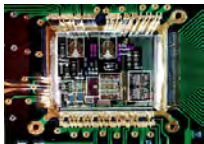
Physical Layout for 45nm Sense Amplifier





Waveform Simulation



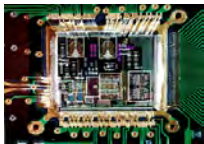


Figures of Merit

- Precharge and Equalization Time
- Average Power Consumption
- Sense Delay
- Sense Margin

Table for Figures of Merit Characterization

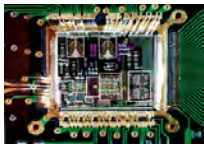
FoM	Precharge	Power	Sense Delay	Sense Margin
Value	7.50 ns	153.101 mW	4.39 ns	43.46 mV



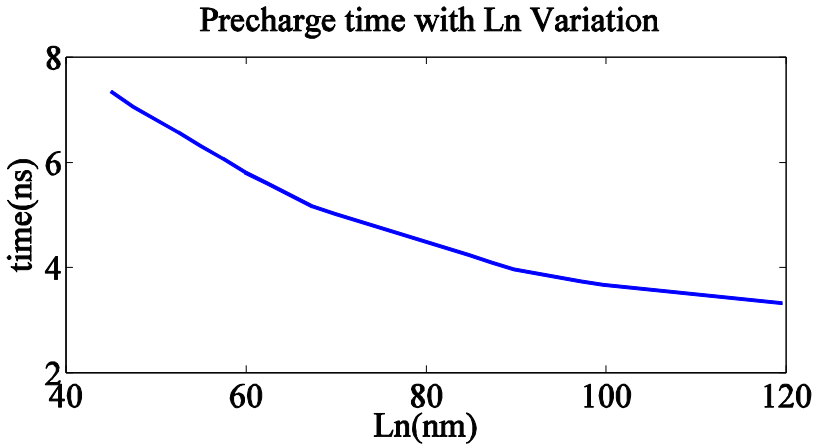
Parametric Analysis

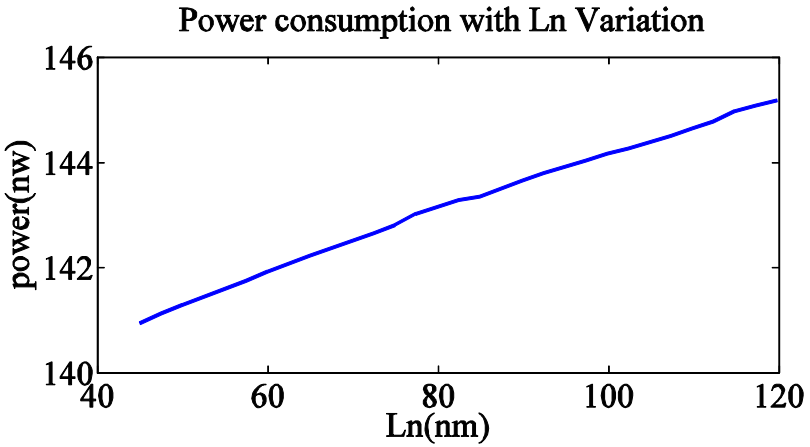
The following parameters analysed

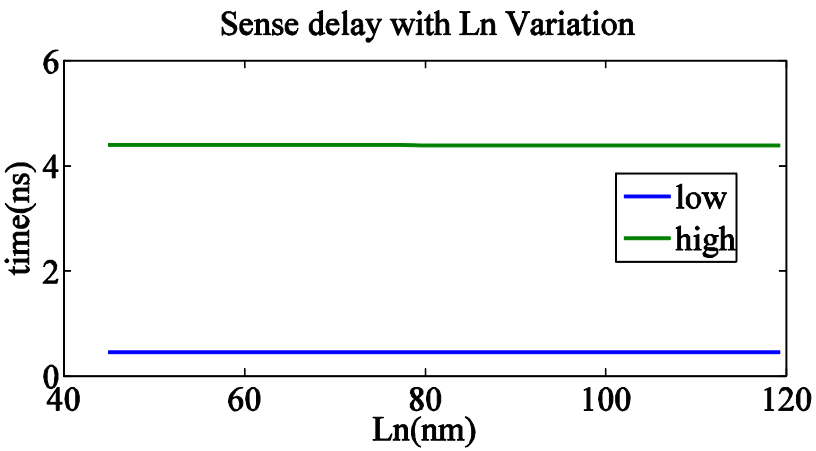
- Gate Lengths and Widths (L_n, L_p, W_n, W_p)
- Voltage Supply (V_{DD})
- Cell Capacitance (C_S)
- Bitline Capacitance (C_{BL})
- Oxide Thickness (T_{oxn},T_{oxp})
- Threshold Voltage (V_{thn}, V_{thp})

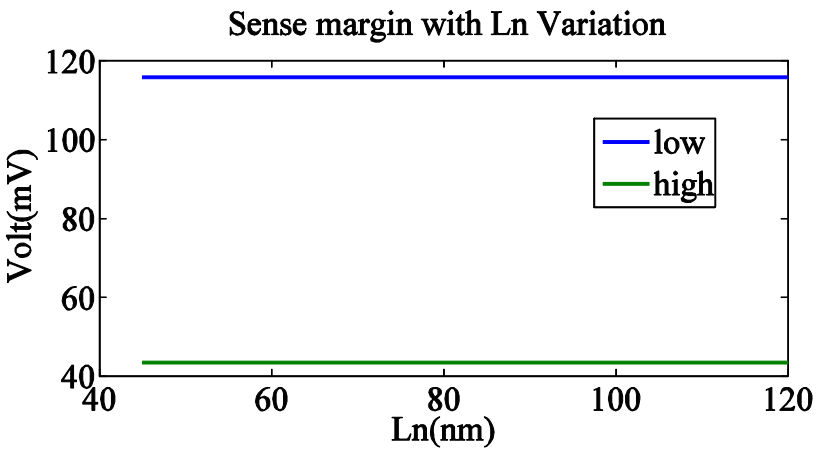


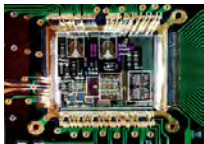
Sensitivity of FoMs on Ln



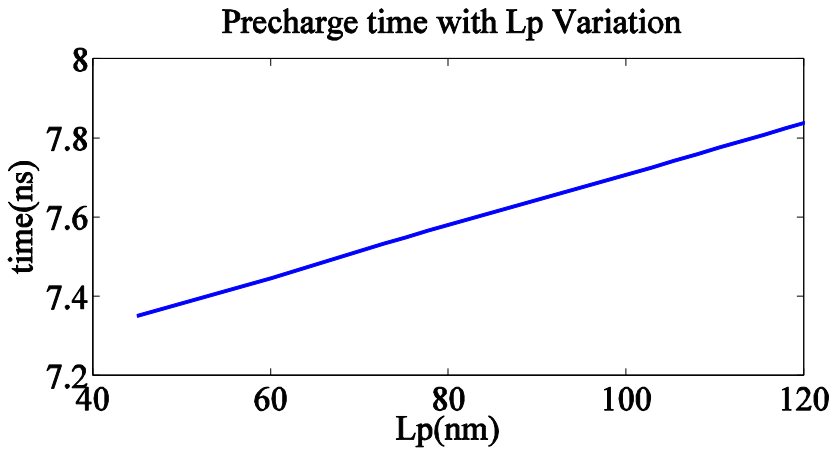


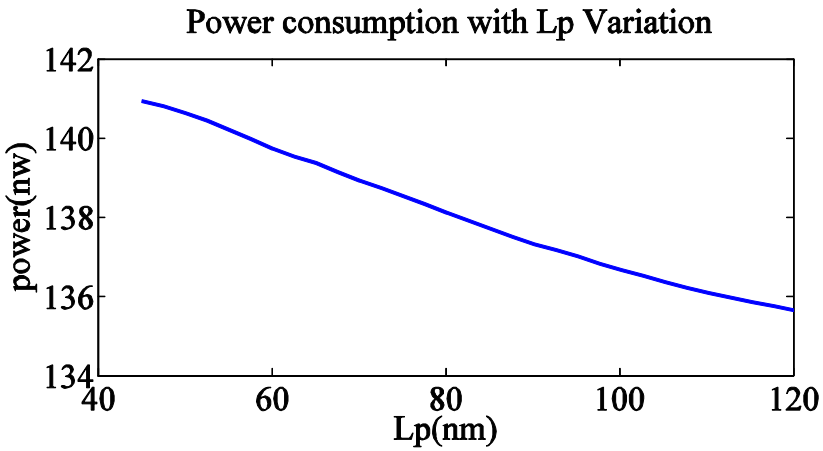


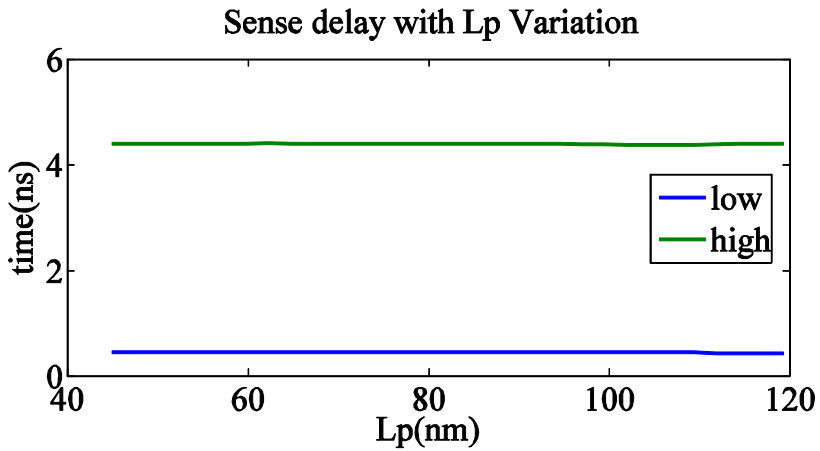


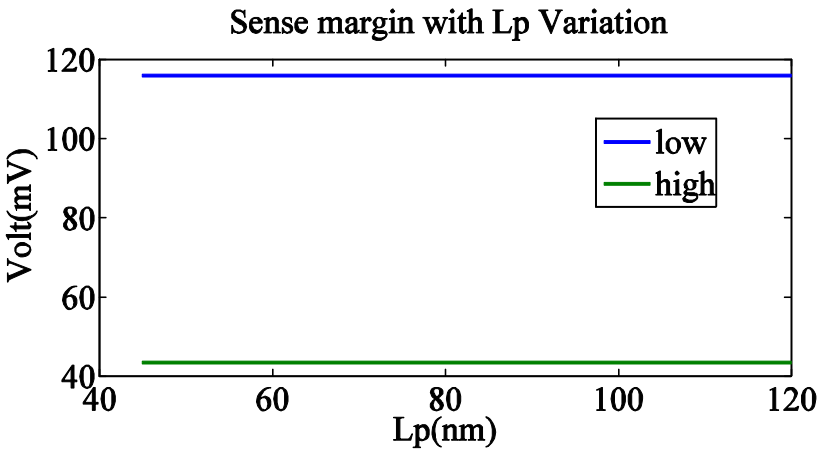


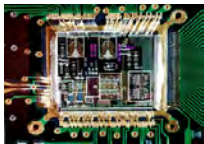
Sensitivity of FoMs on Lp



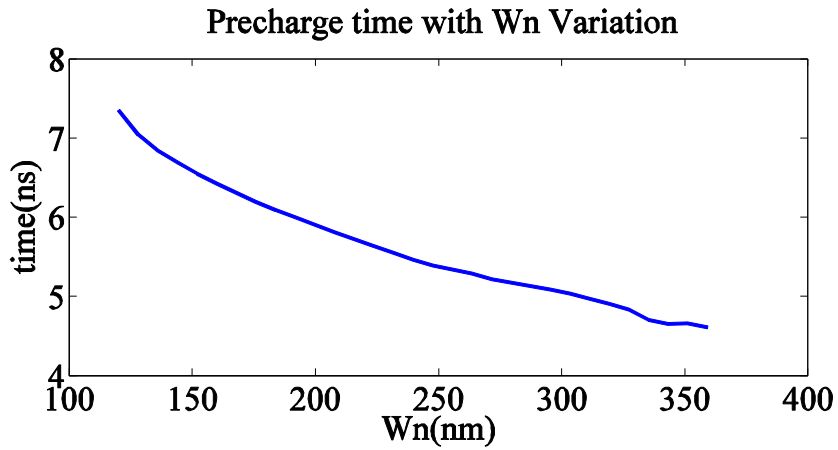


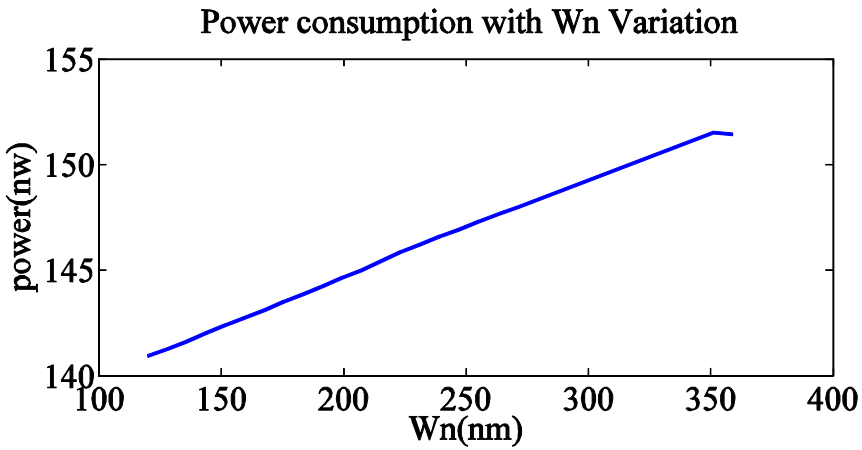


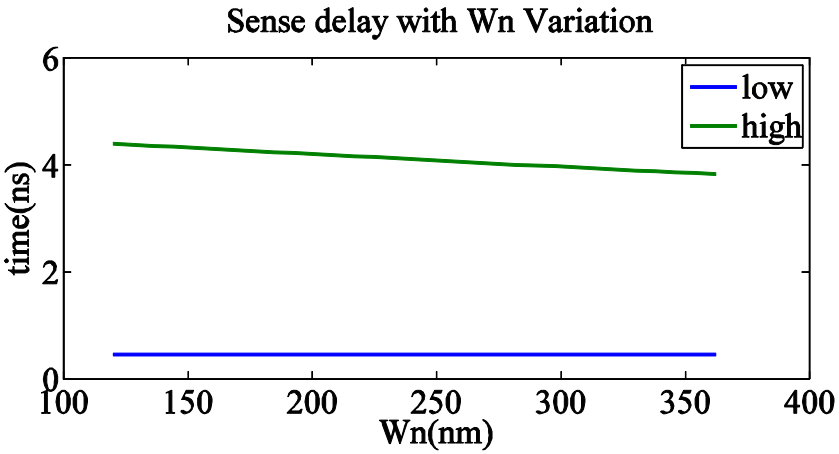


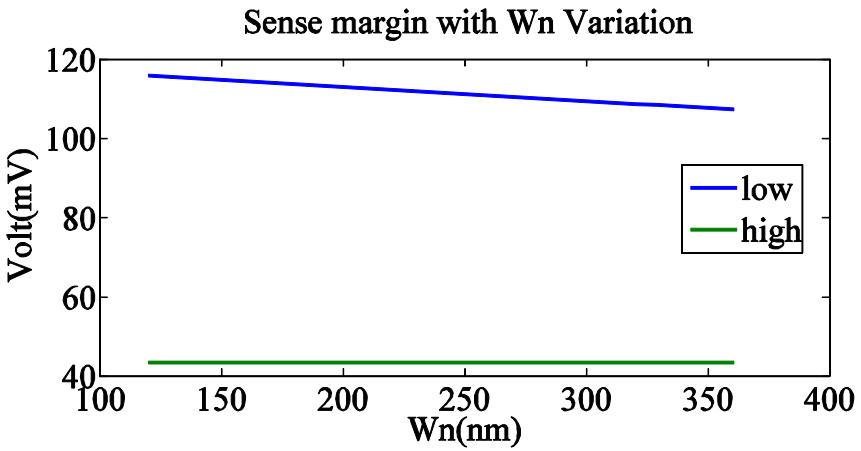


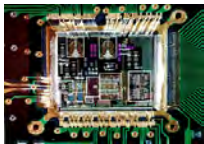
Sensitivity of FoMs on Wn



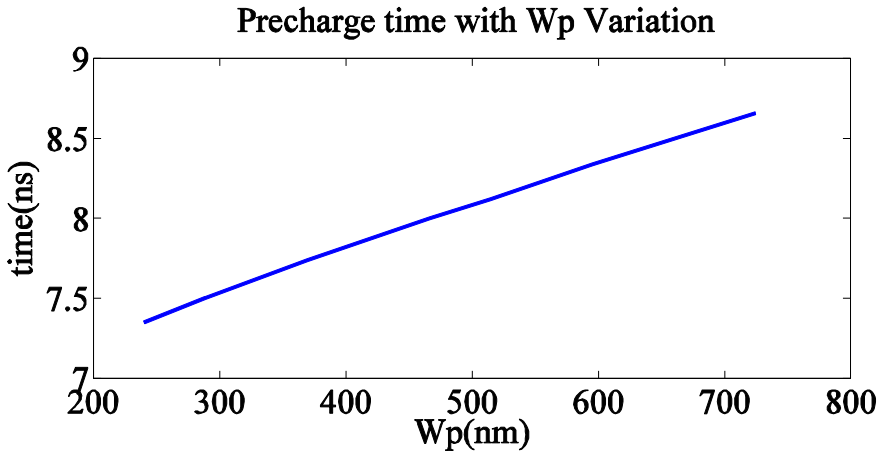


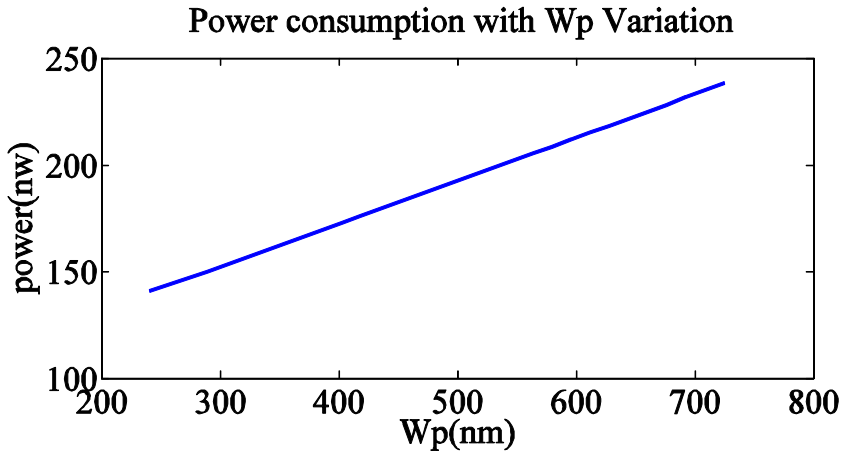


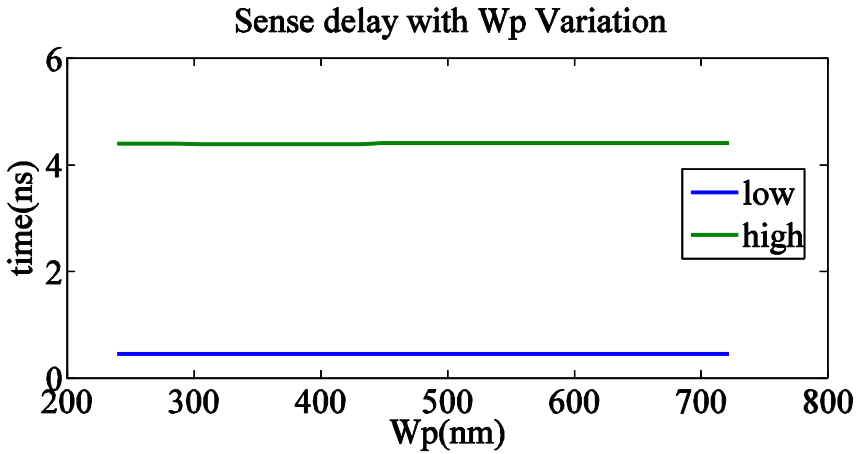


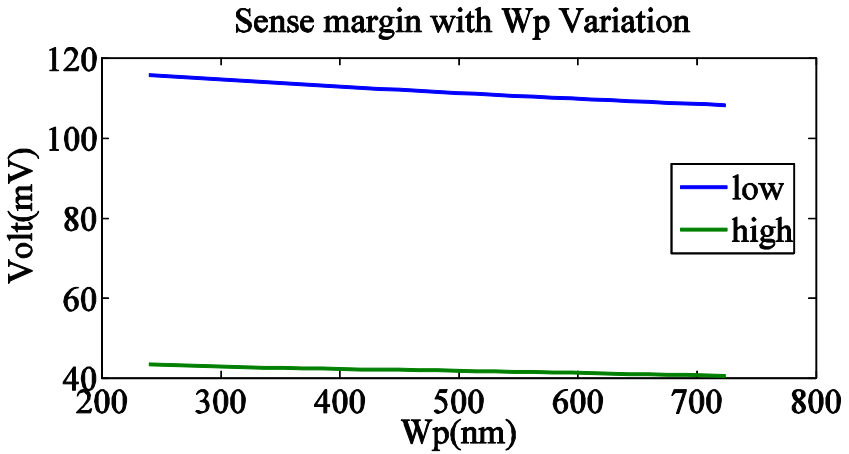


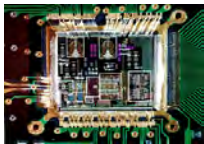
Sensitivity of FoMs on Wp







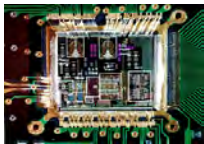




Summary of Effects of Parameter Variations on FoMs

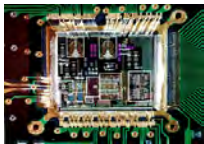
- Table of Parameter Variations

Parameter	Precharge	Power	Sense Delay	Sense Margin
L_n	decrease	increase	mild decrease	mild increase
L_p	increase	decrease	mild decrease	mild decrease
W_n	decrease	increase	decrease	decrease
W_p	increase	increase	mild decrease	decrease
V_{DD}	decrease	increase	decrease	increase
C_S	increase	increase	decrease	increase
C_{BL}	increase	increase	mild increase	decrease
V_{thn}	increase	decrease	increase	mild decrease
V_{thp}	increase	decrease	increase	mild decrease
t_{oxn}	decrease	increase	decrease	increase
t_{oxp}	decrease	decrease	mild decrease	mild increase

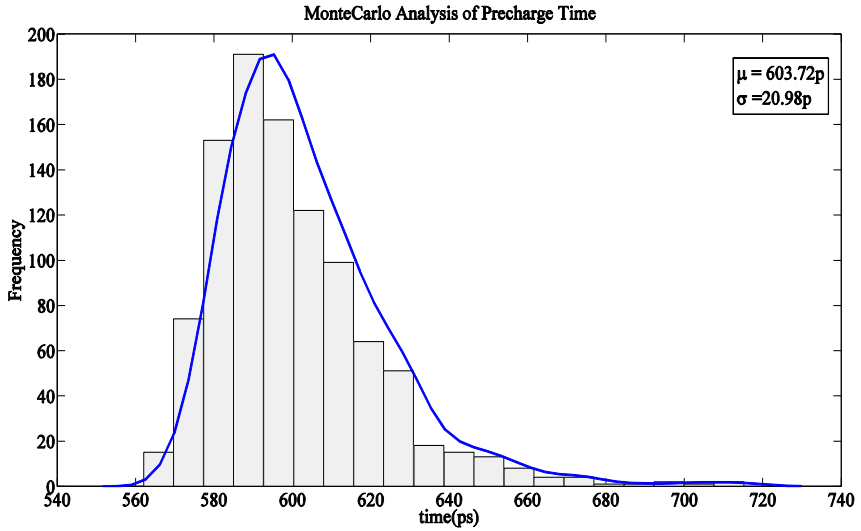


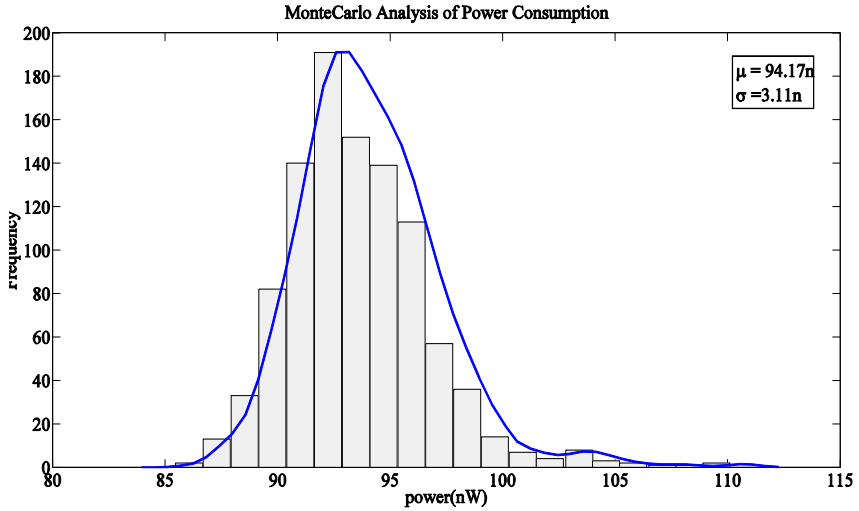
Dual Oxide Technology

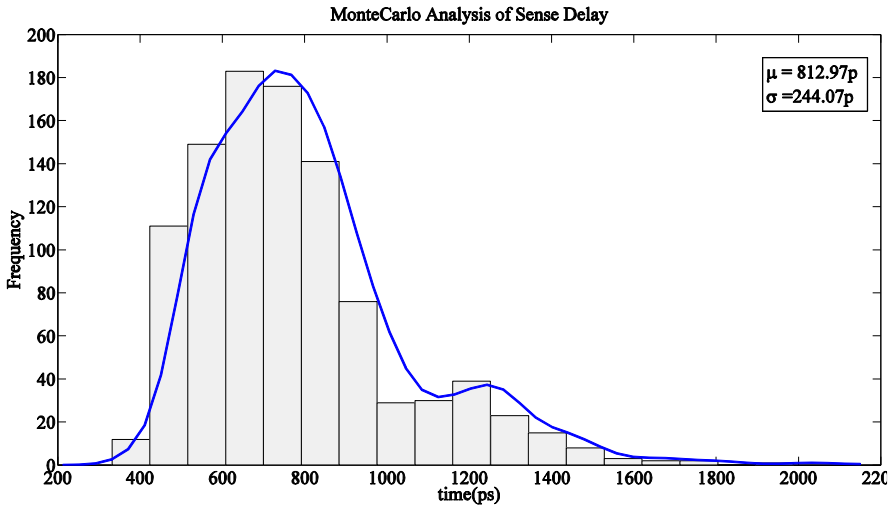
- A Monte Carlo analysis of the effects of process variation of design parameters on FoMs
  - Parameters were varied at +/- 10% of selected values from parametric analysis
- A Monte Carlo analysis of the FoMs reaction to variation of individual parameters
- Transistors are assigned different oxide thickness for optimizing design
  - $T_{ox,high}$ = 3nm
  - $T_{ox,low}$ = 2.4nm
- FoM's are analyzed with different oxide thickness

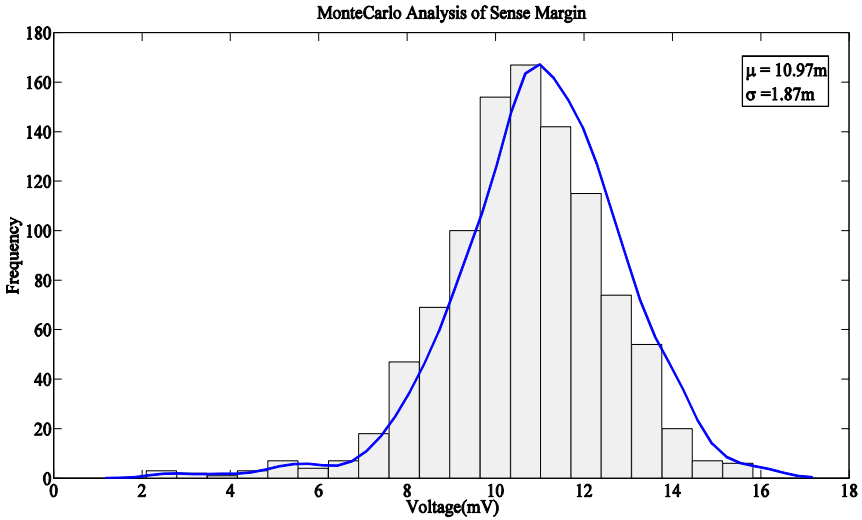


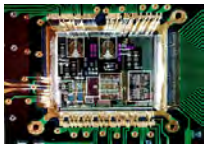
Monte Carlo Analysis:PDF of FoMs





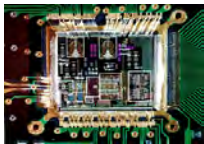




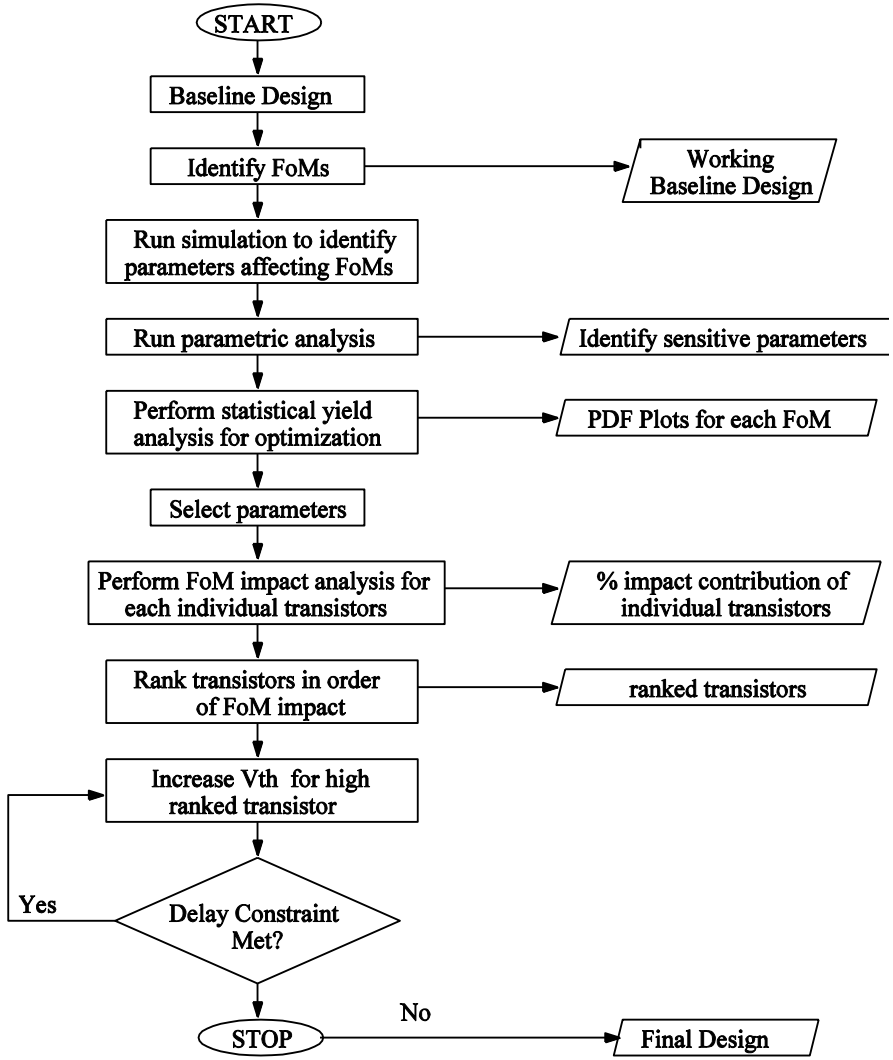


Probability Density Function of Different FoMs of the Sense Amplifier

Params	Precharge PDF		Power PDF		Sense Delay PDF		Sense Margin PDF	
	μ (ps)	σ(ps)	μ (nW)	σ(nW)	μ (μs)	σ(ps)	μ (mV)	σ(μV)
L_n	773.65	13.81	191.67	0.56	1.26	16.79	10.67	32.22
L_p	773.44	2.40	191.67	0.06	1.26	0.15	10.68	2.22
W_n	773.18	5.04	191.71	0.50	1.25	15.82	10.67	102.41
W_p	774.08	6.34	190.69	2.07	1.26	0.22	10.68	13.49
V_{DD}	772.72	123.68	190.85	27.25	1.30	0.36	10.21	2074.63
C_S	772.61	0.20	191.68	0.25	1.26	49.81	10.66	367.51
C_{BL}	773.48	14.76	191.73	6.38	1.26	3.76	10.69	591.49
t_{oxn}	774.15	11.68	191.32	1.47	1.26	25.48	10.62	311.87
t_{oxp}	773.74	2.05	192.06	1.93	1.26	0.10	10.68	65.80



Flow Diagram



Algorithm 1 Heuristic algorithm for sense amplifier optimization using Dual Oxide Based Technology

1: Create the netlist of the sense amplifier circuit.

2: Number each of the transistors in the netlist from 1 to N.

3: **for** Each of the transistors i = 1 to N **do**

4: Rank the transistors for a figure of merit. For example, contributions to precharge.

5: Identify the significant transistors from the ranks, e.g. 30% or 50%

6: **end for**

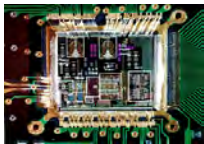
7: Start with the highest ranked transistor as i =0

8: **while** Design constraint of the sense amplifier is met and the transistor M_i is a significant transistor that contributes to the overall FoM value of the sense amplifier **do**

9: Increase thickness oxide of the the transistor M_i

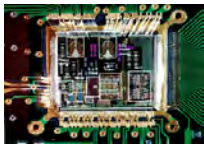
10: Move to the next ranked transistor

11: **end while**

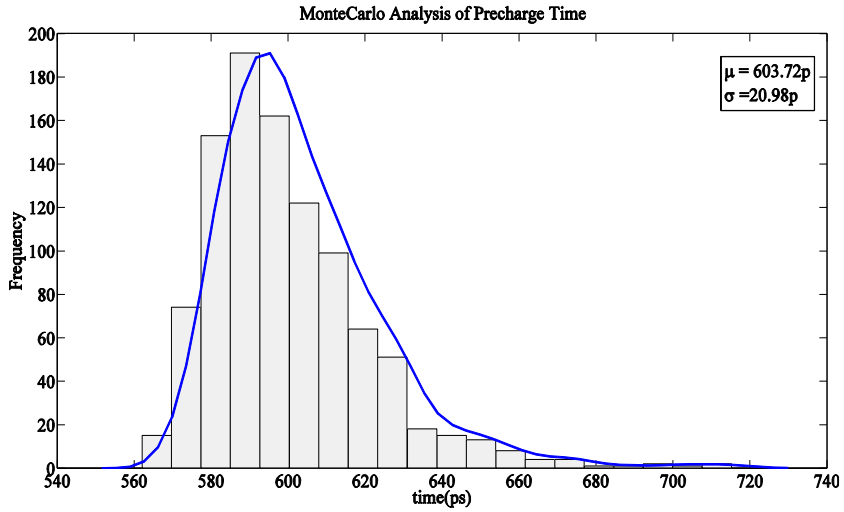


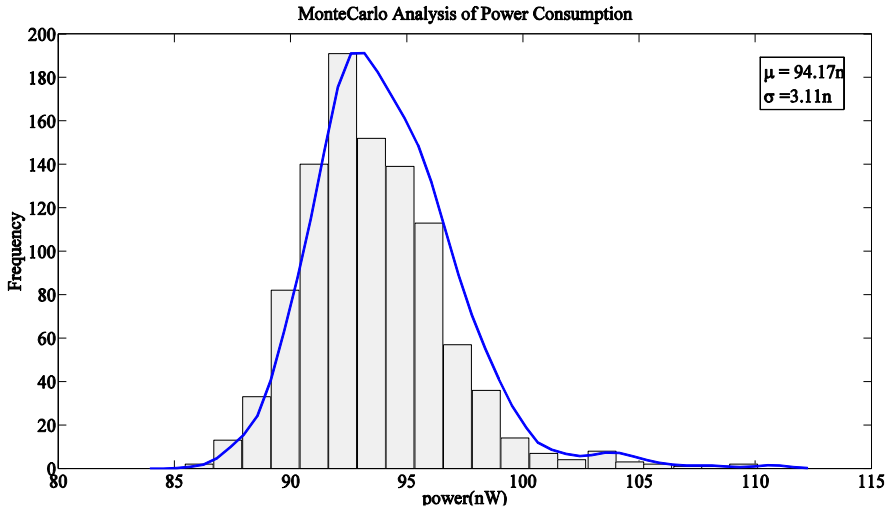
Dual Threshold Voltage Technology

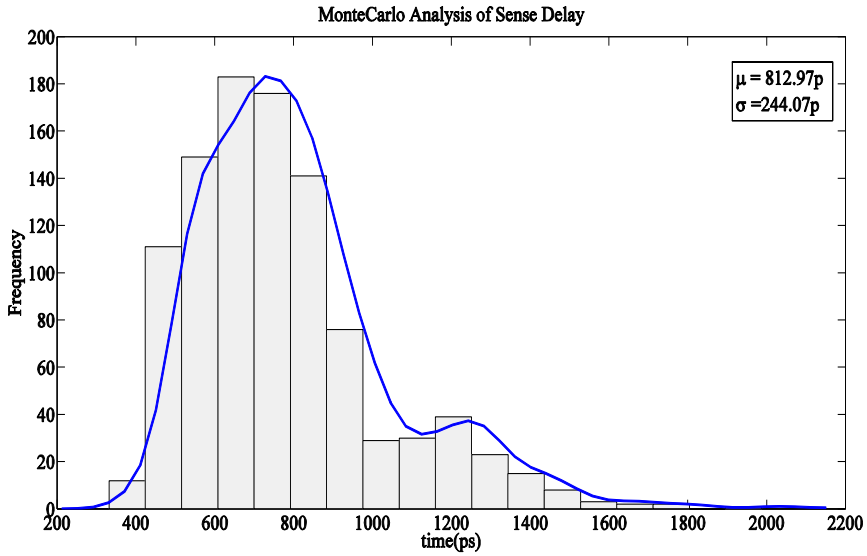
- A Monte Carlo analysis of the effects of process variation of design parameters on FoMs
  - Parameters were varied at +/- 10% of selected values from parametric analysis
- A Monte Carlo analysis of the FoMs reaction to variation of individual parameters
- Transistors are assigned different threshold voltages for optimizing design
  - $V_{th,high}$ = 0.36V
  - $V_{th,low}$ = 0.18V
- FoM's are analyzed with different threshold voltages

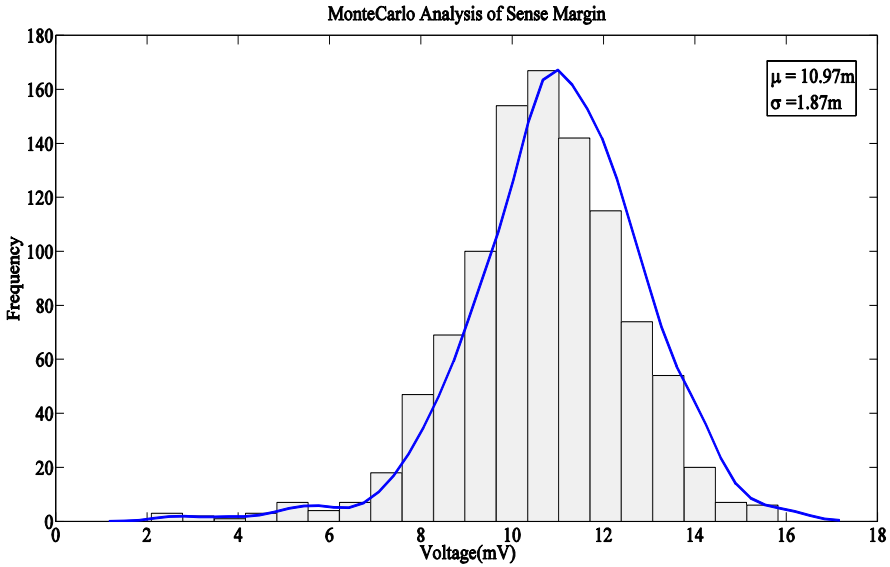


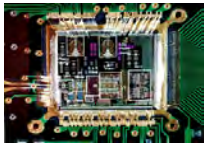
PDF of FoMs


MonteCarlo Analysis of Precharge Time
μ = 603.72p
σ =20.98p
Frequency
time(ps)


MonteCarlo Analysis of Power Consumption
μ = 94.17n
σ =3.11n
Frequency
power(nW)

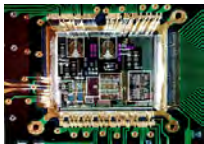

MonteCarlo Analysis of Sense Delay
μ = 812.97p
σ =244.07p
Frequency
time(ps)


MonteCarlo Analysis of Sense Margin
μ = 10.97m
σ =1.87m
Frequency
Voltage(mV)

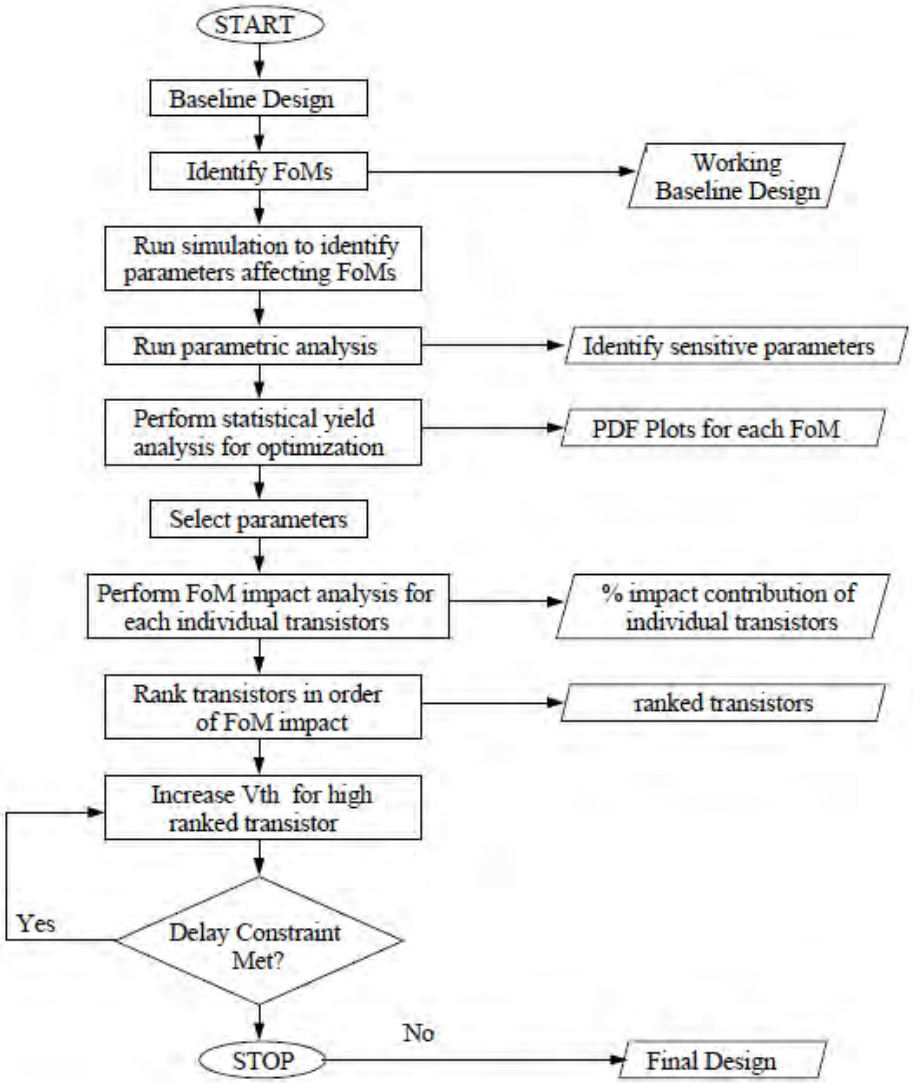


Probability Density Function of Different FoMs of the Sense Amplifier

Params	Precharge PDF		Power PDF		Sense Delay PDF		Sense Margin PDF	
	μ (ps)	σ(ps)	μ (nW)	σ(nW)	μ (μs)	σ(ps)	μ (mV)	σ(μV)
L_n	598.01	4.22	94.93	3.13	770.10	80.85	7.89	907.49
L_p	597.92	4.12	94.20	3.08	770.12	80.85	7.88	914.88
W_n	598.20	5.47	94.16	3.03	770.20	81.01	7.87	920.6
W_p	597.93	4.16	94.15	3.25	770.12	80.86	7.88	913.22
V_{DD}	602.37	17.83	94.59	16.88	803.06	211.95	6.93	3154.05
C_S	597.93	4.15	94.18	3.02	769.13	89.73	7.87	943.99
C_{BL}	597.82	6.16	94.11	4.11	770.41	81.40	7.91	999.44
V_{thn}	598.69	5.93	94.42	3.12	774.26	98.08	7.89	1007.7
t_{oxn}	598.19	5.09	94.36	3.53	773.61	90.90	7.82	1220.27
t_{oxp}	598.11	4.20	94.41	3.09	771.42	85.22	7.96	1003.42



Flow Diagram/Algorithm



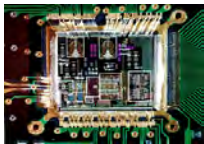
Algorithm 2 Heuristic algorithm for sense amplifier circuit optimization using Dual Threshold Based Technology

1: Create the netlist of the sense amplifier circuit.
2: Number each of the transistors in the netlist from 1 to N.
3: **for** Each of the transistors $i = 1$ to N **do**
4: Rank the transistors for a figure of merit. For example, contributions to precharge.
5: Identify the significant transistors from the ranks, e.g. 30% or 50%, etc
6: **end for**
7: Start with the highest ranked transistor as $i = 0$
8: **while** Design constraint of the sense amplifier is met and the transistor M_i is a significant transistor that contributes to the overall FoM value of the sense amplifier **do**
9: Increase threshold voltage of the transistor M_i.
10: Move to the next ranked transistor.
11: **end while**

Characterization of Optimized Design

- The FoM's are improved on the final design.

FoMs	Precharge	Power	Sense Delay	Sense Margin
Baseline	7.5 ns	153.1 μW	4.4 ns	43.4 mV
Dual-V_{th}-Optimal	1.2 ns	133.1 μW	0.87 ns	70.4 mV
Improvement	83.9%	13.1%	80.2%	61.9%



Conclusions

- The effects of process variation were analyzed through parametric and Monte Carlo analysis.
- A method of producing more tolerant and optimal designs was presented.
- FoM's were improved
  - Precharge by 83.9%
  - Sense delay by 80.2%
  - Sense margin by 61.9%
  - Power dissipation by 13.1%
- Analysis will be extended to different sense amplifier topologies.