Lecture 7: Components of Phase Locked Loop (PLL)

CSCE 6933/5933
Advanced Topics in VLSI Systems

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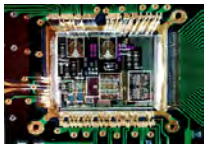
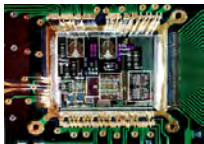


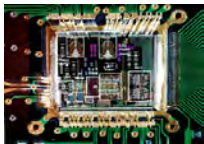
Lecture Outline

- Overall view of a Phase Locked Loop
- Components of a PLL
- High Level System Design
- Component - wise Design and Power Optimization
- Mixed-Signal System Analysis



Phase Locked Loop

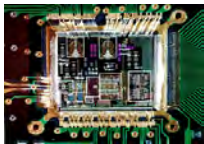
- The first phase locked loop was proposed by a French scientist de Bellescize in 1932.
- Basic idea of working: reduction of phase difference between a locally generated signal and a reference signal by using feedback.
- A Phase Locked Loop (PLL) circuit synchronizes to an input waveform within a selected frequency range, returning an output voltage proportional to variations in the input frequency.
- Used to generate stable output frequency signals from a fixed low-frequency signal.
- Two types: Analog and Digital
  - Analog PLLs are extensively used in communication systems as they maintain a linear relationship between the input and the output
  - Digital PLLs are suitable for synchronization of digital signals, clock recovery from encoded digital data streams and other digital applications



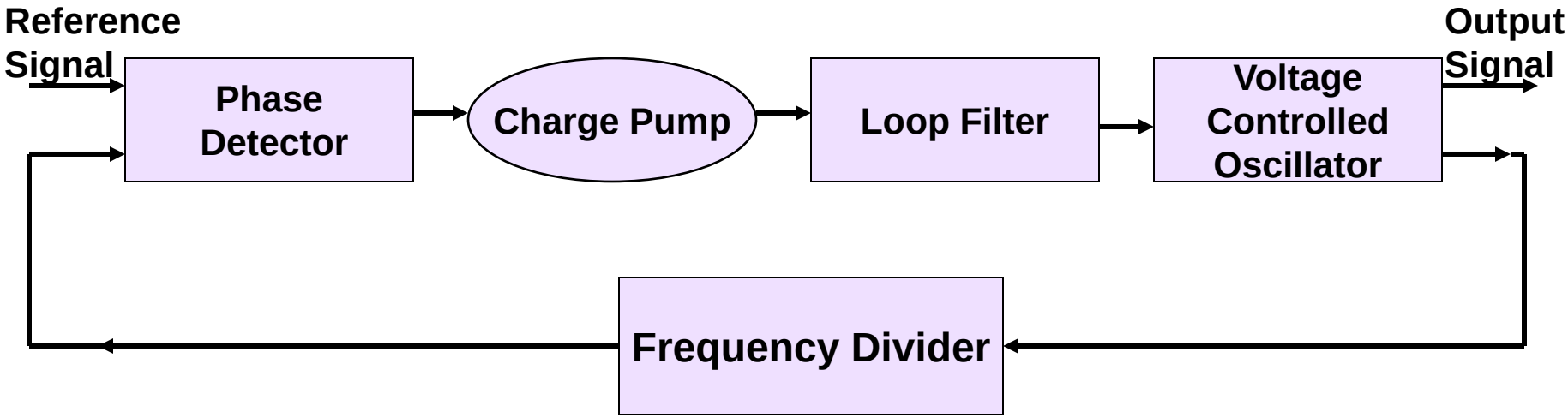
Phase Locked Loop (contd..)

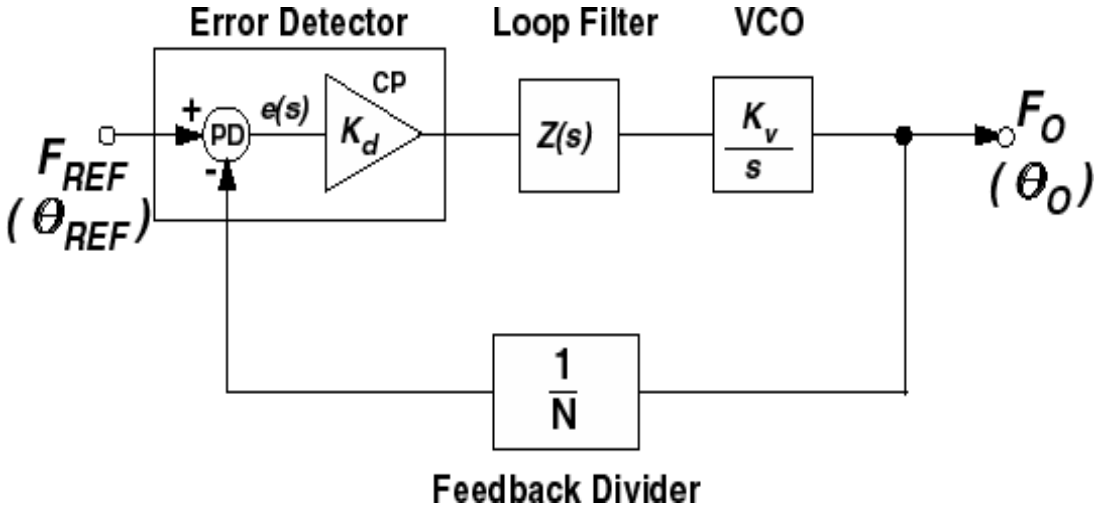
- Three fundamental purposes of a PLL
  - Demodulator: matched filter operating as a coherent detector.
  - Tracker of a carrier or synchronizing signal: narrow-band filter for removing noise from the signal and regenerating a clean replica of the signal.
  - Frequency synthesizer: oscillator is locked to a multiple of an accurate reference frequency.

- The components of a Phase Locked Loop are:
  - Phase Detector
  - Charge Pump
  - Loop Filter
  - Voltage Controlled Oscillator
  - Frequency Divider

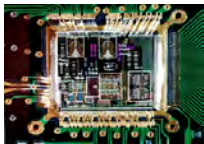


Phase Locked Loop (contd..)



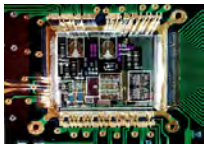


Phase detector and charge pump together form the error detector block



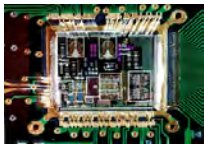
High Level System Design

- Behavioral-modeling languages like Verilog-AMS and Verilog-A are very important tools for a top-down design methodology for circuit designers.
- Provide validation of the overall system.
- Better performance at a higher speed.
- Verilog-A: C like behavioral description language for circuit designing.
- Non-ideal characteristic behavior description.



Voltage Controlled Oscillator

- Oscillators are used to create a periodic logic or analog signal with a stable and predictable frequency.
- Types of oscillators:
  - LC oscillators - oscillates by charging and discharging a capacitor through an inductor
  - Crystal oscillators
  - Ring oscillators
- VCO is an electronic oscillator specifically designed to be controlled in oscillation frequency by a voltage input.
- Current starved VCO is used.



High Level System Design of a Voltage Controlled Oscillator

- INSTANCE parameters
  - Amplitude of the output signal
  - Centre frequency of oscillation
  - Oscillator conversion gain
- VCO_{gain} = (f_i - f_c) / V_{in} ; where f_i= instantaneous frequency, f_c= centre frequency of oscillation, V_{in}= input voltage.

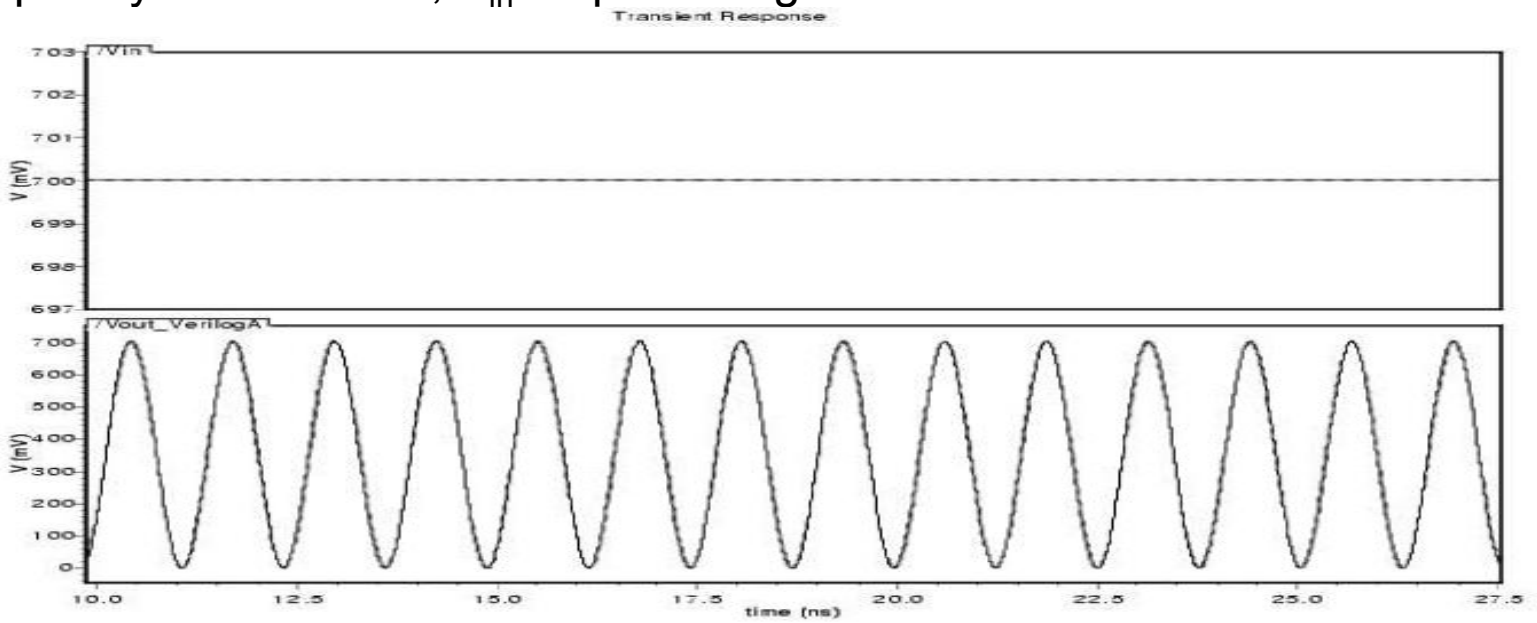
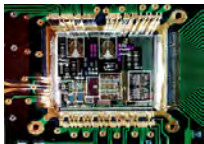


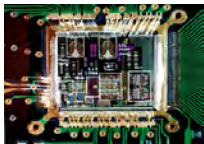
Figure: Simulation results of the Verilog-A code for Voltage Controlled Oscillator



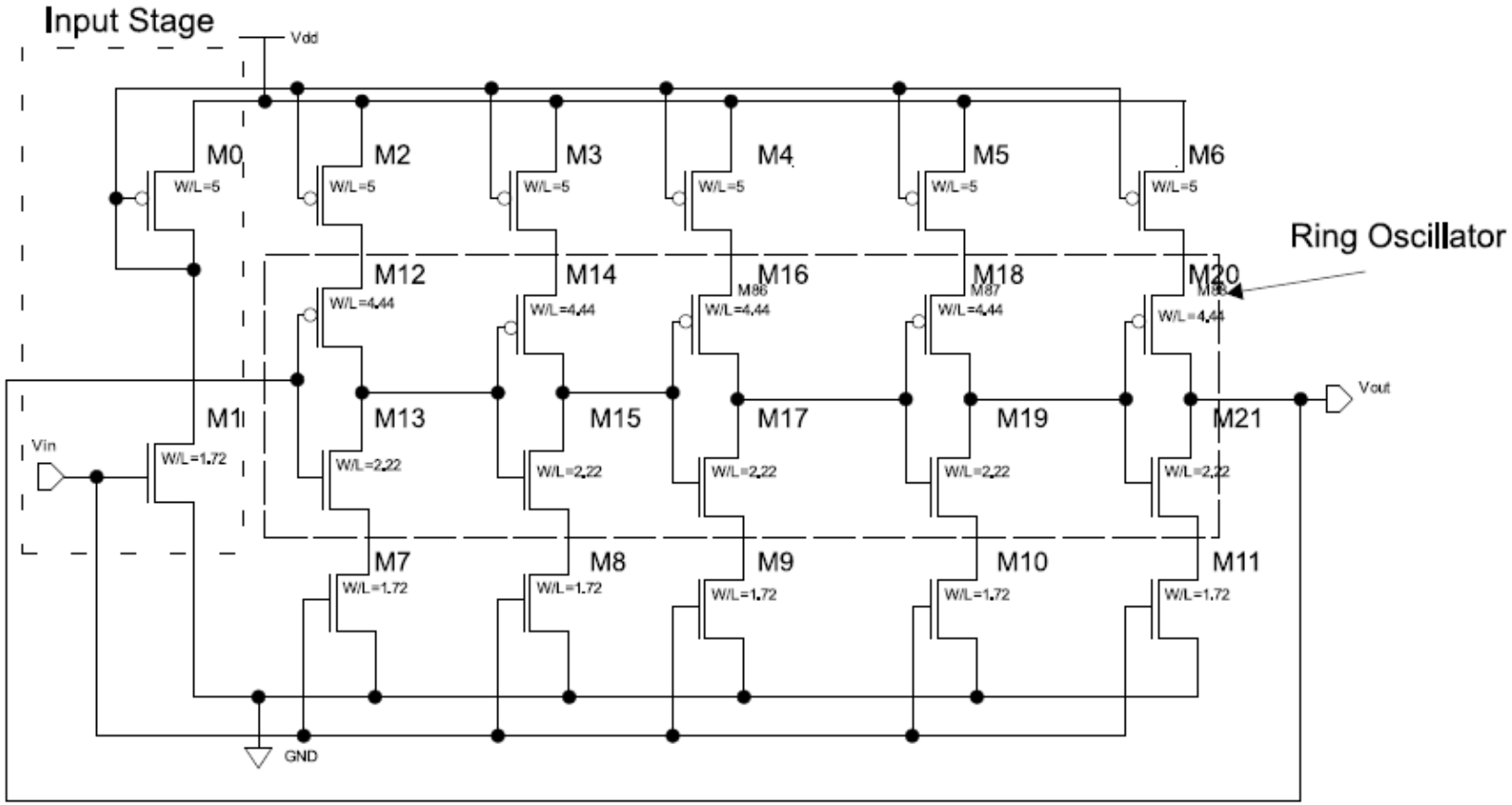
Current Starved Voltage Controlled Oscillator

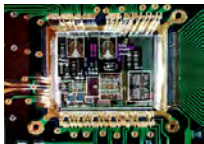
- Current Starved VCO comprises of
  - Odd numbered chain of inverters
  - Two input stage transistors => limit current flow to the inverter

- Frequency of oscillation (f_o) depends on
  - Number of inverters (N)
  - Size of the transistor (W/L)
  - Current flowing through the inverter (I_{inv}) which is dependent on the input voltage (V_{dd})
  - So, $f_o = I_{inv} / (N*C_{TOT}*V_{dd})$; where C_{TOT} is the total capacitance of the inverter transistors



Transistor Level Diagram of a VCO





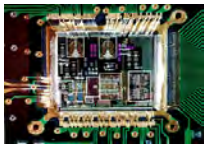
VCO Equations

Frequency of Oscillation $$f_o = \frac{1}{N(T_{TOT})} = \frac{I_{inv}}{(N * C_{TOT} * V_{dd})}$$

where $$T_{TOT} = \frac{(C_{TOT} * V_{dd})}{I_{inv}}$$

and $$C_{TOT} = C_O + C_I = \hat{C}_{ox}(W_p L_p + W_n L_n) + \frac{3}{2}\hat{C}_{ox}(W_p L_p + W_n L_n),$$

$$C_{TOT} = \frac{5}{2}\hat{C}_{ox}(W_p L_p + W_n L_n)$$



Analog Design and Simulation Results of the VCO

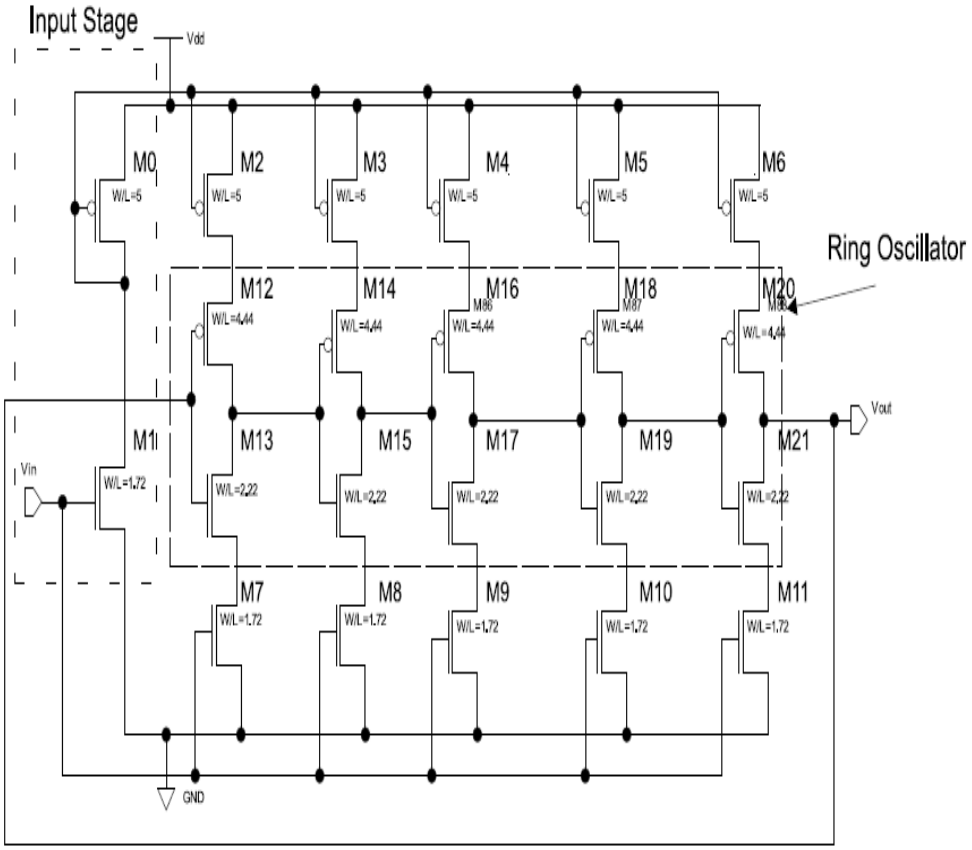


Fig: Transistor level circuit diagram of the VCO

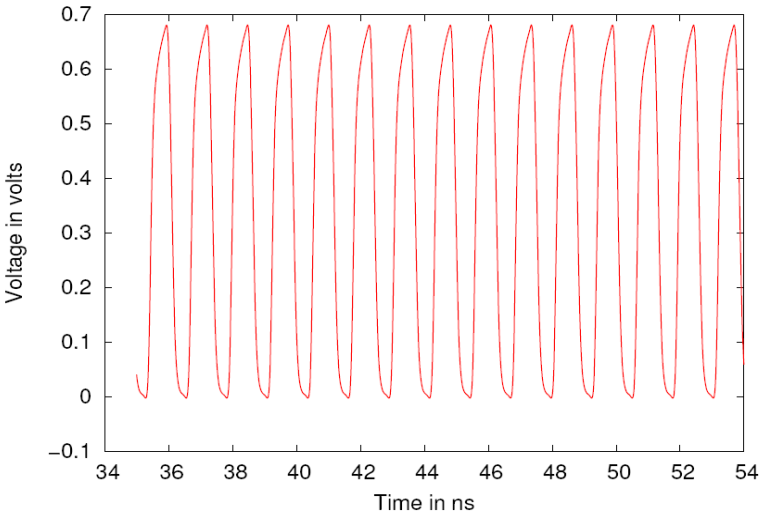


Fig: Simulation waveform of the analog VCO

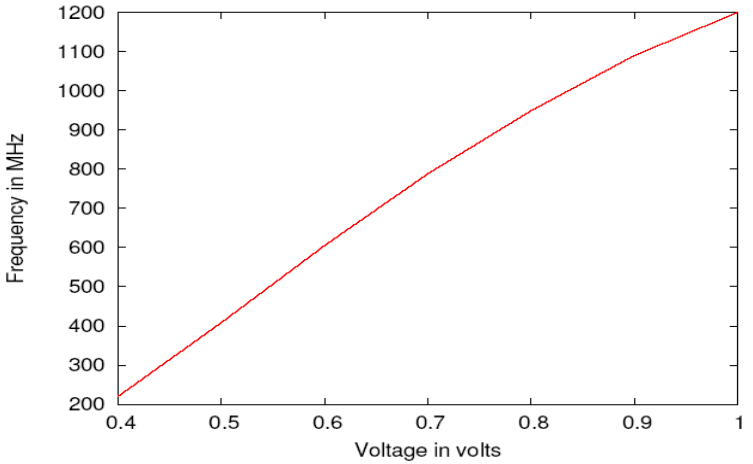


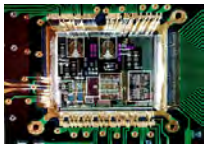
Fig: Voltage versus Frequency response

Experimental Results: Power Analysis on VCO

- Average power and Leakage power are calculated
- Calculator option in Cadence Spectre was used

Transistor type	Transistors	Average Power in μW	Leakage Power in nW	Percentage
Input	PMOS (M0)	12.26	0.0331	0.00027
	NMOS (M5)	4.69	4.82	0.103
Current Starved	PMOS (M75, M76, M77, M78, M79)	0.215	0.345	0.159
	NMOS (M80, M81, M82, M83, M84)	0.255	30.41	0.0193
Inverter	PMOS (M4, M85, M86, M87, M88)	0.912	207.07	0.715
	NMOS (M92, M91, M90, M89, M62)	0.832	95.87	0.539
Total		28.02	338.54	9.36

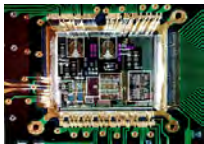
Table: Gate leakage and dynamic current for individual transistors in the VCO for an input voltage of 0.7V



Design of Experiments

- Full factorial method
  - Change in output studied with change in input
  - Two values for each input; one is considered as '+1' and the other as '–1'
  - Taguchi L8 design matrix
  - Eight different combinations => eight experiments
  - Output responses are tabulated
  - Average values of output responses and then Δ (effect) values are calculated and then the average value over each column of '+' and '-' is computed
  - Pareto diagrams: factors affecting the output response is known
  - Prediction equations corresponding to that particular output response is written using:

$$\hat{y} = \bar{\bar{y}} + \frac{\Delta_A}{2} * A + \frac{\Delta_B}{2} * B + \frac{\Delta_{AB}}{2} * AB$$

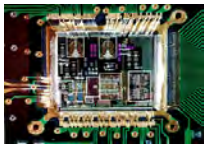


Design of Experiments: Results

- Inputs:
  - Gate oxide thickness
  - W/L ratios for current starved NMOS, current starved PMOS, input NMOS, and input PMOS
- Outputs:
  - Frequency of operation
  - Average power
  - Leakage power

Table: DOE, Experimental results

Run	T_{ox}	$\beta_1 = (\frac{W}{L})$ for PMOS CS	$\beta_2 = (\frac{W}{L})$ for NMOS CS	$\beta_3 = (\frac{W}{L})$ for PMOS Input	$\beta_4 = (\frac{W}{L})$ for NMOS Input	Frequency f_{osc} (MHz)	Correlation Coefficient R (%)	Average Power P_{av} (μW)	Leakage Power P_{leak} (pW)
1	1.4	5	1.72	10	3.44	787.91	99.21	46	342.66
2	1.4	5	3.44	5	1.72	925.04	99.28	29.64	408.83
3	1.4	10	1.72	10	1.72	813.78	99.06	32.05	370.58
4	1.4	10	3.44	5	3.44	992.46	98.91	38.29	497.63
5	1.7	5	1.72	5	3.44	630.65	99.85	32.90	310.35
6	1.7	5	3.44	10	1.72	692.12	99.82	29.57	326.29
7	1.7	10	1.72	5	1.72	672.32	99.77	26.25	337.14
8	1.7	10	3.44	10	3.44	777.18	99.81	45.66	417.31



Design of Experiments: Pareto Diagrams

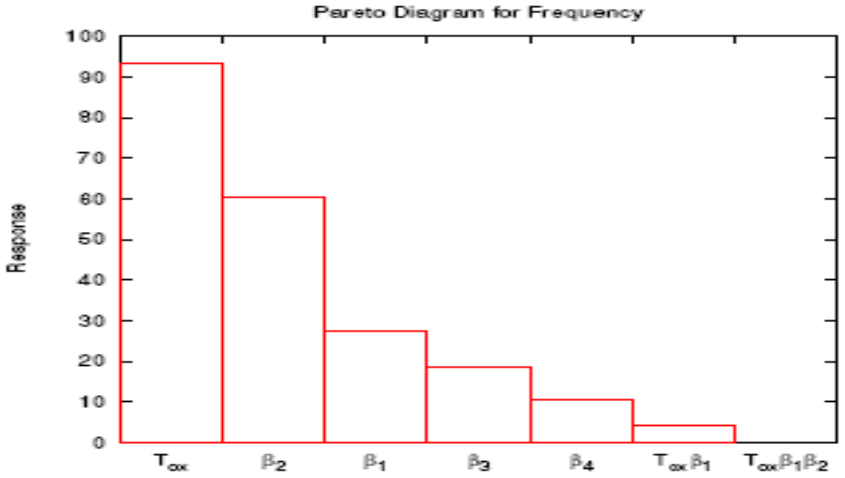


Fig: Pareto diagram for frequency

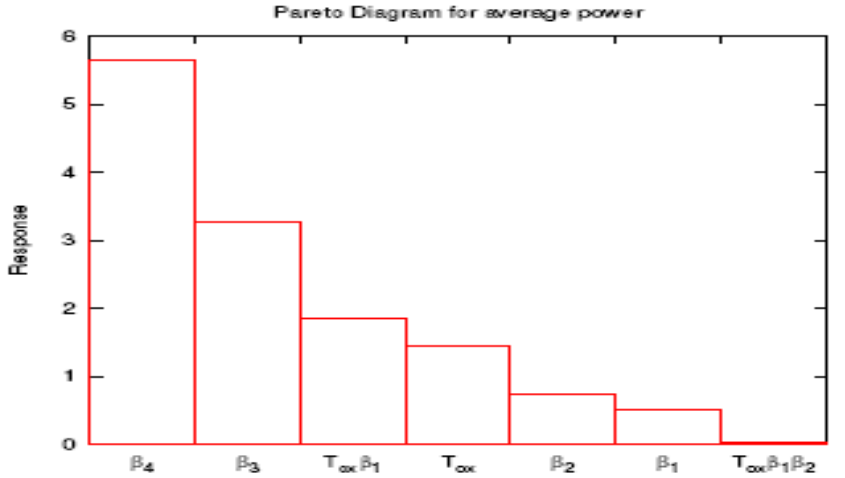


Fig: Pareto diagram for average power

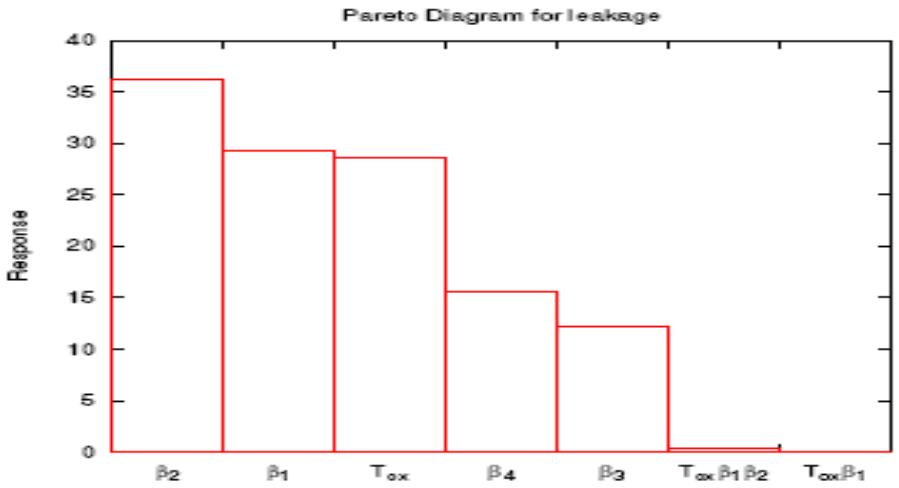


Fig: Pareto diagram for leakage power

- **T_{ox} - Gate oxide thickness**
- **β_1 - W/L ratio for** the PMOS inverter transistors
- **β_2** – W/L ratio for the NMOS inverter transistors.
- **β_3 –** W/L ratio for the PMOS current starved transistors.
- **β_4 –** W/L ratio for the NMOS current starved transistors.

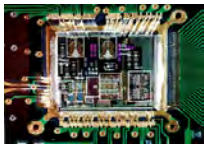
Design of Experiments: Prediction Equations and Optimization

- Prediction equations for the outputs considered:
  - $F\hat{} = 786.43 - 93.36T_{ox} + 60.3\ \beta_2$
  - $P\hat{} = 35.05 + 5.7\ \beta_4 + 3.3\ \beta_3$
  - $P_L\hat{} = 376.35 - 28.58\ T_{ox} + 29.32\ \beta_1 + 36.17\ \beta_2$

- Optimization of frequency of operation:
  - To maximize the frequency of oscillation, T_{ox} must be -1 while β_2 must be +1

- Optimization of average power:
  - β_4 and β_3 must be -1, as average power has to be minimized

- Optimization of leakage power:
  - T_{ox} and β_1 must be -1 and β_2 must be +1



Frequency Divider

- In any flip-flop, when a continuous train of pulse waveforms at fixed frequency is fed to it as an input signal, an output signal of approximately half the frequency of the input signal can be obtained
- Design and Working
  - JK flip-flop: realized using two 3-input and two 2-input NAND gates
  - Principle: count two pulses and then reset

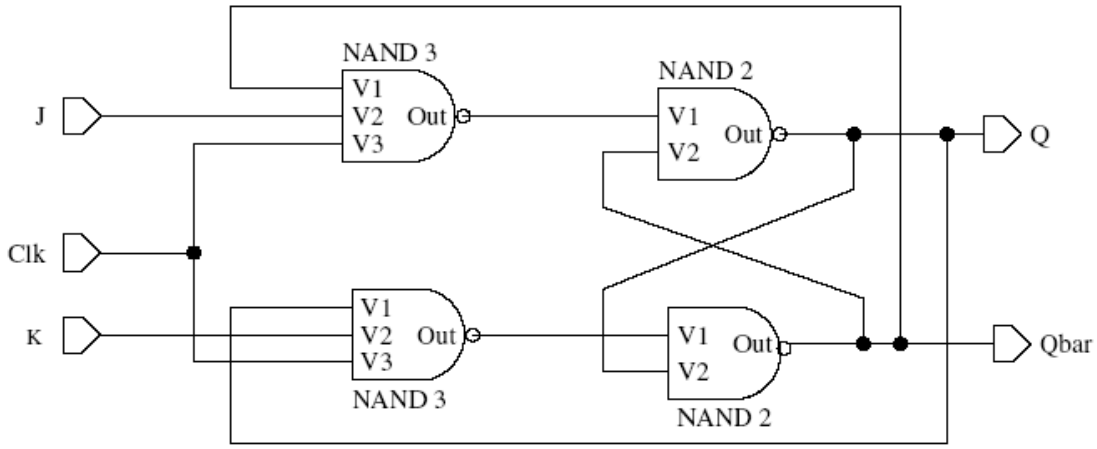
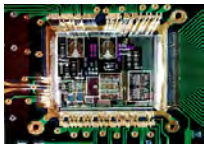


Fig: Circuit diagram of a J-K flip-flop



Analog Design and Simulation Results of a Frequency Divider

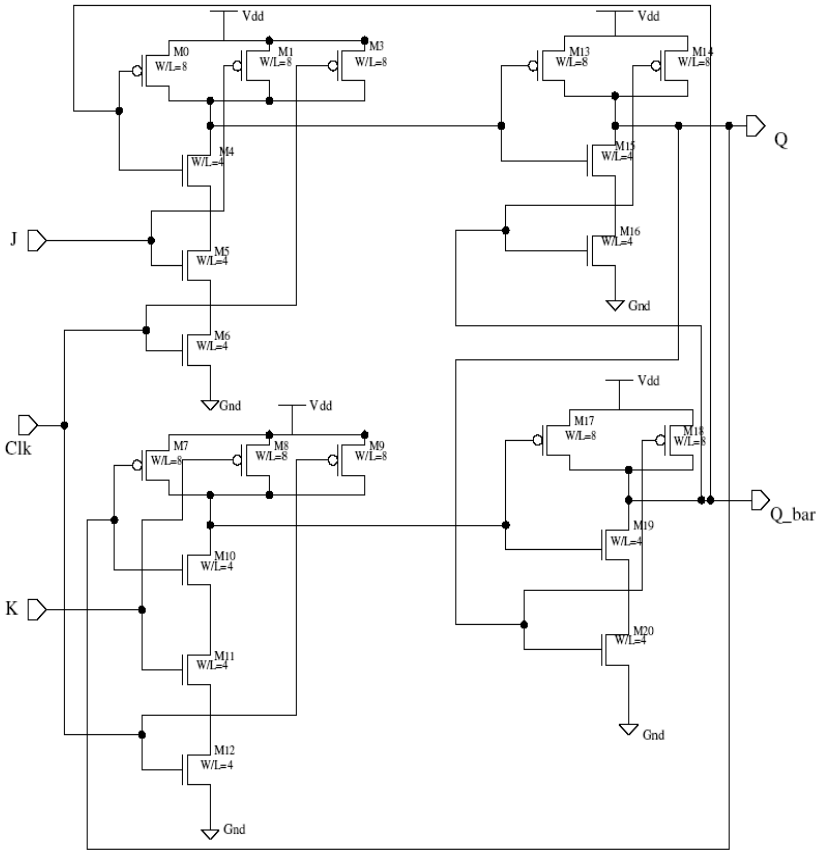


Fig: Transistor level circuit diagram of a frequency divider

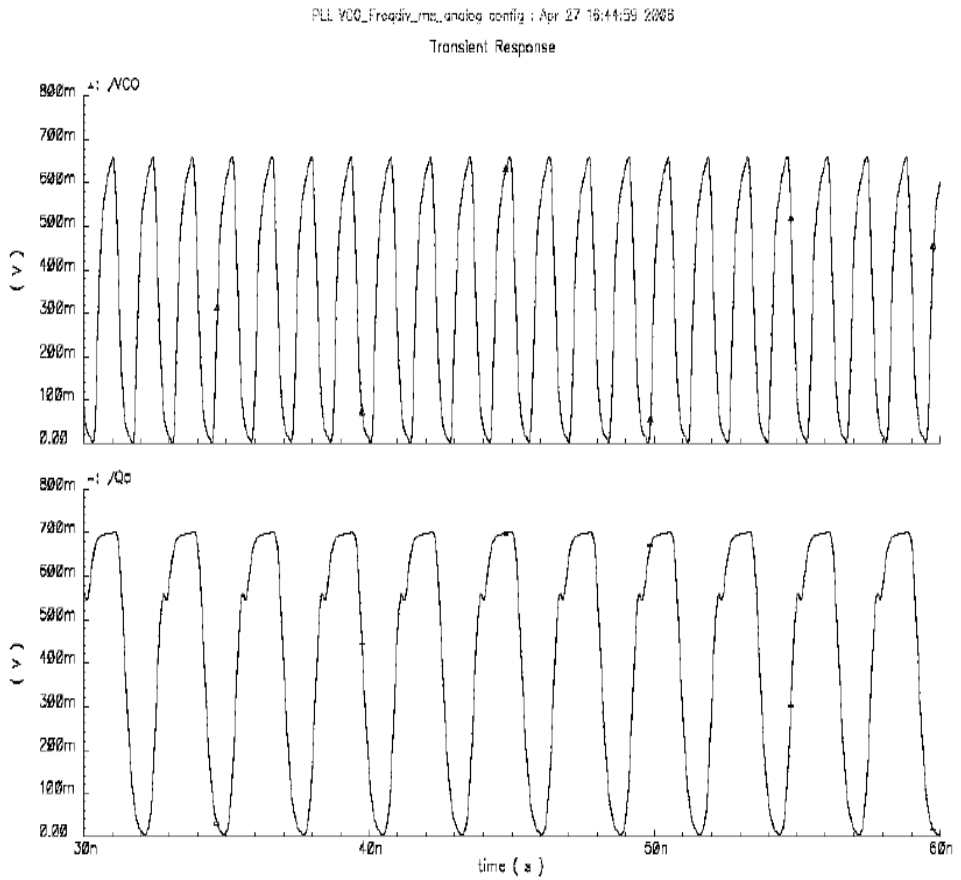
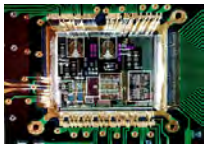
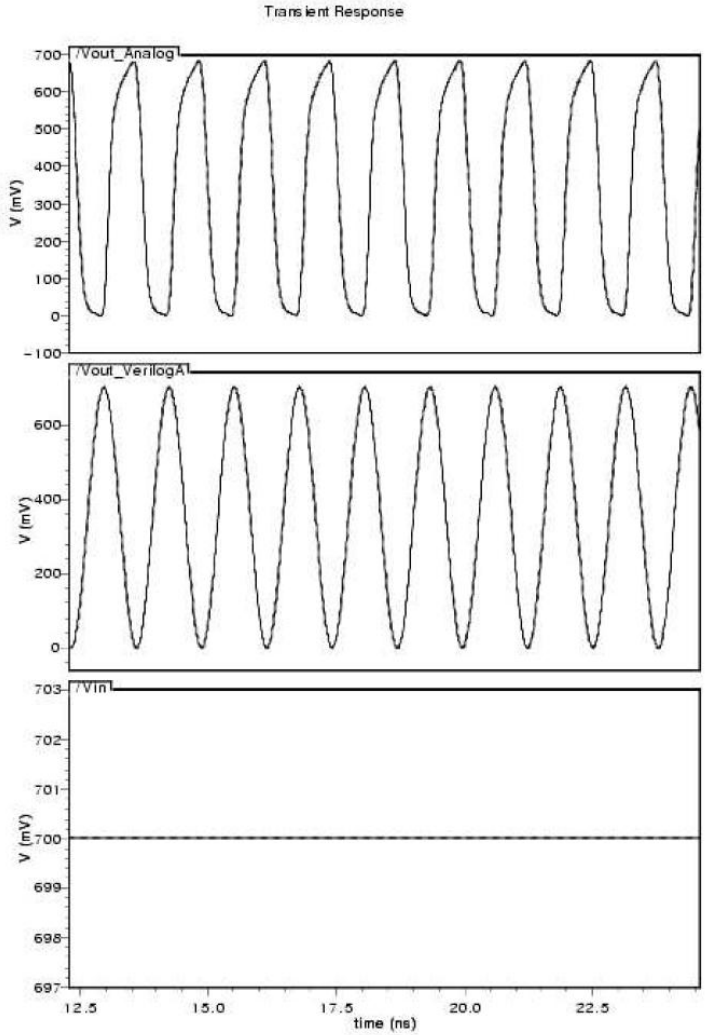
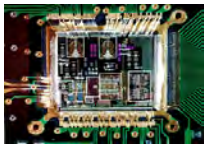


Fig: Simulation results of the VCO and frequency divider for an input voltage of 0.7V



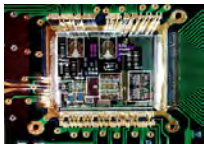
Comparative Simulation Results of Analog VCO with Verilog-A modeled VCO





Phase Frequency Detector

- Compares the phase of the local oscillator to that of the reference signal.
- Directs the charge pump to supply charge amounts in proportion to the phase error detected.
- Detects the phase or frequency differences and produces the resultant error voltage (output is proportional to the difference in phase or frequency).
- Types of phase detectors:
  - XOR gate
  - Four-quadrant multiplier, also known as a mixer
  - Bang-bang charge pump phase detector
  - Proportional phase detector
- A PFD is realized using two D flip-flops and one 2-input NAND gate.



High Level System Design of a Phase Frequency Detector

- INSTANCE parameters
  - output voltage for high
  - output voltage for low
  - V_{trans} = voltages above this voltage at input are considered high
  - Rise time, Fall time, and Delay time
- Reference signal is “behind” the input signal => Inc_out is low & Dec_out is high and vice versa.

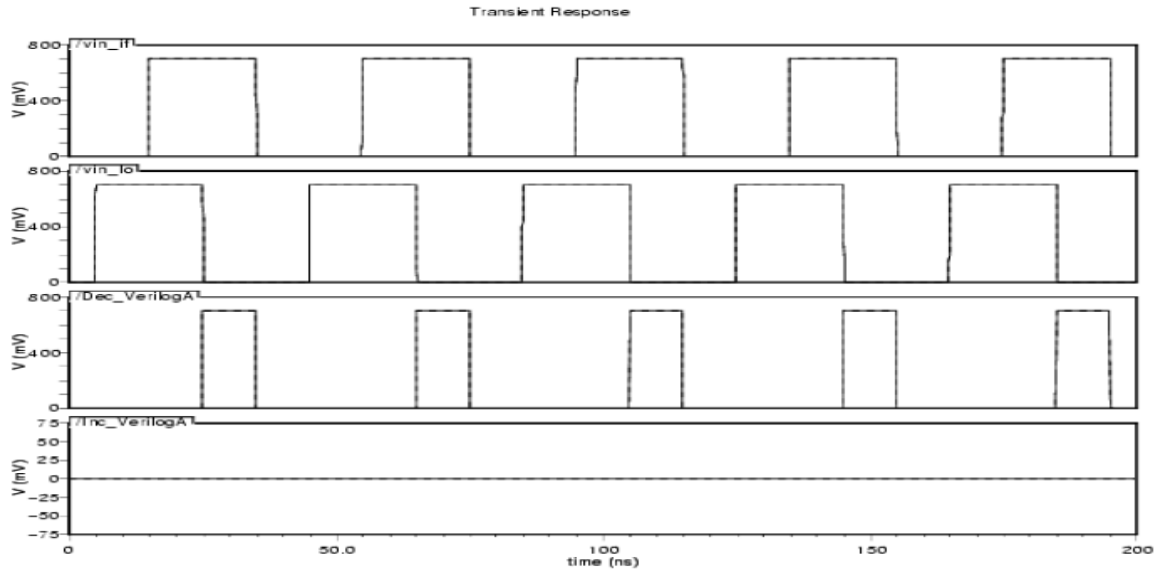
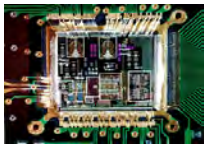


Figure: Simulation results of the Verilog-A code for Phase Frequency Detector



Simulation Results of the Analog Design for a Phase Frequency Detector

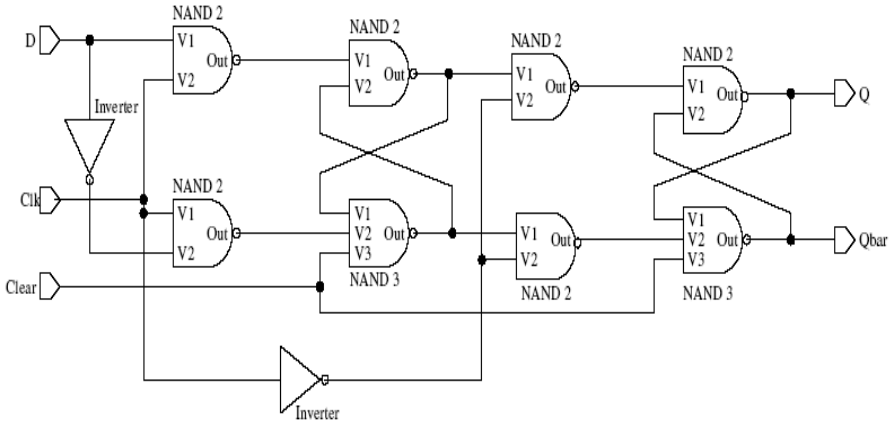


Fig: Circuit diagram of a D flip-flop

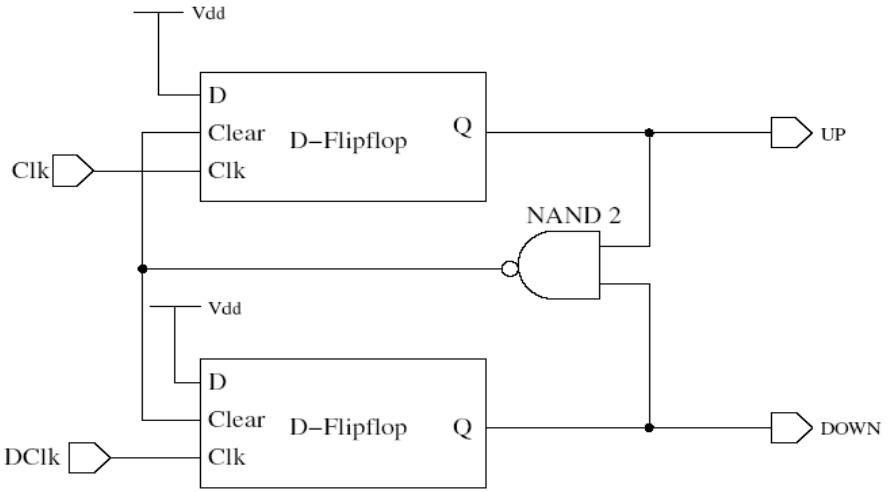
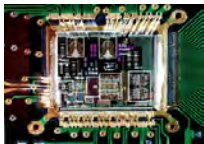


Fig: Circuit diagram of a PFD



Simulation Results of the Analog Design for a Phase Frequency Detector

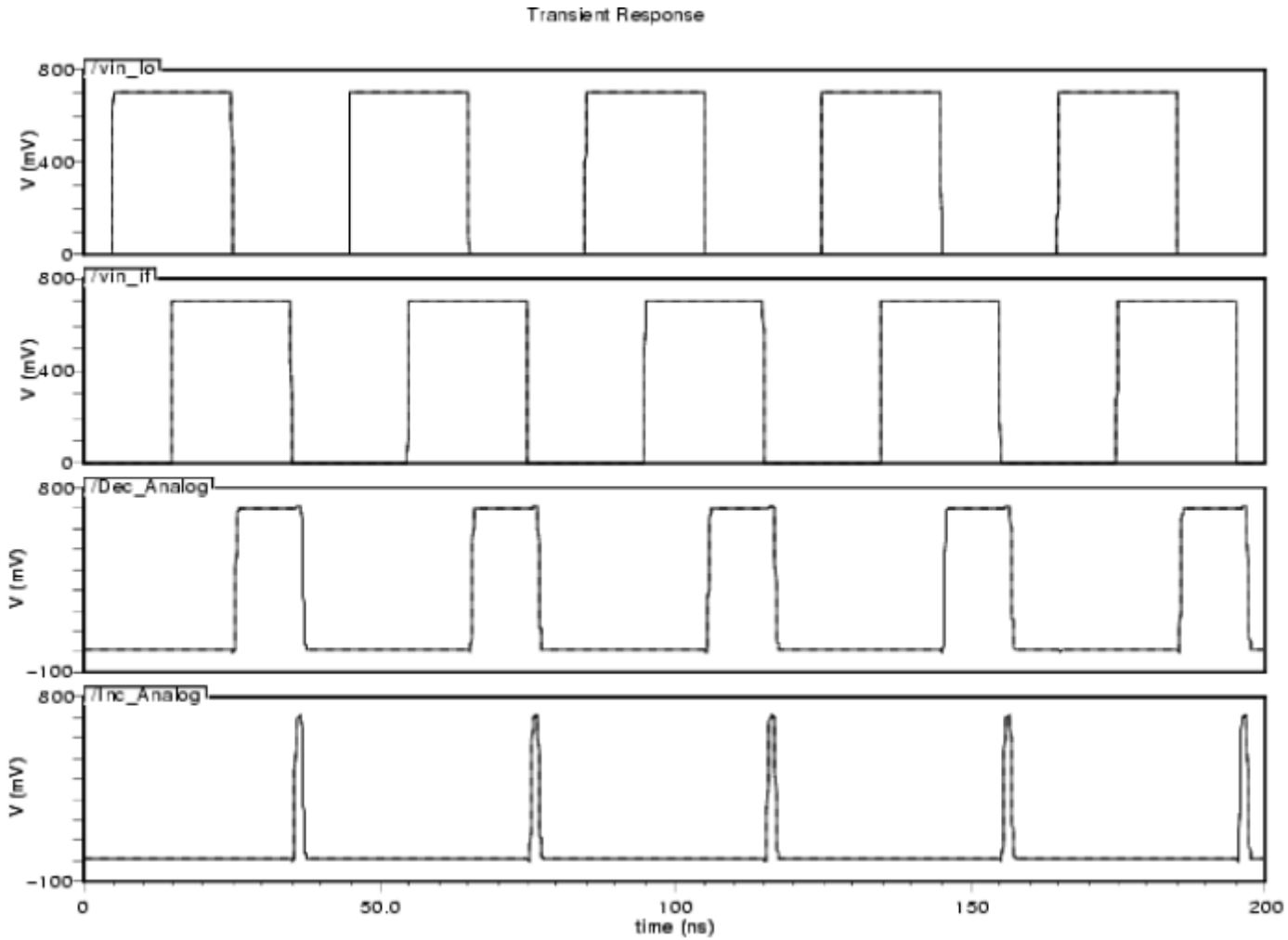
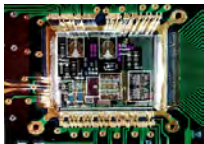


Fig: Simulation results of the PFD



Comparative Simulation Results of Analog PFD with Verilog-A modeled PFD

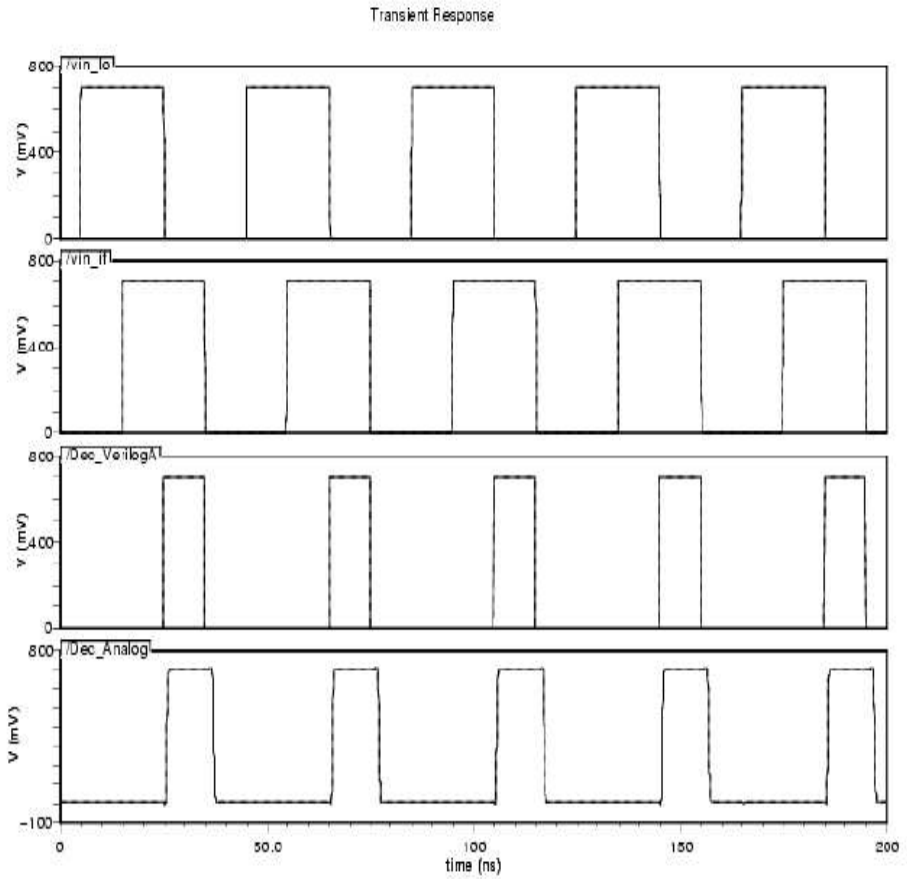


Fig: Comparative view of the simulation results of the Dec_out signal for a PFD for the analog and Verilog-A system design approaches.

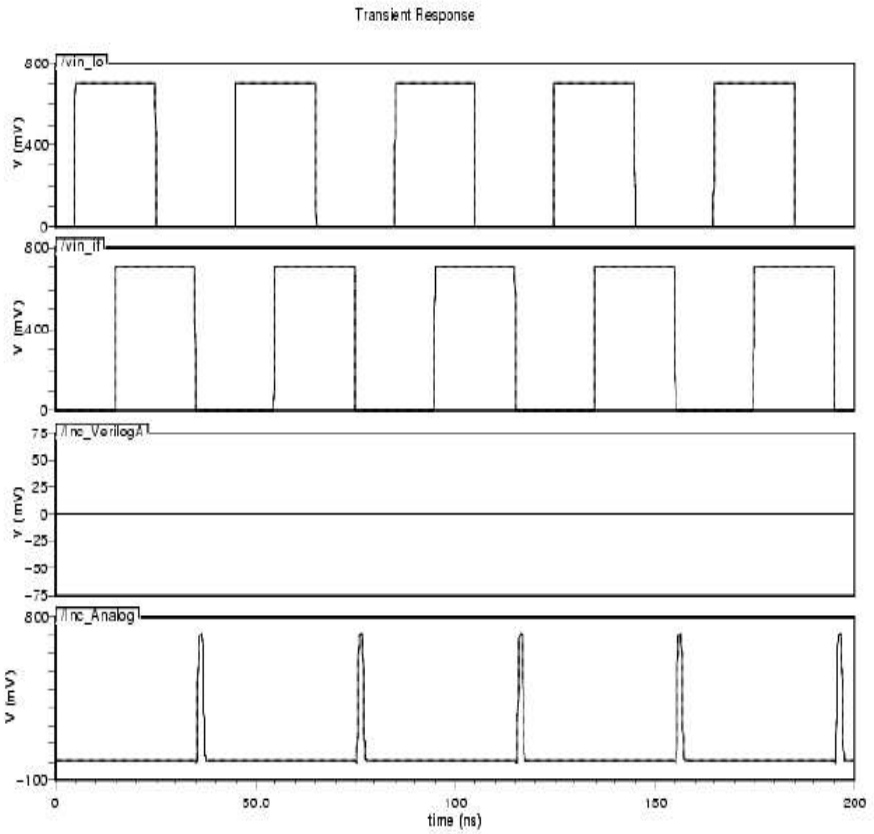
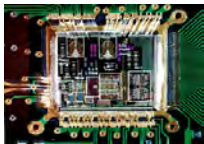
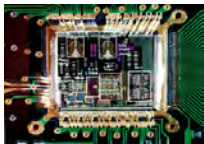


Fig: Comparative view of the simulation results of the Inc_out signal for a PFD for the analog and Verilog-A system design approaches.



Charge Pump

- Stabilizes spurious fluctuation of currents and switching time, to minimize the spurs in the VCO input.
- Manipulates the amount of charge on the filter's capacitors depending upon the signals from the UP and DOWN outputs of the PFD.
- Principle: two current sources and two switches controlled by the PFD outputs.
- UP is High & DOWN is Low => V_{out} increases => sources current on to the capacitor.
- UP is Low & DOWN is High =>V_{out} decreases => sinks current on the capacitor.
- UP is Low & DOWN is Low => V_{out} is constant and I_{out} is zero.
- Power analysis proves that the designed charge pump acts as a power source.



Analog Design and Simulation Results of the Charge Pump

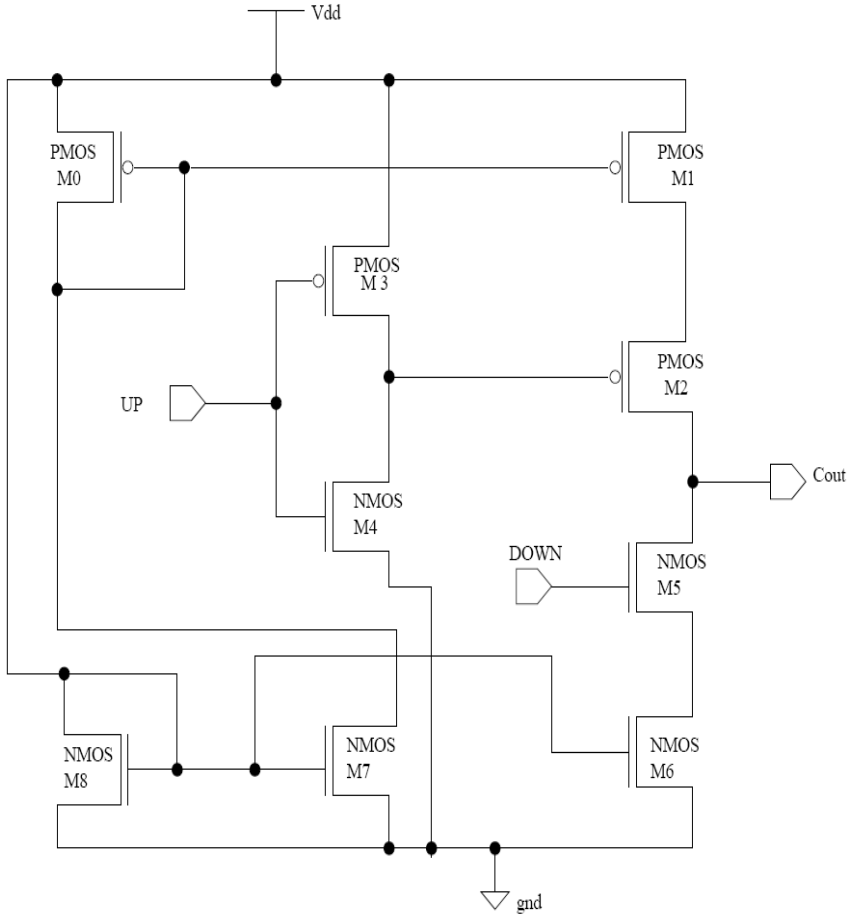


Fig: Transistor level circuit diagram of the charge pump

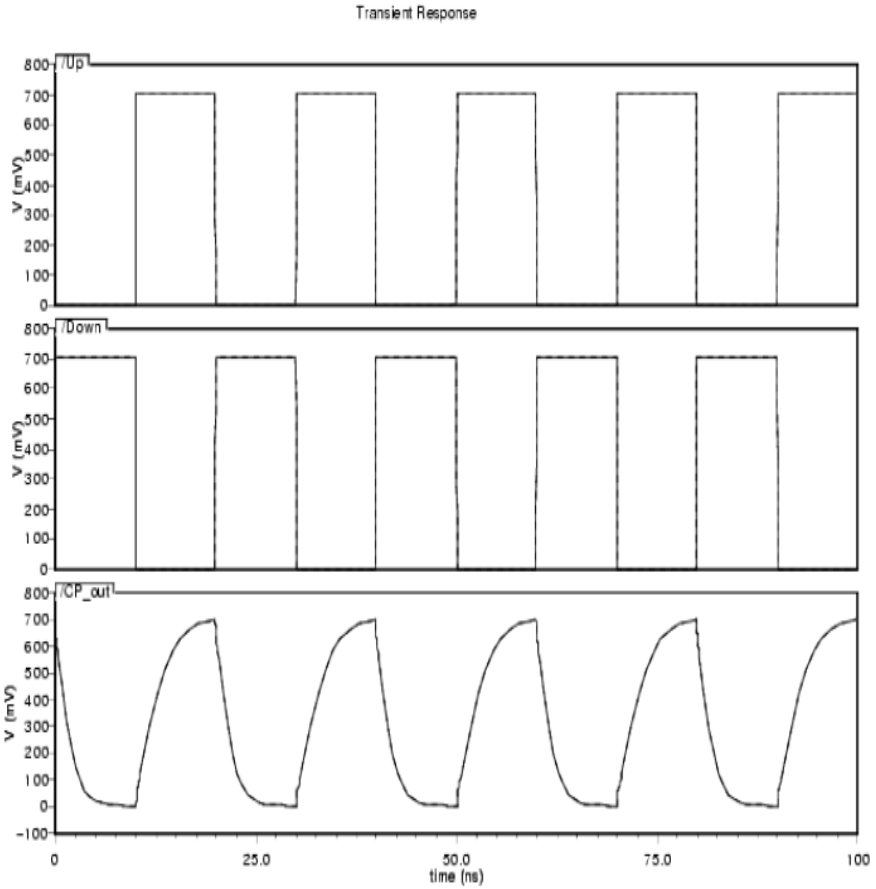
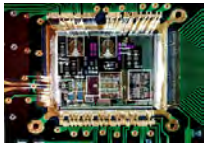


Fig: Simulation results of the charge pump at an input voltage of 0.7V

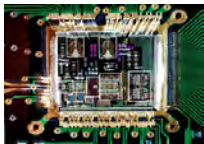


Power Analysis on a Charge Pump

- Average power and gate leakage power are calculated
- Gate leakage is a major component of leakage
- Scaling in gate oxide thickness results in an alarming increase in gate leakage current due to tunneling through the thin gate oxide.
- Average power calculated for the whole device = 104.732 μW

Table: Power analysis on a 45 nm charge pump

Transistor	Type	Total Avg Power in μW	Gate Leakage Power in nW
M0	PMOS	26.98	0.0562
M1	PMOS	1.55	0.1052
M2	PMOS	2.56	6.91
M3	PMOS	0.0919	8.35
M4	NMOS	0.0926	10.97
M5	NMOS	0.842	7.89
M6	NMOS	0.704	14.67
M7	NMOS	7.66	12.18
M8	NMOS	64.24	9.17
	Total	104.72	70.301

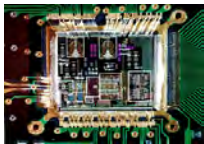


Transistor Wise Power Analysis According to Region of Operation on a Charge Pump

- Regions of operation
  - Triode
  - Saturation
  - Sub-threshold
- Sub-threshold leakage power is a vital component in the total power consumption as scaling of device dimensions and threshold voltage results in increased sub-threshold leakage
- Sub-threshold power was negligible when compared to the total power
- Total power consumed (transistor wise calculations) is 91.74 µW

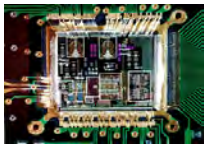
Table: Power Analysis for transistor M0 according to each region of operation in a charge pump

Region for M0	Drain to Source Voltage V_{ds} (V)	Drain to Source Current I_{ds} (A)	Gate to Source Voltage V_{gs} (V)	Gate Current I_g (A)	Gate Leakage Power P_g (W)	Drain to Source Power P_{ds} (W)
Triode	0.022	8.089μ	0.7	$20.96n$	$14.67n$	0.178μ
Saturation	0	0	0	0	0	0
Subthreshold	0	0	0	0	0	0
Total					$14.67n$	0.178μ
Total						0.192μ



Low Pass Filter

- Low pass RC filter passes frequency signals within the range of the VCO
- Principle: Cutoff frequency of the filter is approximately equal to the maximum frequency of the VCO => the filter will reject signals at frequencies above the maximum frequency of the VCO
- RC filter acts as a AC voltage divider circuit that discriminates against high frequencies, as the capacitive reactance decreases with frequency
- Low-pass filter smoothes out the abrupt control inputs from the charge pump



High Level System Design of a Low Pass Filter

- INSTANCE parameters
  - bandwidth of the filter
- f_{cutoff} = 1/ (2π*R*C); where R=1K and f_{cutoff}=788MHz

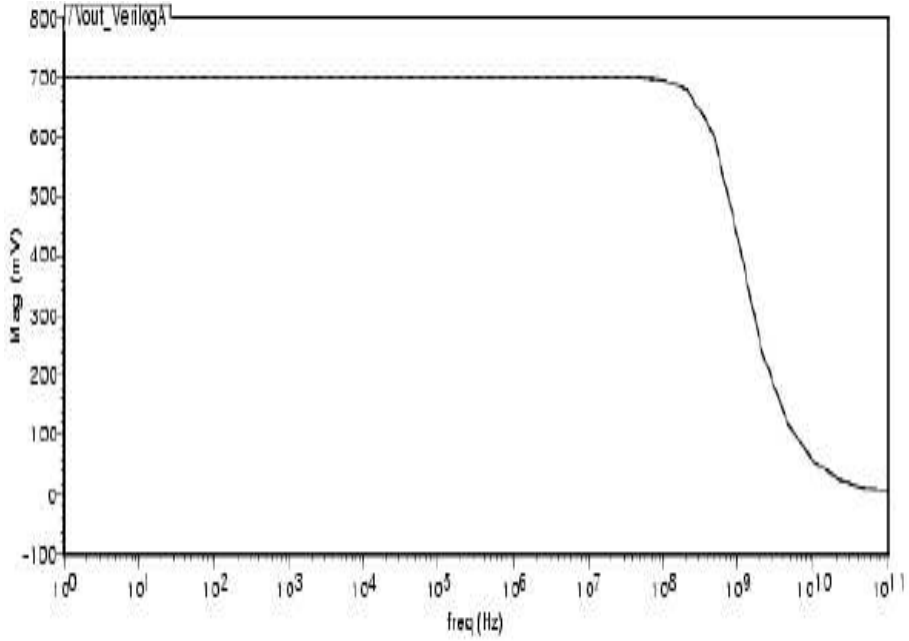


Figure: Simulation results of the Verilog-A code for **a low pass filter for an input voltage of 0.7V**

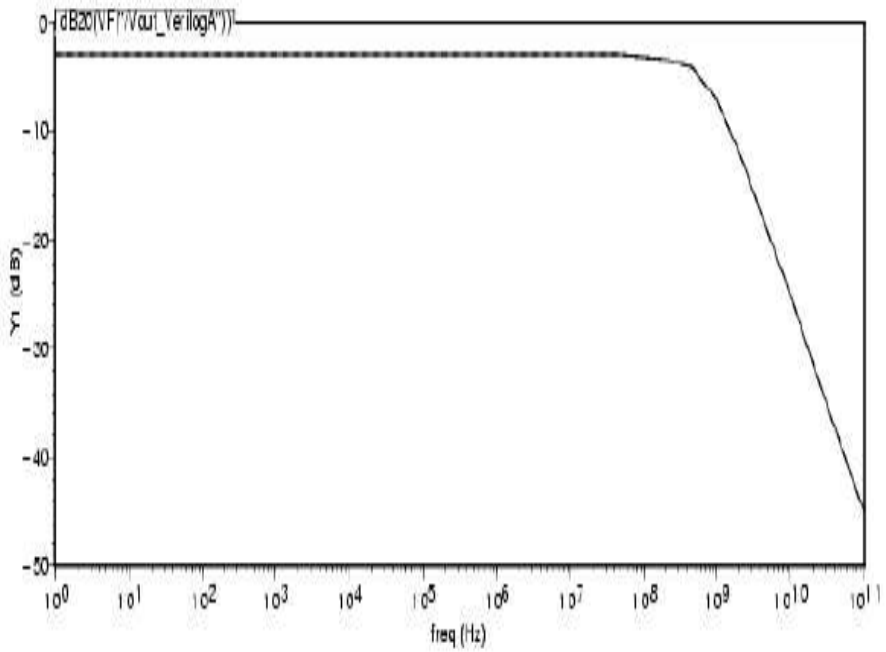
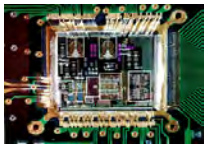


Figure: Simulation results of the Verilog-A code for **a low pass filter on a dB scale.**



Analog Design and Simulation Results of the Low Pass Filter

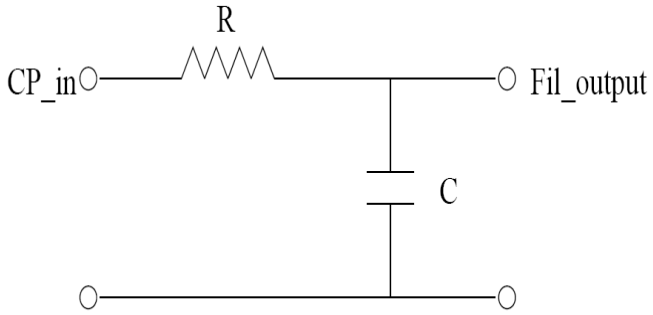


Figure: Circuit diagram of a low pass RC filter

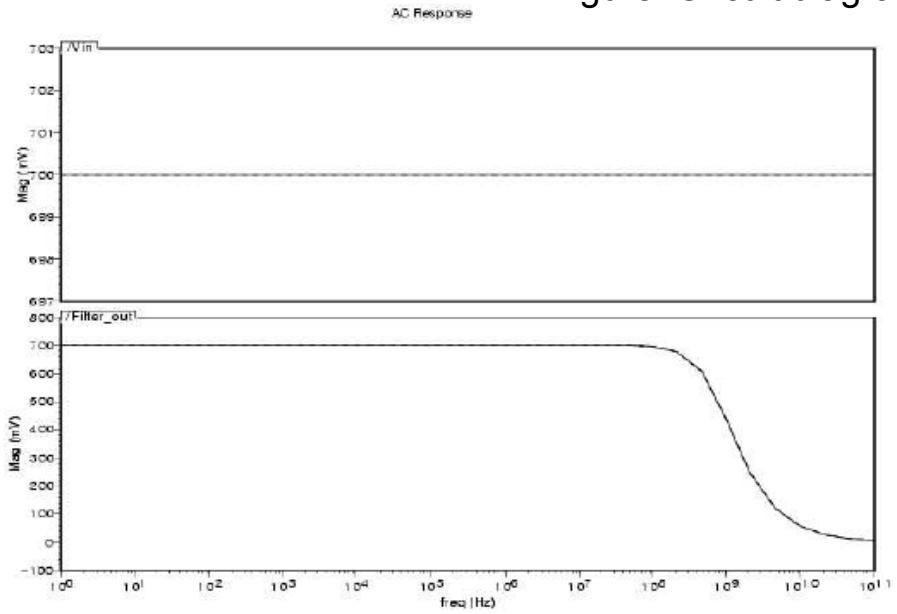


Figure: Simulation results for the **low pass RC filter**

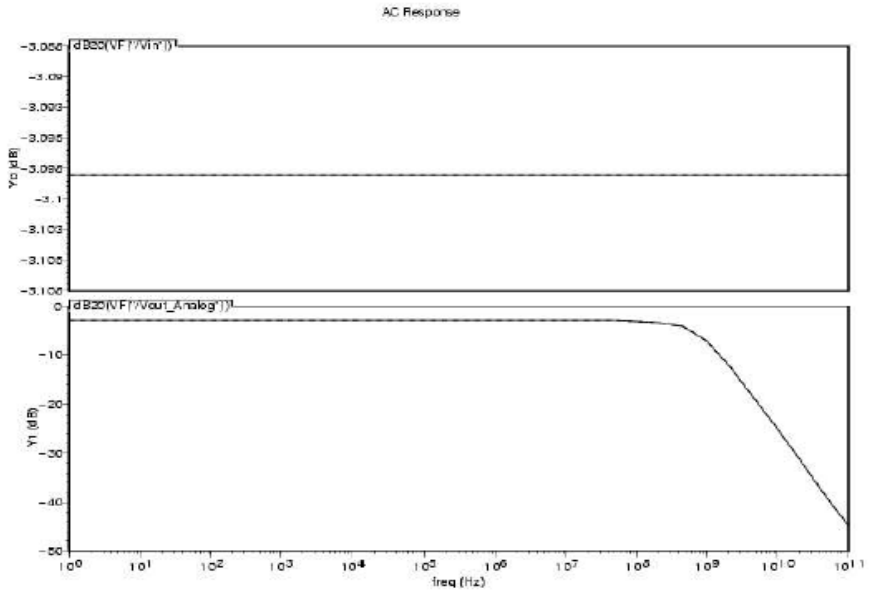
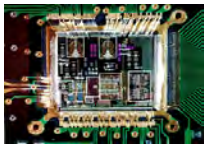


Figure: Simulation results for **the low pass RC filter on a dB scale.**



Comparative Simulation Results of Analog Low Pass Filter with Verilog-A modeled Low Pass Filter

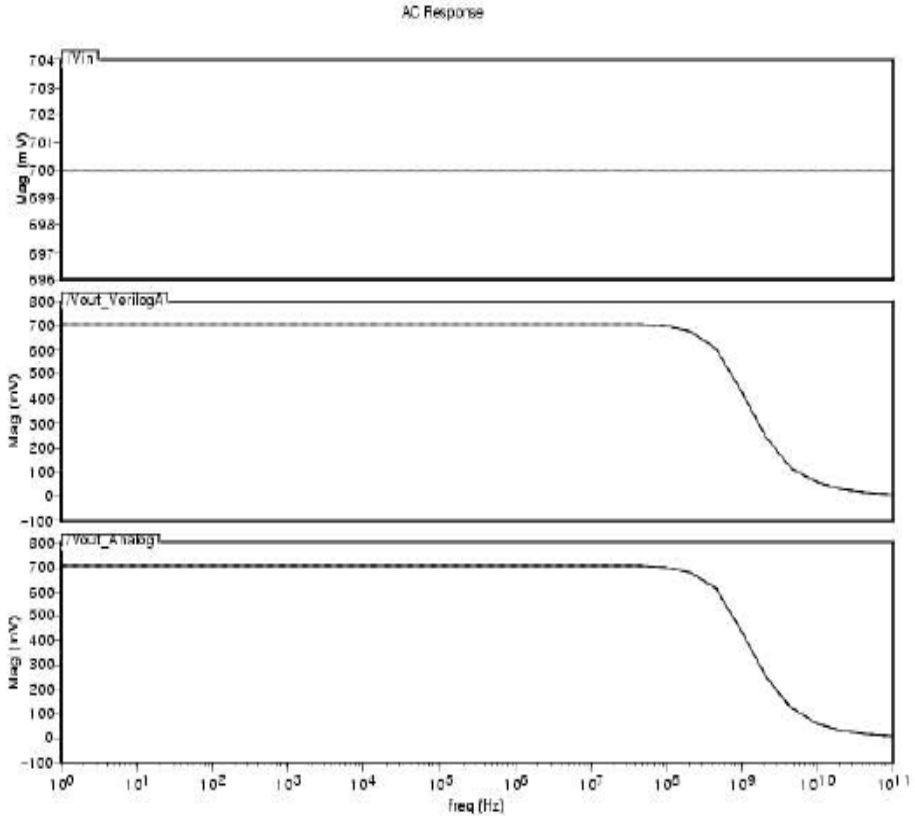


Fig: Comparative view of the simulation results of the low pass filter for the analog and Verilog-A system design approaches

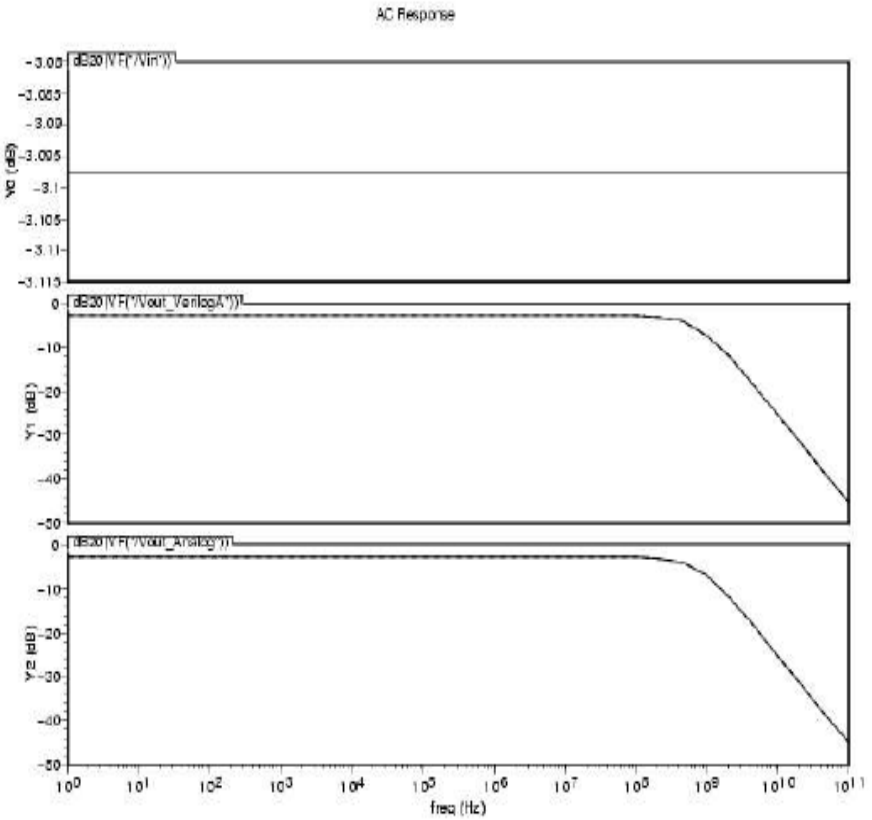
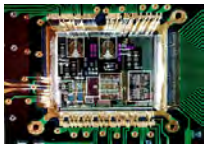
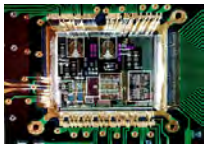


Fig: Comparative view of the simulation results of the low pass filter for the analog and Verilog-A system design approaches on a dB scale



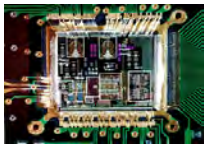
Mixed Signal Analysis

- Analog circuits
  - Signals are continuously varying voltages, currents or frequencies => provide accuracy
  - Voltage scaling and library design are the two problems related to the analog circuits
- Digital circuits
  - Signals are two-level discrete voltages that are either low or high => provide speed
  - Digital library can be easily built as any digital circuit would be a combination of different logic functions like NAND, NOR and data storage elements like flip-flops
- Issues with Analog Circuits
  - Decrease in supply voltage leads to lower performance
  - Gate leakage
- Mixed signal circuits
  - High accuracy and speed along with low cost and low power consumption
  - provide improved system reliability and flexibility
  - System performance is usually limited by the a2d or d2a interfaces as the speed of the data conversion has to be accounted



Mixed Signal Analysis on VCO and Frequency Divider

- VCO – Analog design => Transistor level
- Frequency divider – Digital design => Behavioral Verilog code
- Frequency of operation:
  - For VCO, f_{VCO} = 717.96 MHz
  - For analog frequency divider, f_a = 358.98 MHz
  - For digital frequency divider, f_d = 394.03 MHz
- Difference in frequency is due to:
  - Regular capacitive loading
  - Gate tunneling or leakage
- The difference in frequencies can be removed by adding a capacitor C_{LOAD} of 2.49 fF of which 2 fF is due to gate tunneling and 0.49 fF is due to capacitive loading
- Optimized Values of the Output Metric:
  - F^ = 786.43 MHz
  - P^ = 61.354 µW
  - P_L^ = 647.38 pW



Mixed Signal Analysis: Experimental Results

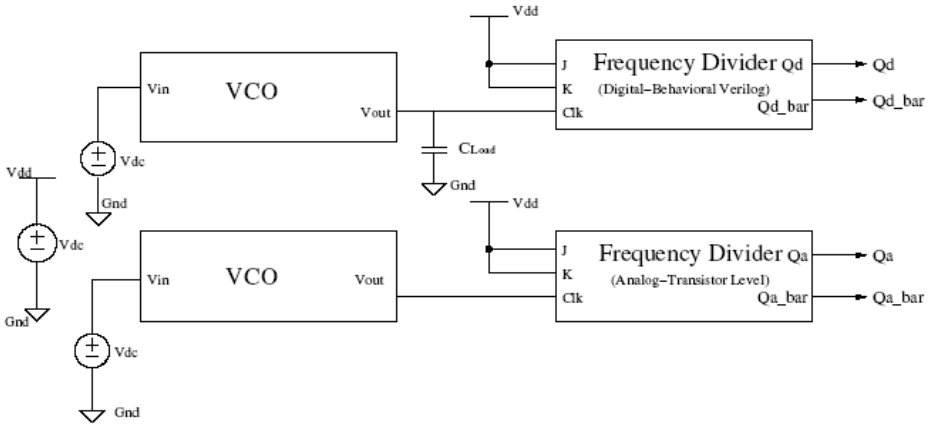


Figure: Block diagram of the VCO along with an analog frequency divider and a digital frequency divider

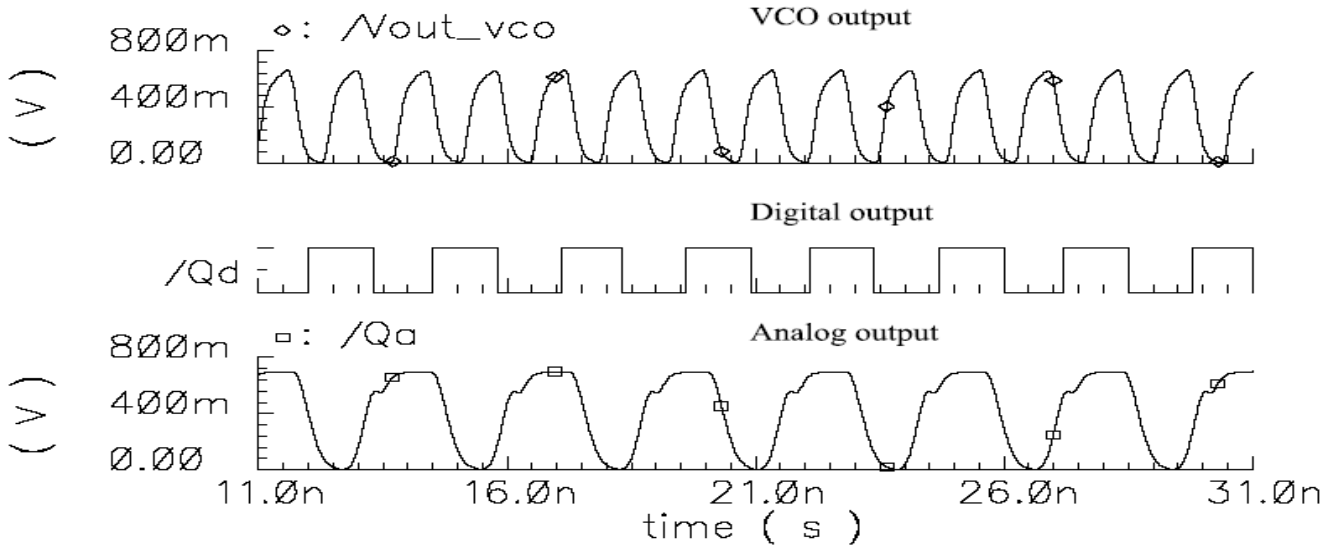


Figure: Output waveforms of the VCO, digital frequency divider and analog frequency divider