Lecture 2: Nano-CMOS Issues

CSCE 6933/5933
Advanced Topics in VLSI Systems

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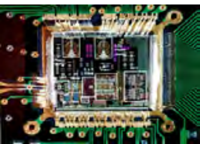
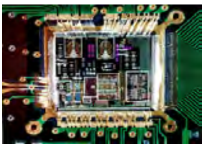


Nano-CMOS Circuit: Design Space

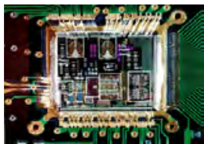
Nano-CMOS Design Space

- Power
- Leakage
- Delay
- Area
- Thermal
- Reliability
- Yield
- Variability



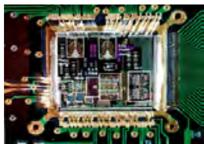
Issues in Nano-CMOS Circuits …

- **Variability**: Variability in process and design parameters has increased. They affect design decisions, yield, and circuit performance.
- **Leakage**: Leakage is increasing. Affects average as well as peak power metrics. Most significant for applications where system goes to standby mode very often, e.g. PDAs.
- **Power**: Overall chip power dissipation increasing. Affect energy consumption, cooling costs, packaging costs.



Issues in Nano-CMOS Circuits

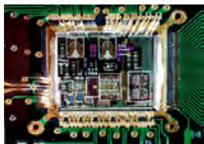
- **Thermals or Temperature**: Maximum temperature that can be reached by a chip during its operation is increasing. Affects reliability and cooling costs.
- **Reliability**: Circuit reliability is decreasing due to compound effects from variations, power, and thermals.
- **Yield**: Circuit yield is decreasing due to increased variability.



Variability: Origin and Sources

- Ion implantation
- Chemical mechanical polishing (CMP)
- Chemical vapor deposition (CVD)
- Sub-wavelength lithography
- Lens aberration
- Materials flow
- Gas flow
- Thermal processes
- Spin processes
- Microscopic processes
- Photo processes

Source: Singhal, DAC Booth 2007



Variability: Types …

Parametric Variations

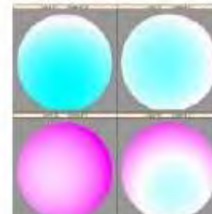
Wafer			Reticle	Local
Global	Linear	Radial	Caused by Photo Processes	Caused by Random Microscopic Processes
	Caused by Materials/Gas Flow	Caused by Thermal/Spin Processes		

Global

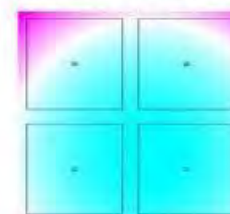
Linear

Radial

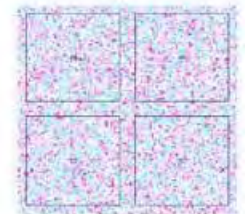
Wafer



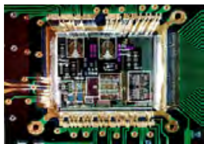
Across Reticle



Local

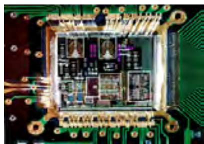


Source: Singhal, DAC Booth 2007



Variability: Types …

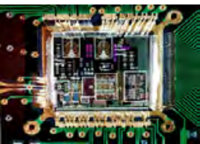
Global Variations		
Fab Process	Lot Process	Wafer Process
From Plant to Plant	From Lot to Lot in a Plant	From Wafer to Wafer in a Lot



Variability: Types …

Variability Classifications

- Inter-Die or Intra-Die
- Random or Systematic
- Correlated or Uncorrelated
- Spatial or Temporal



Variability: Types

- Process variations are classified as:
  - Inter-die and Intra-die.

Fab1

Fab2

Device to Device

Die to Die

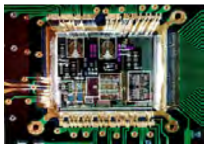
Wafer to Wafer

Lot to Lot

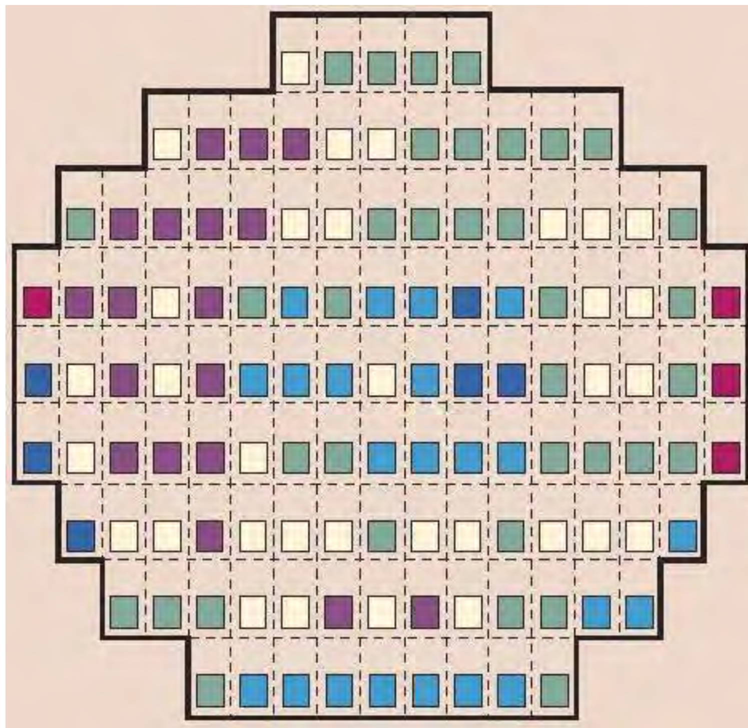
Line to Line

Intradie

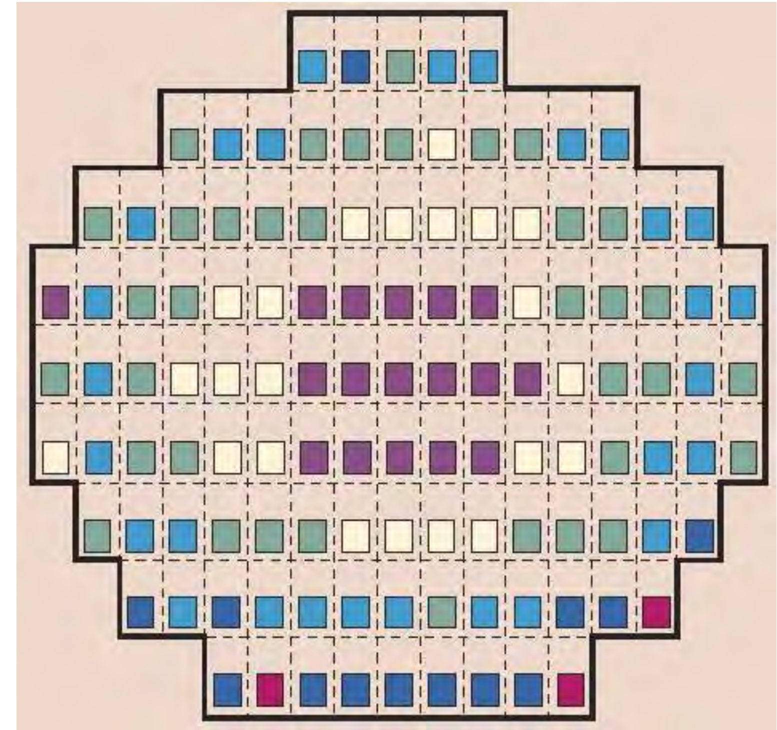
Interdie



Variability: The Impact in a Wafer …

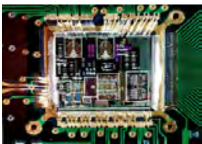


Source–drain resistance is different for different chips in a same die.



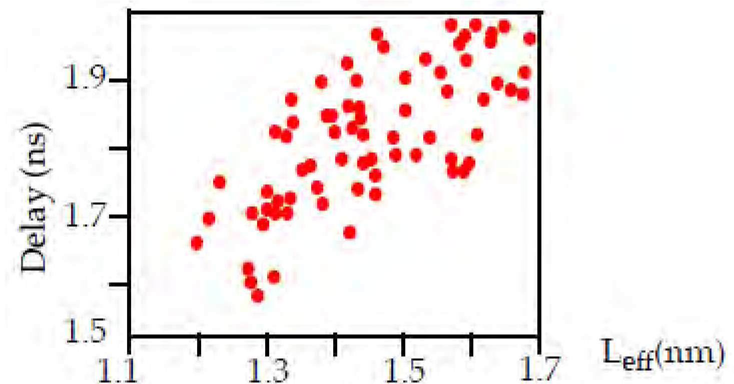
Gate-to-source and gate-to-drain overlap capacitance is different for different chips in a same die.

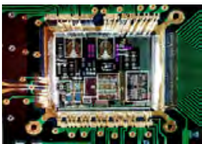
Source: Bernstein et al., IBM J. Res. & Dev., July/Sep 2006.



Variability: The Impact in a Wafer

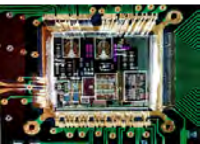
- The impact of process variations is seen as design yield loss.
- Digital circuits are typically optimized for speed and power.
- Analog circuits are designed to meet as many as five to ten performance metrics.
- Variations in process parameters have a resounding effect on the performance metrics of analog/mixed-signal and RF circuits.
- Figure showing impact of effective transistor channel length on the speed of an adder cell.



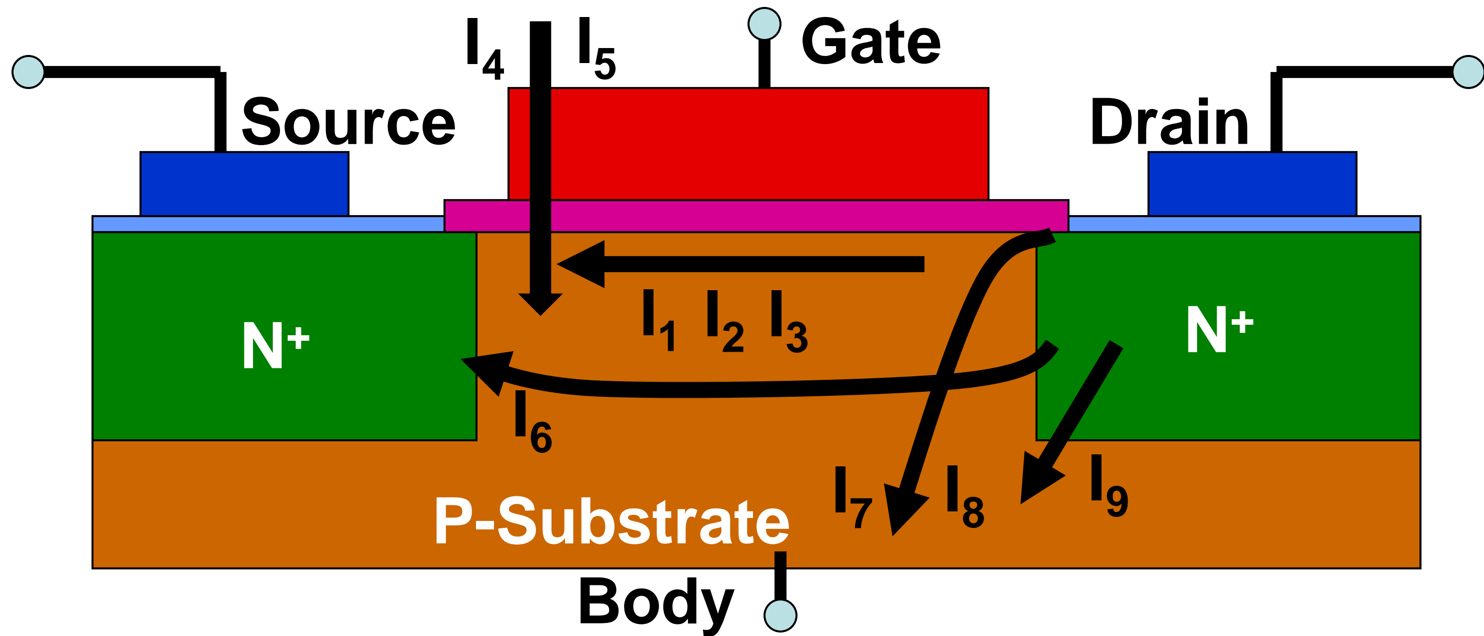


Variability: The 15 Device Parameters

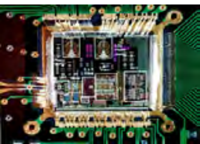
1) V_{DD}: supply voltage
2) V_{Thn}: NMOS threshold voltage
3) V_{Thp}: PMOS threshold voltage
4) t_{gaten}: NMOS gate dielectric thickness
5) t_{gatep}: PMOS gate dielectric thickness
6) L_{effn}: NMOS channel length
7) L_{effp}: PMOS channel length
8) W_{effn}: NMOS channel width
9) W_{effp}: PMOS channel width
10) N_{gaten}: NMOS gate doping concentration
11) N_{gatep}: PMOS gate doping concentration
12) N_{chn}: NMOS channel doping concentration
13) N_{chp}: PMOS channel doping concentration
14) N_{sdn}: NMOS source/ drain doping concentration
15) N_{sdp}: PMOS source/ drain doping concentration.



Power and Leakage …



I_1 : drain-to-source active current (ON state)
I_2 : drain-to-source short circuit current (ON state)
I_3 : subthreshold leakage (OFF state)
I_4 : gate Leakage current (both ON & OFF states)
I_5 : gate current due to hot carrier injection (both ON & OFF states)
I_6 : channel punch through current (OFF state)
I_7 : gate induced drain leakage (OFF state)
I_8 : band-to-band tunneling current (OFF state)
I_9 : reverse bias PN junction leakage (both ON & OFF states)

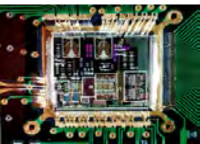


Power and Leakage

- The relative prominence of these components depend on:
  - Technology Node: 65nm, 45nm, or 32nm
  - Process : SiO_2/Poly or High-κ/Metal-Gate

SiO_2/Poly			High-κ/Metal-Gate		
Dynamic	Subthreshold	Gate	Dynamic	Subthreshold	Gate-Induced Drain Leakage (GIDL)

- BTBT tunneling is important for sub-45nm.



Nano-CMOS Design: Feedback Needed

Customer Specifications
System Design
Architecture Design
Logic Design
Circuit Design
Physical Design

Feedback for DFM

Silicon Specifications
Silicon Ingot
Slicing
Blank Wafers
Lithography Etching, Deposition
Wafer with circuit printed
Dicing
Die with Circuitry
Packaging Testing
Working Chips
Chip goes to Customers