Reconfigurable Robust Hybrid Oscillator Arbiter PUF for IoT Security based on DL-FET

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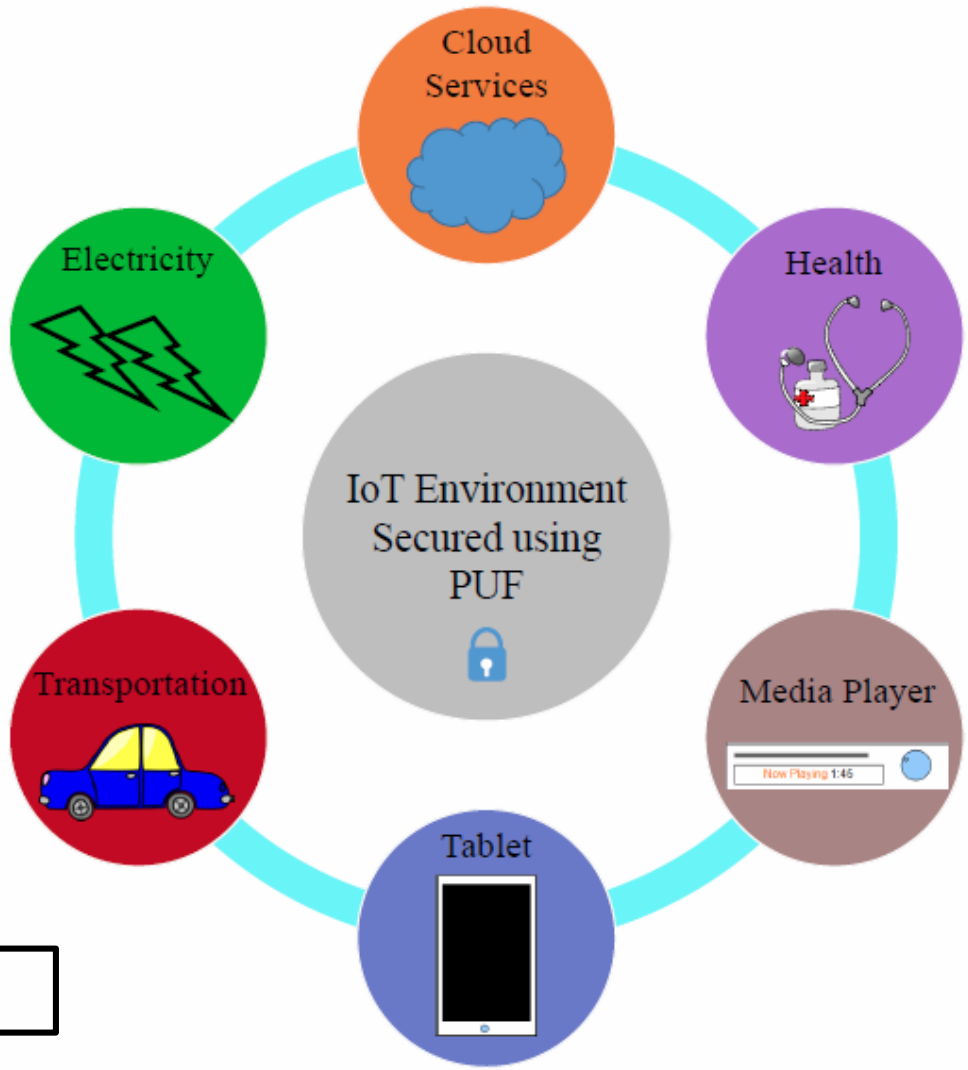
Outline of the talk

- IoT and Attacks
- Novel Contributions
- Physical Unclonable Functions
- Reconfigurable Architecture
- Results
- Conclusion and Future Research

Internet of Things

- Internet of Things is a network of devices where each and every device in the network is recognizable and connected



Internet of (Every)thing !!

Security in the Internet of Things

Novel Contributions

- Two designs of Reconfigurable Hybrid Oscillator Arbiter Physical Unclonable Functions are Implemented using DL-FETs.
- To the authors' best knowledge, this is the first paper using DL-FETs.

What is PUF ?

Physical Unclonable Functions (PUFs) is based on the idea that even though the mask and manufacturing process is the same among different ICs, each IC is slightly different due to the manufacturing variability.[1]

[1] C. Herder, M. D. Yu, F. Koushanfar and S. Devadas, "Physical Unclonable Functions and Applications: A Tutorial," in *Proceedings of the IEEE*, vol. 102, no. 8, pp. 1126-1141, Aug. 2014.

Why PUF ?

- Strong authentication
- Uniqueness
- Unclonability

Unclonable randomness !!

PUF

A Silicon "biometric"!!

Advantage of PUF

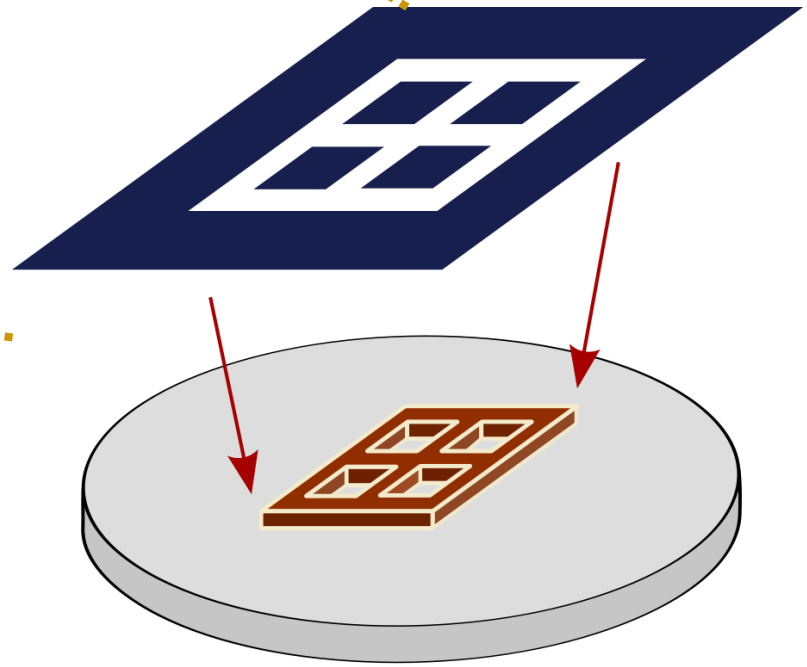
- PUF architectures are composed of simple digital circuits which consume less area and power.
- It does not require expensive cryptographic hardware or encryption algorithms.
- It is very difficult to change physical characteristics of the IC.

How PUF Works

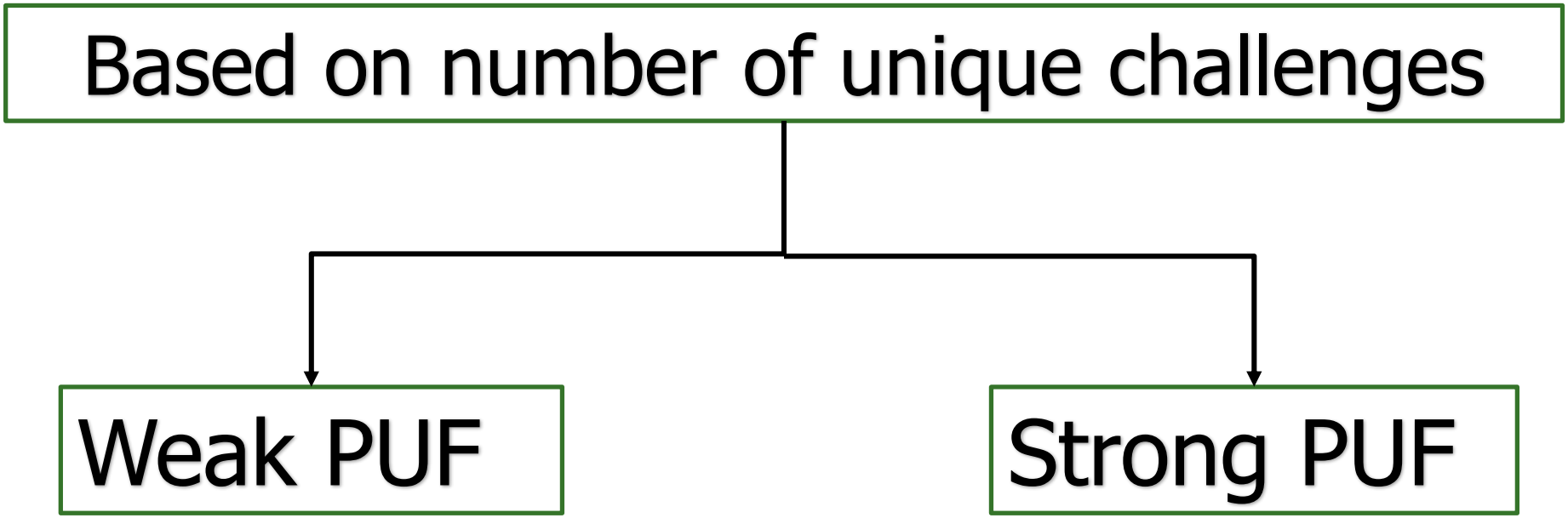
How PUF Works

Process Variation

Mismatch Variation



Types of PUF



Types of PUF

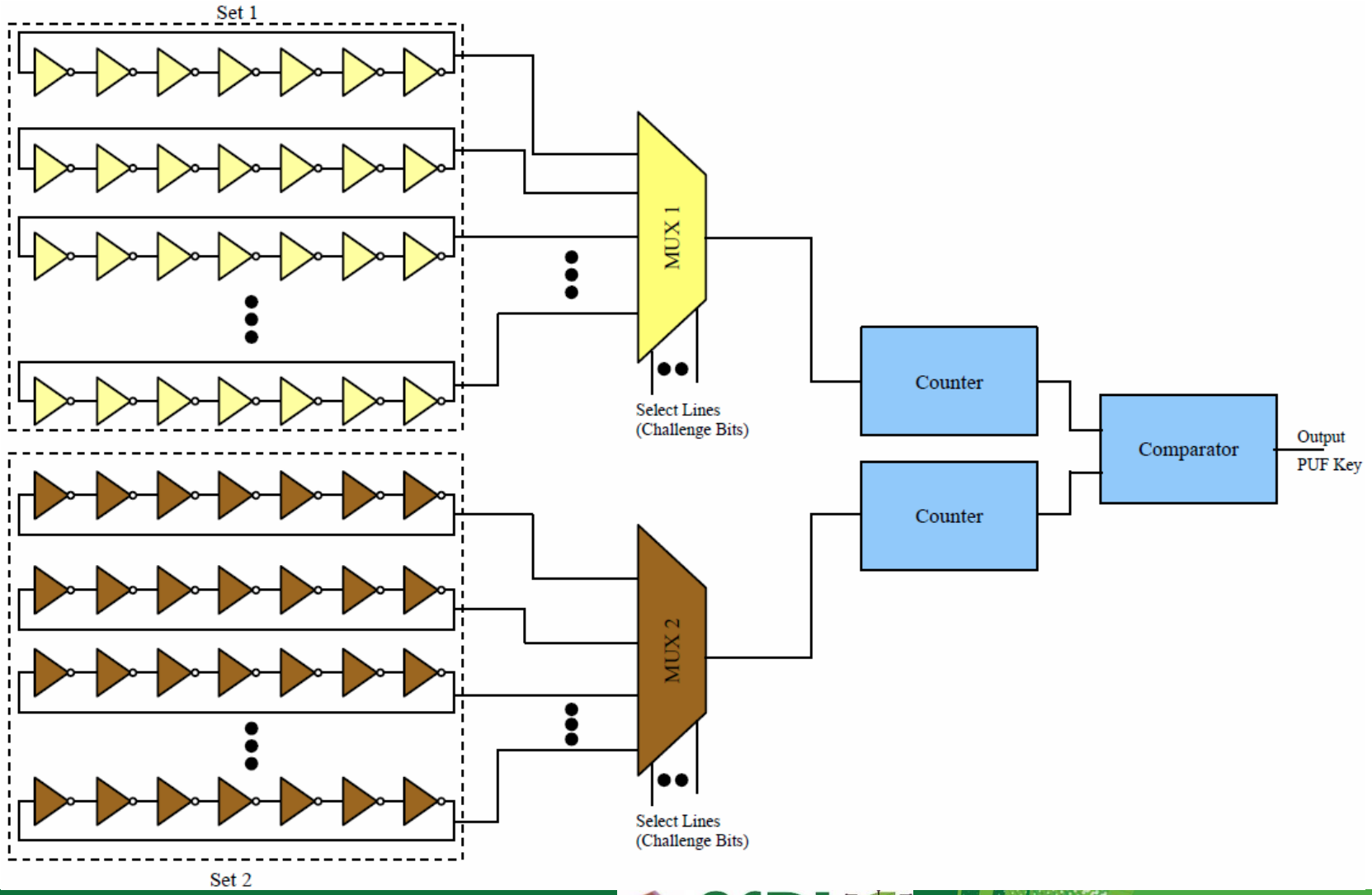
Strong PUF

- Optical PUF
- Arbiter PUF

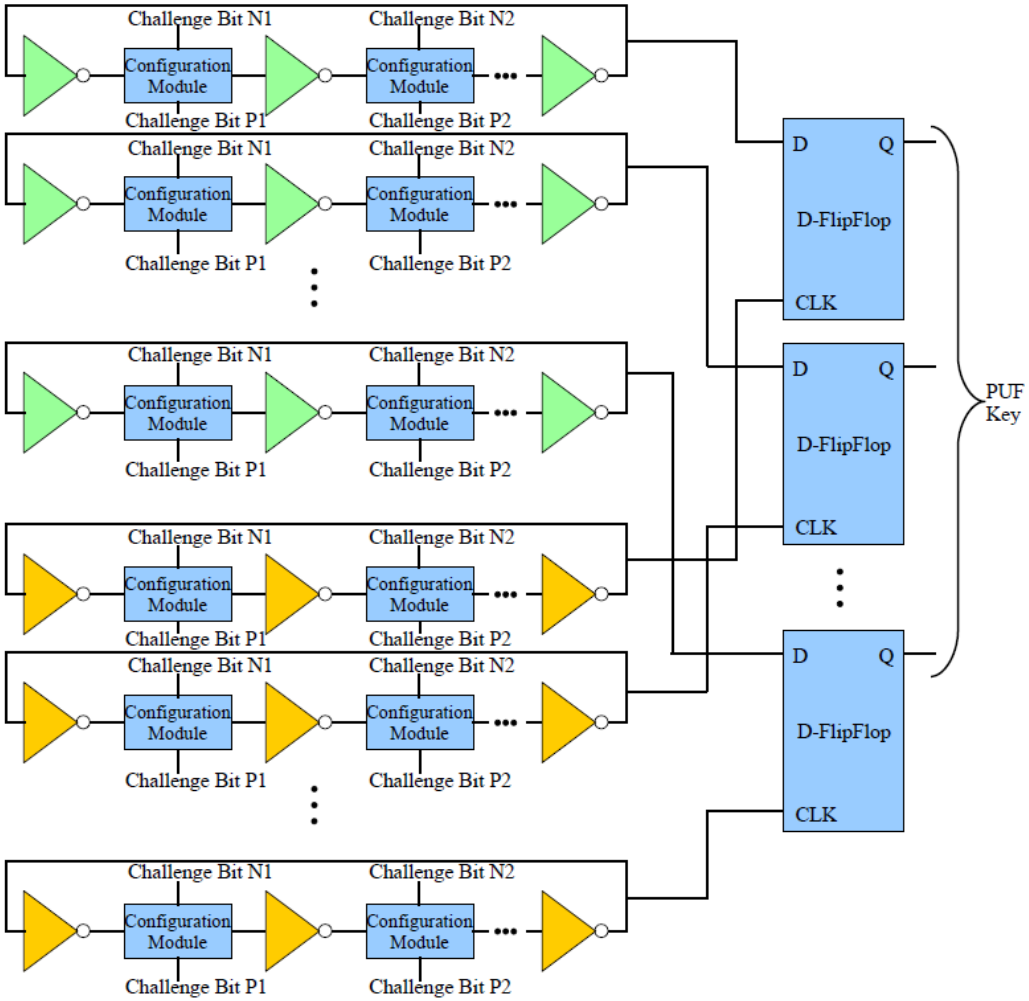
Weak PUF

- RO PUF
- SRAM PUF

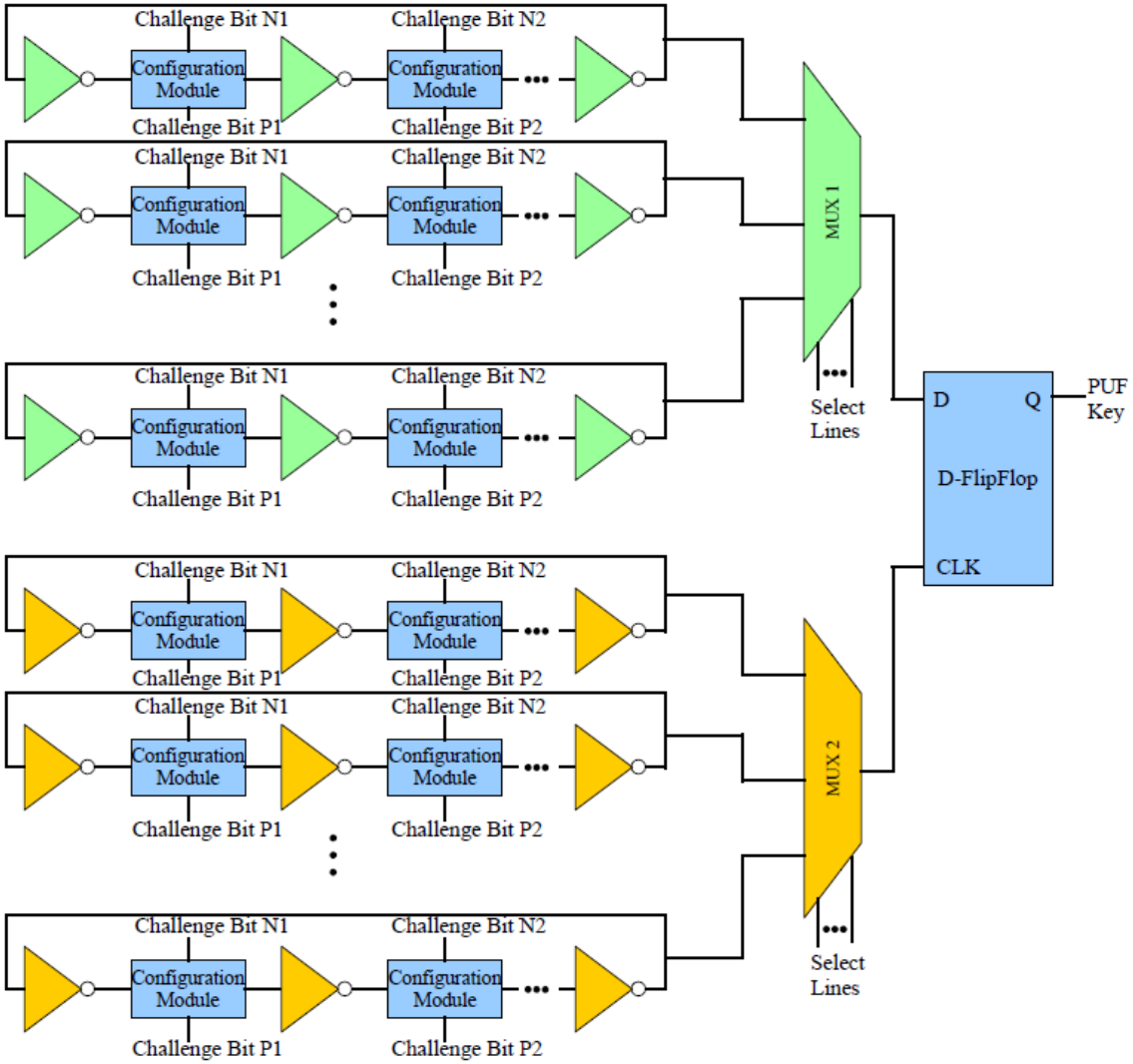
DL-FET Based Conventional RO PUF



Speed Optimized Hybrid Oscillator Arbiter PUF



Power Optimized Hybrid Oscillator Arbiter PUF



Configuration Module

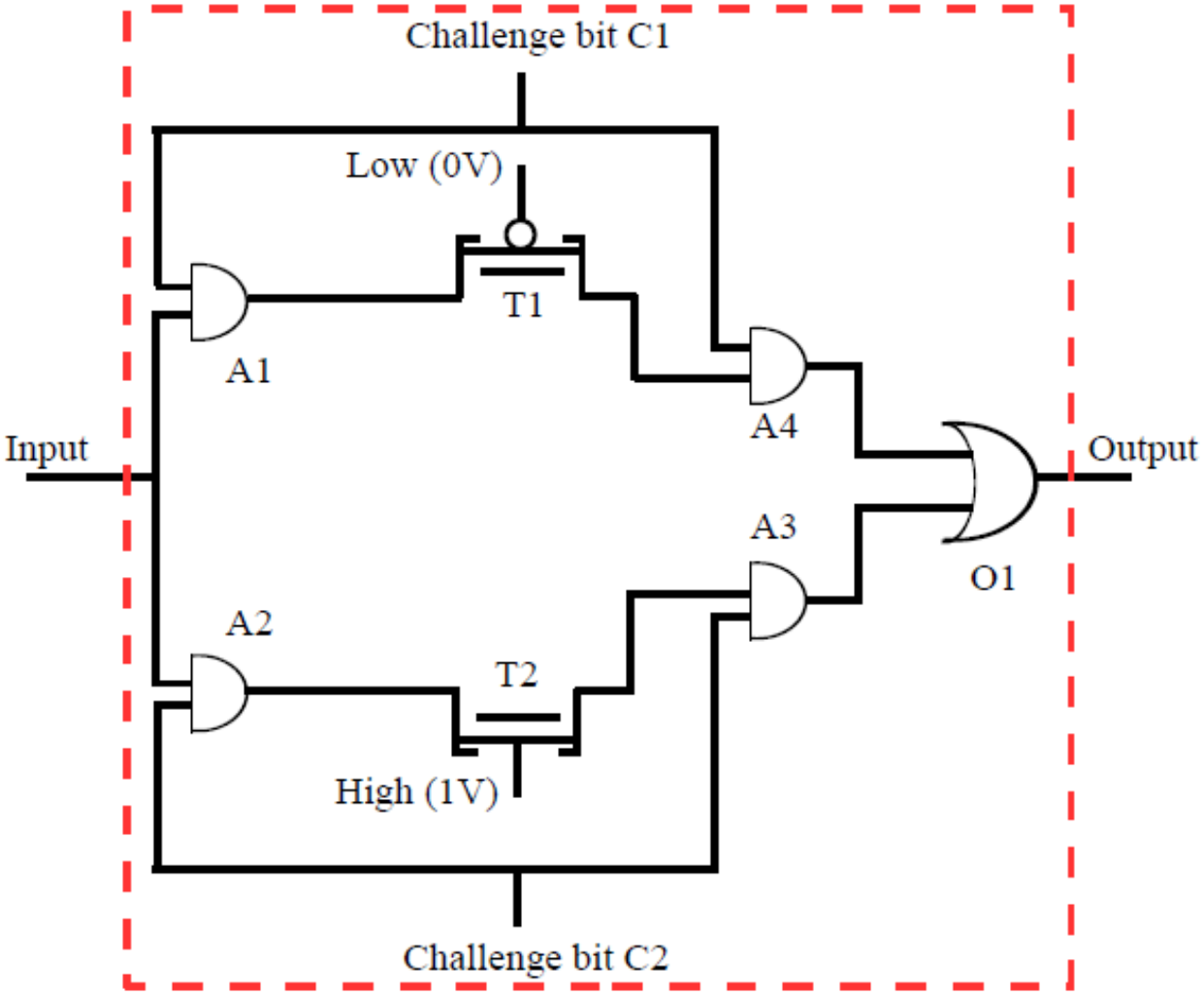


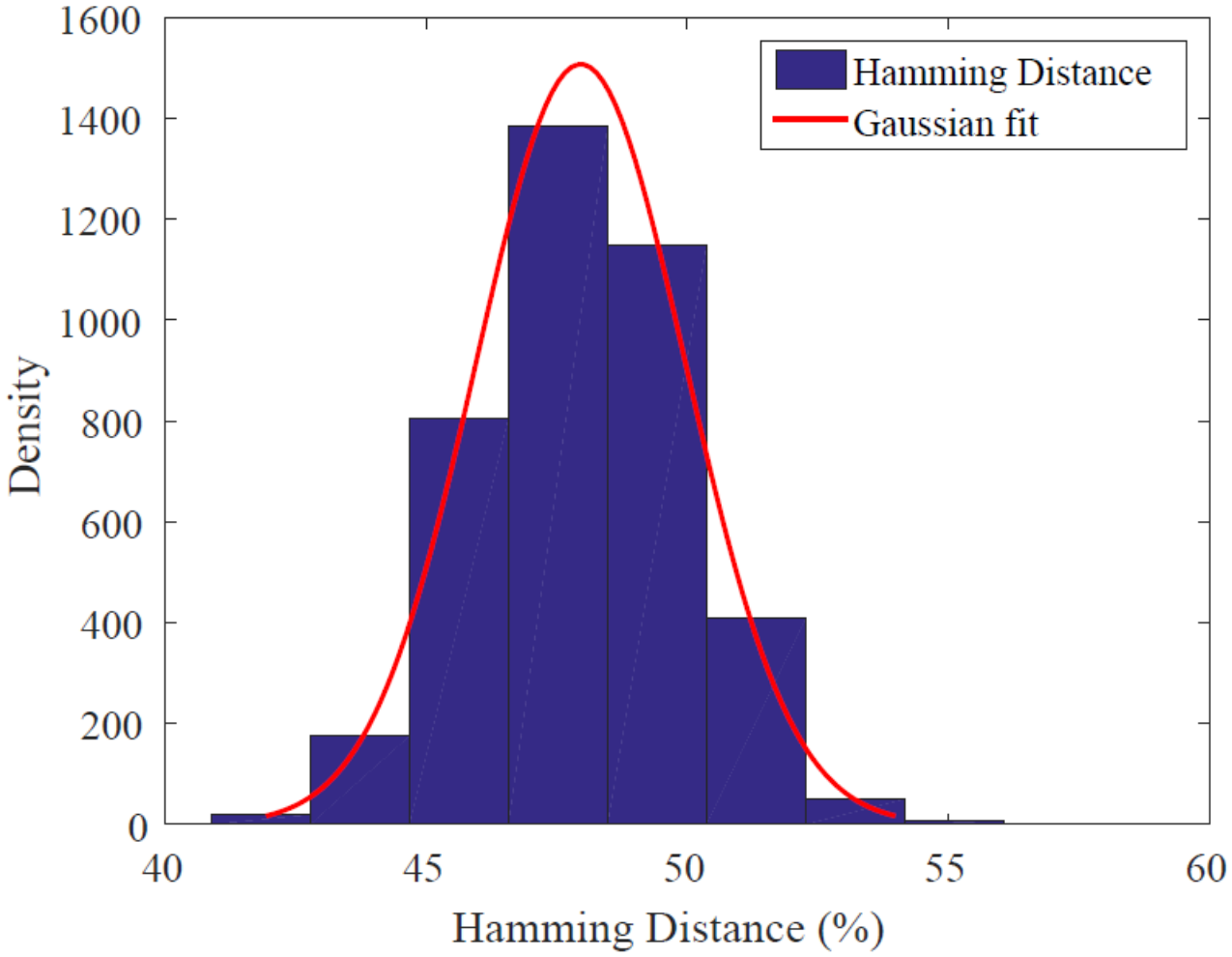
Figure of Merits

- Hamming Distance : The hamming distance between two keys should be 50%.
- Reliability : If the same PUF is run with the same challenge input, with environment variations, the output key should not change – Hamming distance should be 0.

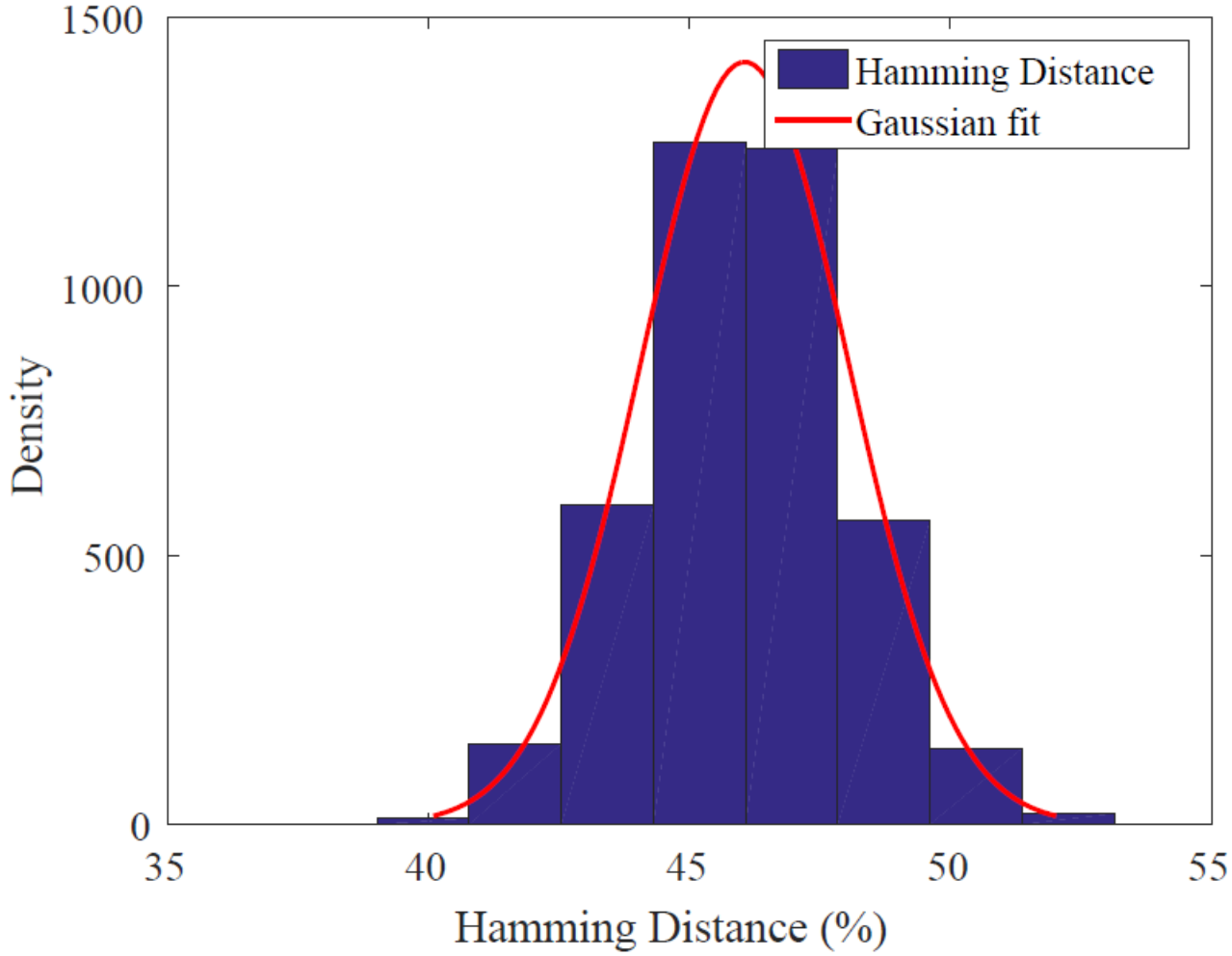
Figure of Merits

- Average Power consumption : Power Consumed by the design.
- Randomness : Randomness is the number of 0's and 1's present in the output key. Ideally it should be 50% of both.

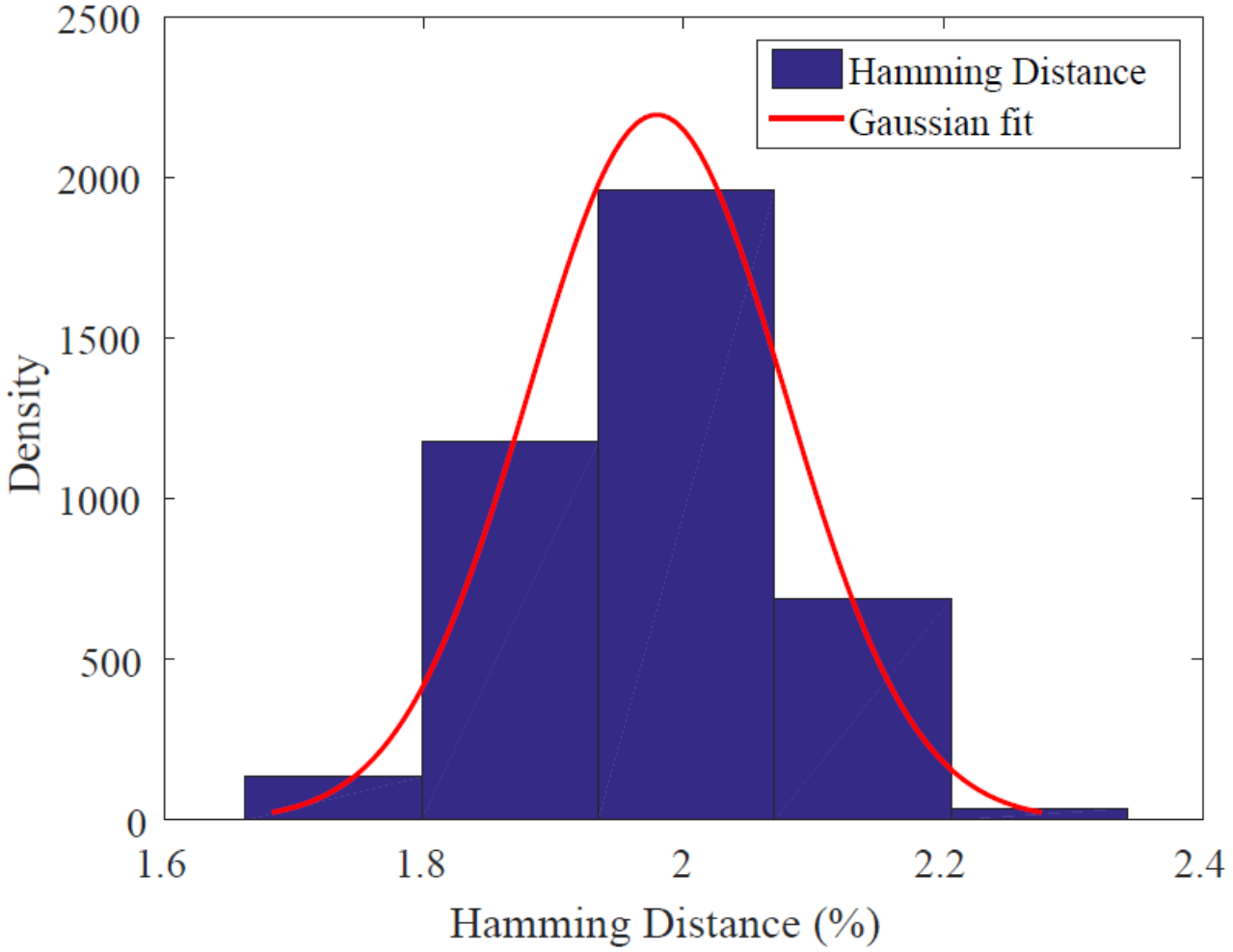
Inter PUF Hamming Distance of Speed Optimized Hybrid Oscillator Arbiter PUF



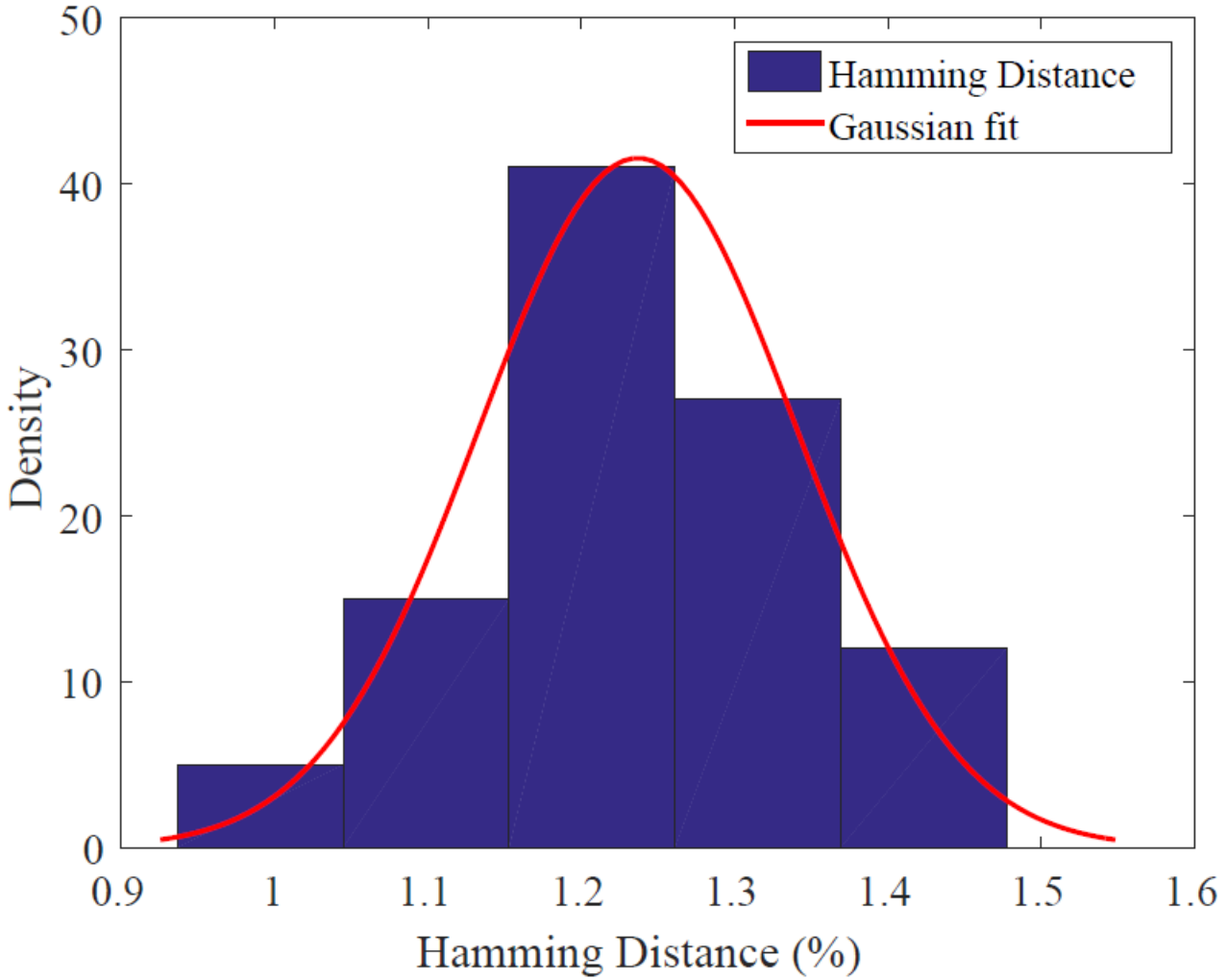
Inter PUF Hamming Distance of Power Optimized Hybrid Oscillator Arbiter PUF



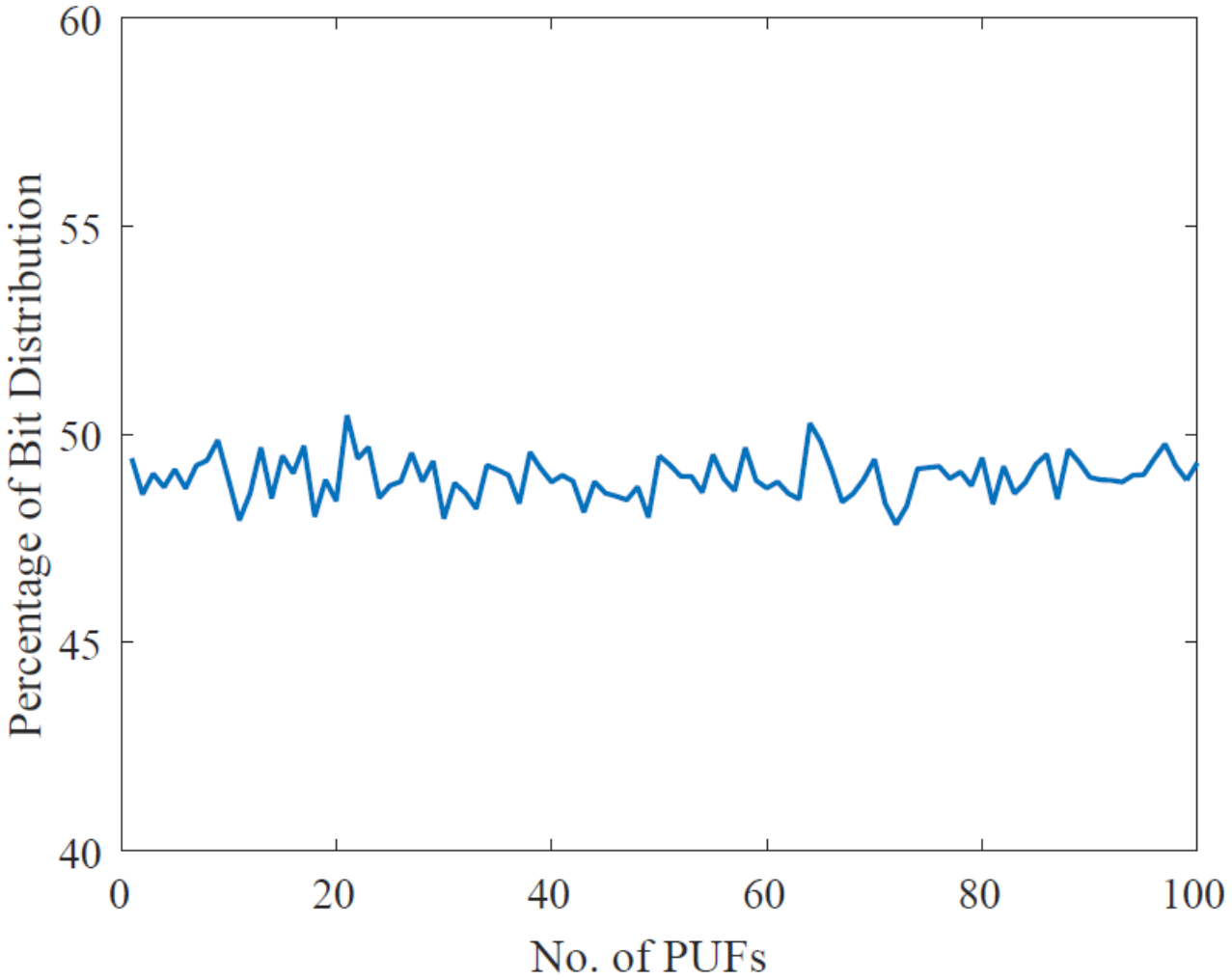
Intra PUF Hamming Distance of Speed Optimized Hybrid Oscillator Arbiter PUF



Intra PUF Hamming Distance of Power Optimized Hybrid Oscillator Arbiter PUF



Randomness


60
55
50
45
40
Percentage of Bit Distribution
0
20
40
60
80
100
No. of PUFs

Average Power of Speed Optimized Hybrid Oscillator Arbiter PUF

Research Works	Technology	Architecture Used	Average Power Consumed	Hamming Distance (%)
Rahman et al. [17]	90nm CMOS	--	--	50
Maiti et al. [9]	180nm CMOS	Ring Oscillator	--	50.72
Sahoo et al. [18]	90nm CMOS	Ring Oscillator	--	45.78
Yanambaka et al. [16]	32nm FinFET	Hybrid Oscillator Arbiter	175.5 µW	47.31
This paper (Power Optimized)	10 nm DL-FET	Reconfigurable Hybrid Oscillator Arbiter	143.3 µW	47.0
This paper (Speed Optimized)	10nm DL-FET	Reconfigurable Hybrid Oscillator Arbiter	167.5 µW	48.0

Conclusion and Future Research

- This paper presents two designs of reconfigurable hybrid oscillator arbiter PUFs, a speed optimized and a power optimized design using DL-FETs.
- A fair comparison of the two technologies, FinFET and DL-FETs is presented to show the power reduction using these transistors.
- As a future research, an ultra low power design of PUF can be implemented.

THANK YOU