Dopingless Transistor based Hybrid Oscillator Arbiter Physical Unclonable Function

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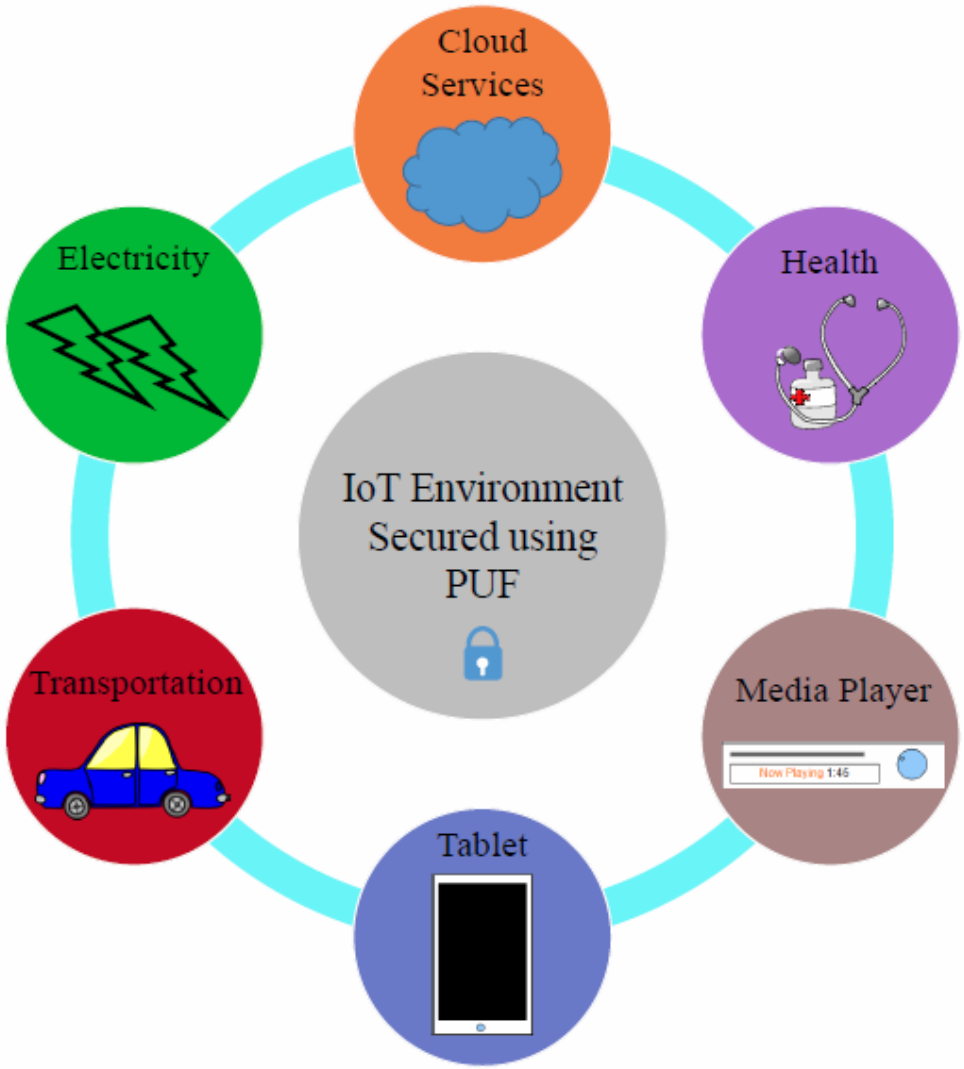
Outline of the talk

- IoT and Attacks
- Novel Contributions
- Physical Unclonable Functions
- Proposed Designs of Physical Unclonable Function
- Results and FoMs
- Conclusion and Future Research

Internet of Things

- In the IoT era, the number of devices connected to the internet is exponentially increasing.



Security in the Internet of Things

Secure Network under lock and key

Security in the Internet of Things

Novel Contributions

- Two designs of Hybrid Oscillator Arbiter Physical Unclonable Functions are implemented using DL-FETs.
- Comparative analysis with FinFETs is presented for the same designs.
- To the authors' best knowledge, this is the first paper using DL-FETs.

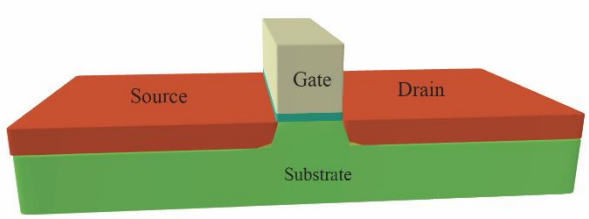
Technology Scaling

90nm CMOS

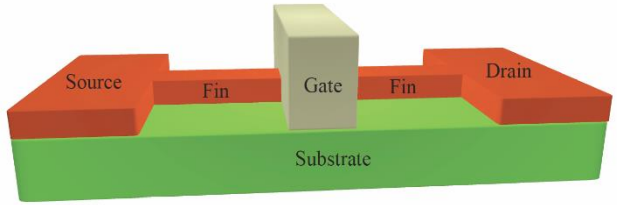
32nm CMOS

14nm FinFET

???

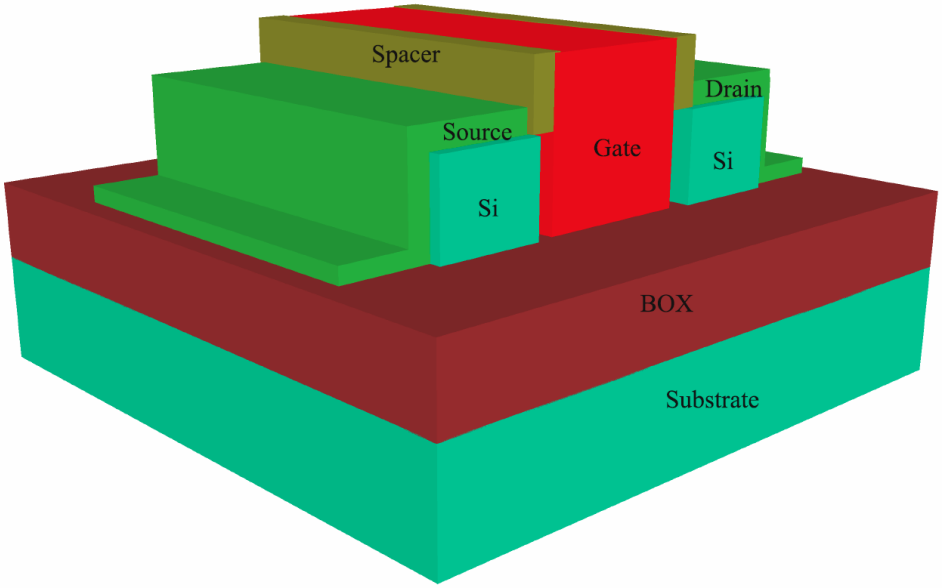


CMOS



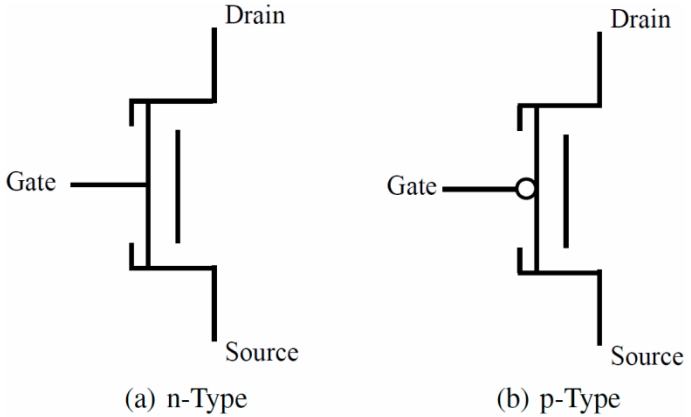
FinFET

Dopingless Transistor



Structure of Dopingless FET

Symbols of n-type and p-type Dopingless FET



Dopingless Transistor

- An undoped single uniform structure is used from source to drain.
- In the DL-FET, a thin intrinsic silicon nanowire is used between metal electrodes and gate, source and drain regions.
- The p-type and the n-type doping regions can be formed using work function engineering inside the undoped thin silicon.

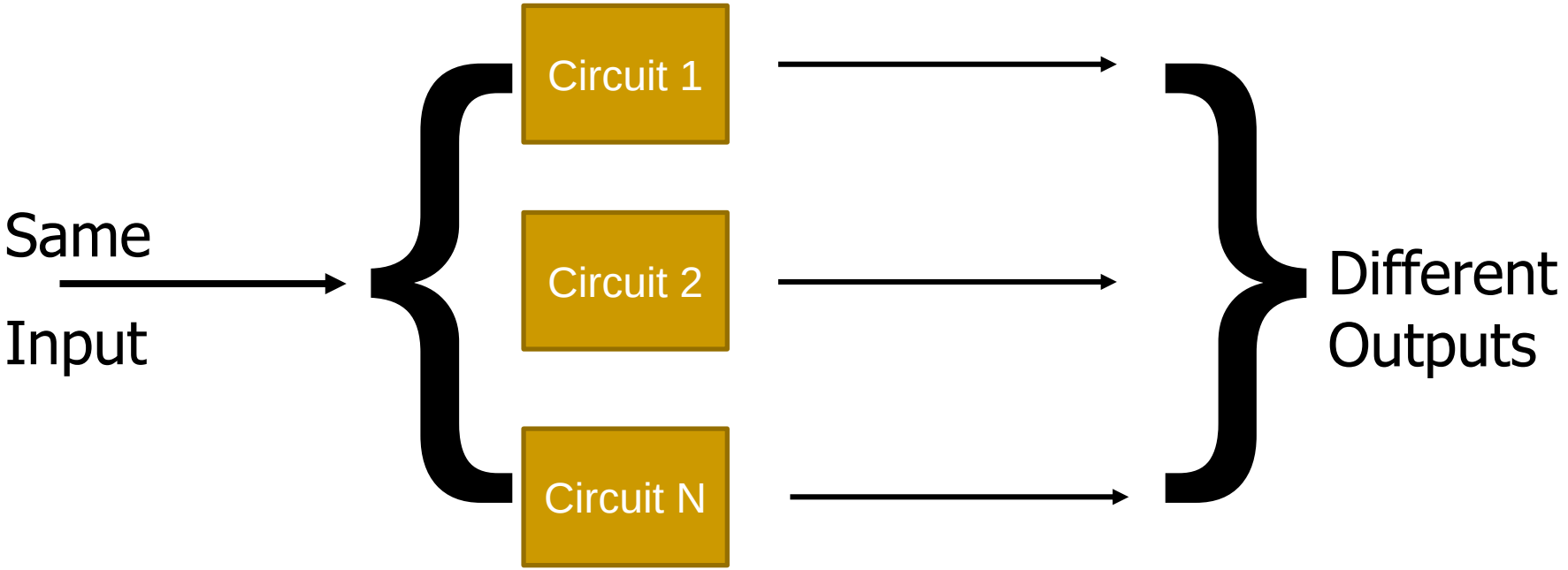
Dopingless Transistor

Parameters	Dopingless FET
Silicon Film Thickness (T_{si})	10 nm
Effective Oxide Thickness (EOT)	1 nm
Gate Length (L_g)	20 nm
Width (W)	1 μm
Source/Drain extension	10 nm
Metal work function/doping for source/drain	3.9 EV (Hafnium)
Metal work function/doping for gate	4.66 eV (TiN)
Doping	$10^{15}/cm^3$

Physical Unclonable Function

- Physical Unclonable Functions are simple primitives for security.
- PUFs are easy to build and impossible to duplicate (theoretically).
- Input and Output are called Challenge Response Pair.

How PUF Works

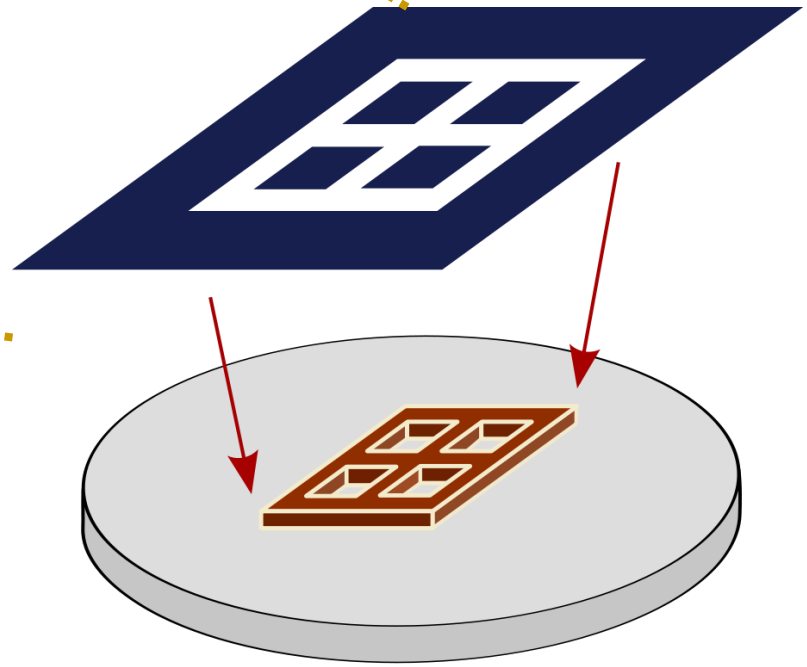


With the same input to different copies of the same circuit, different outputs are obtained, each unique to each circuit.

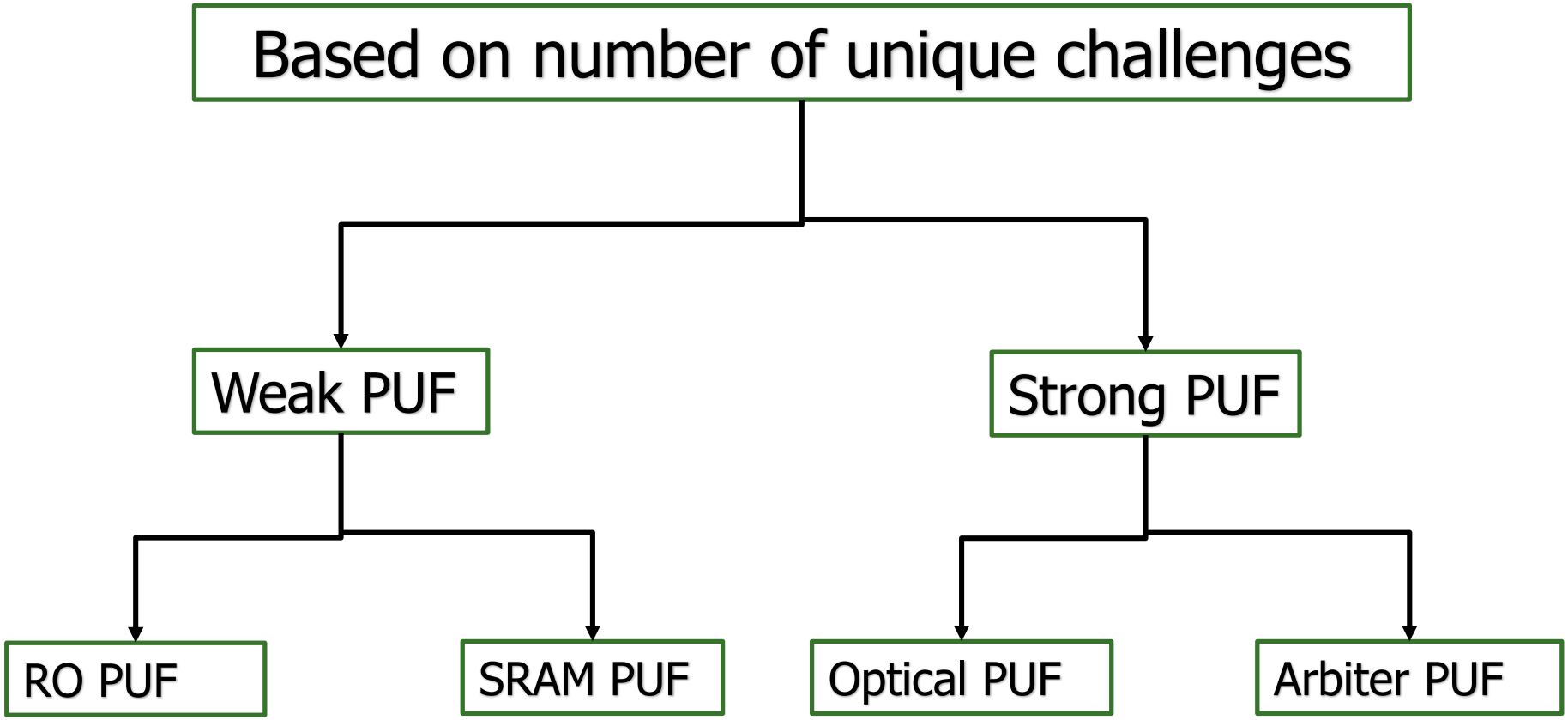
How PUF Works

Process Variation

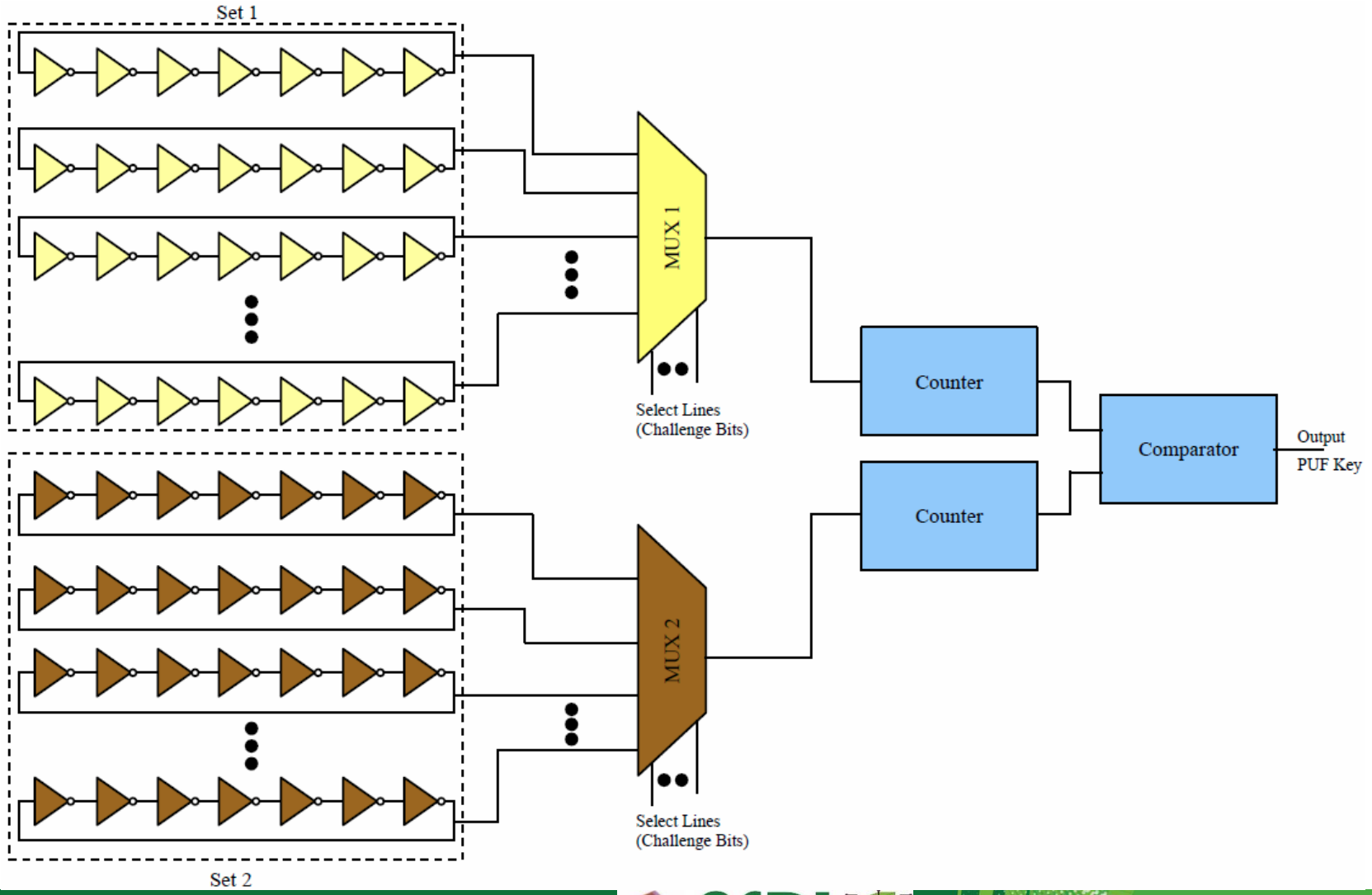
Mismatch Variation



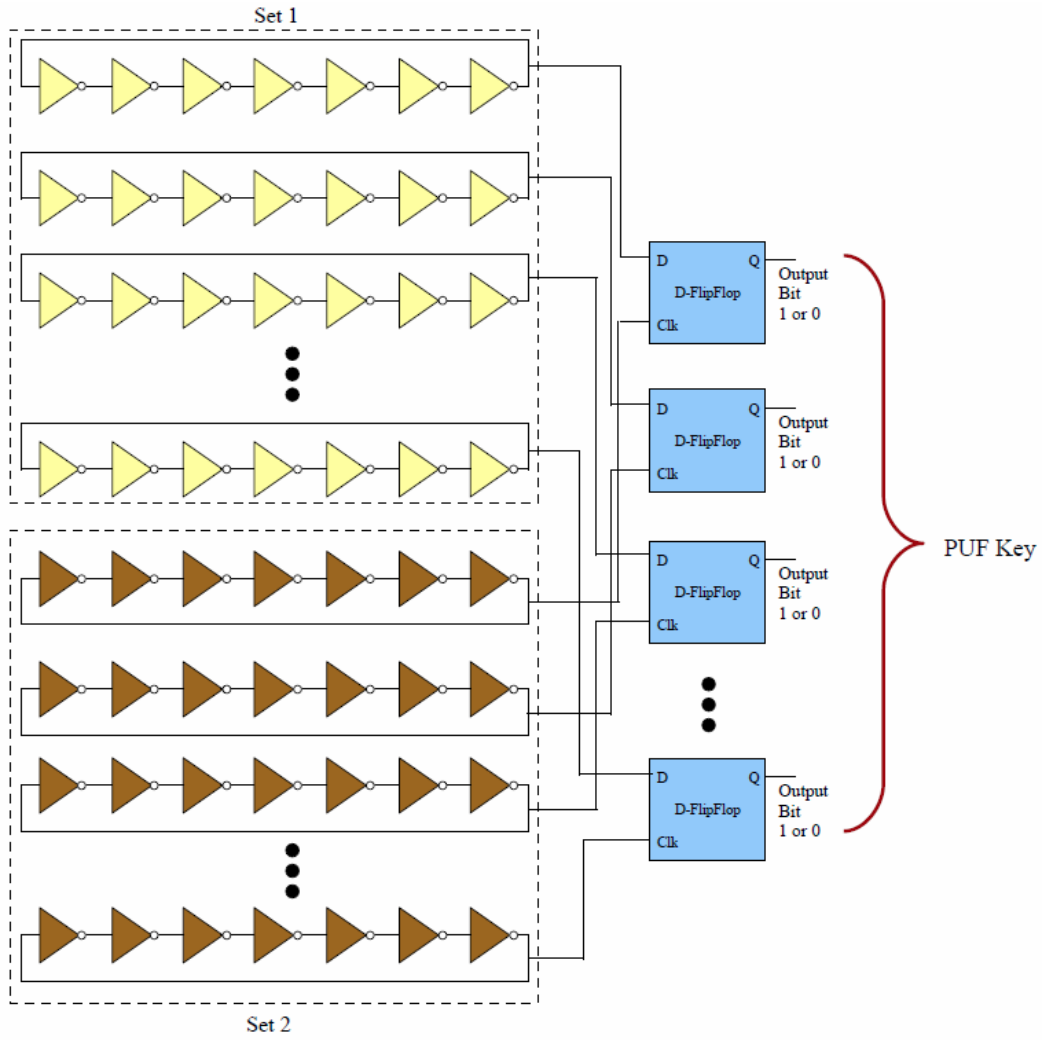
Types of PUF


Based on number of unique challenges
Weak PUF
Strong PUF
RO PUF
SRAM PUF
Optical PUF
Arbiter PUF

DL-FET Based Conventional RO PUF



Speed Optimized Hybrid Oscillator Arbiter PUF



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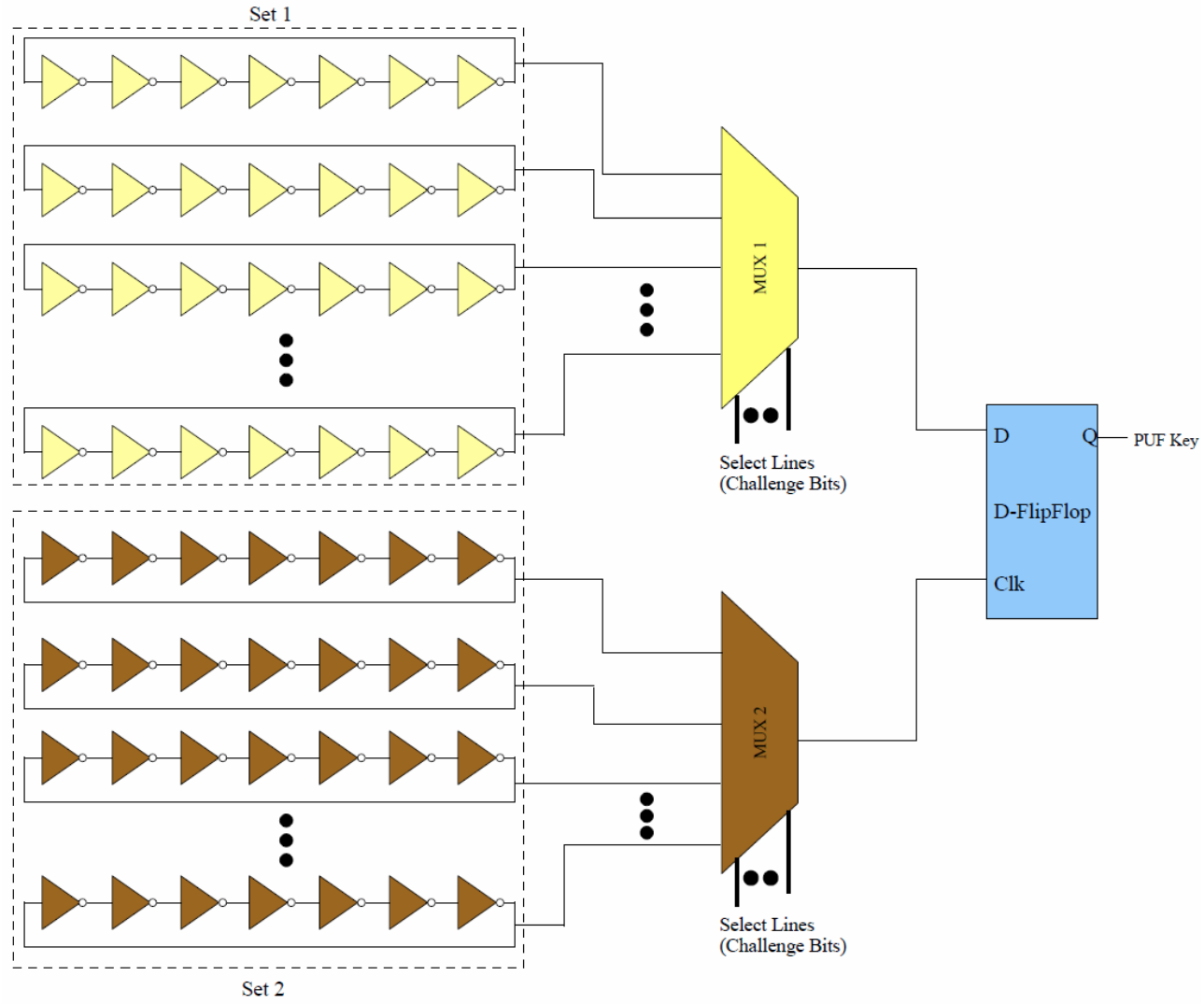
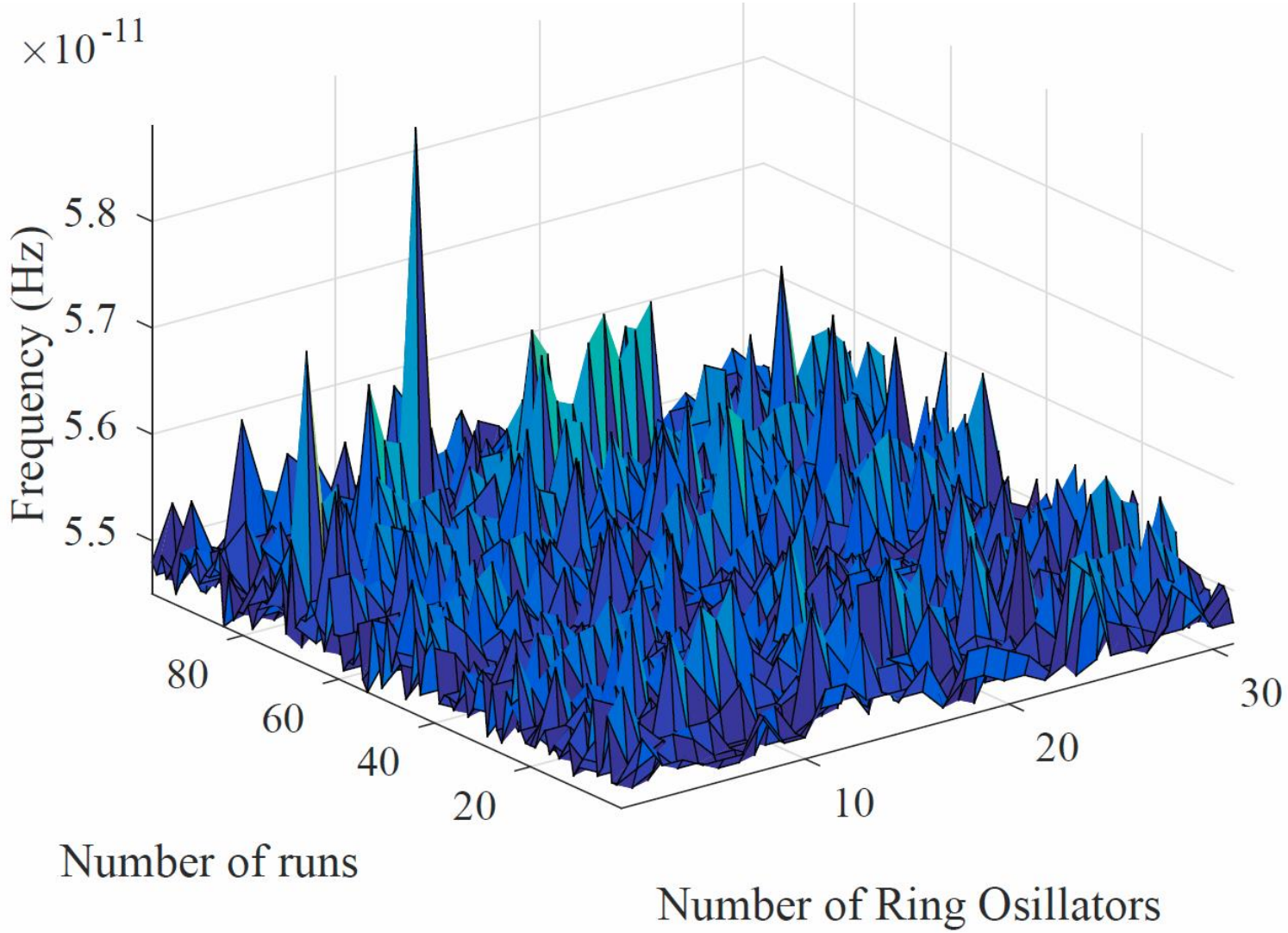


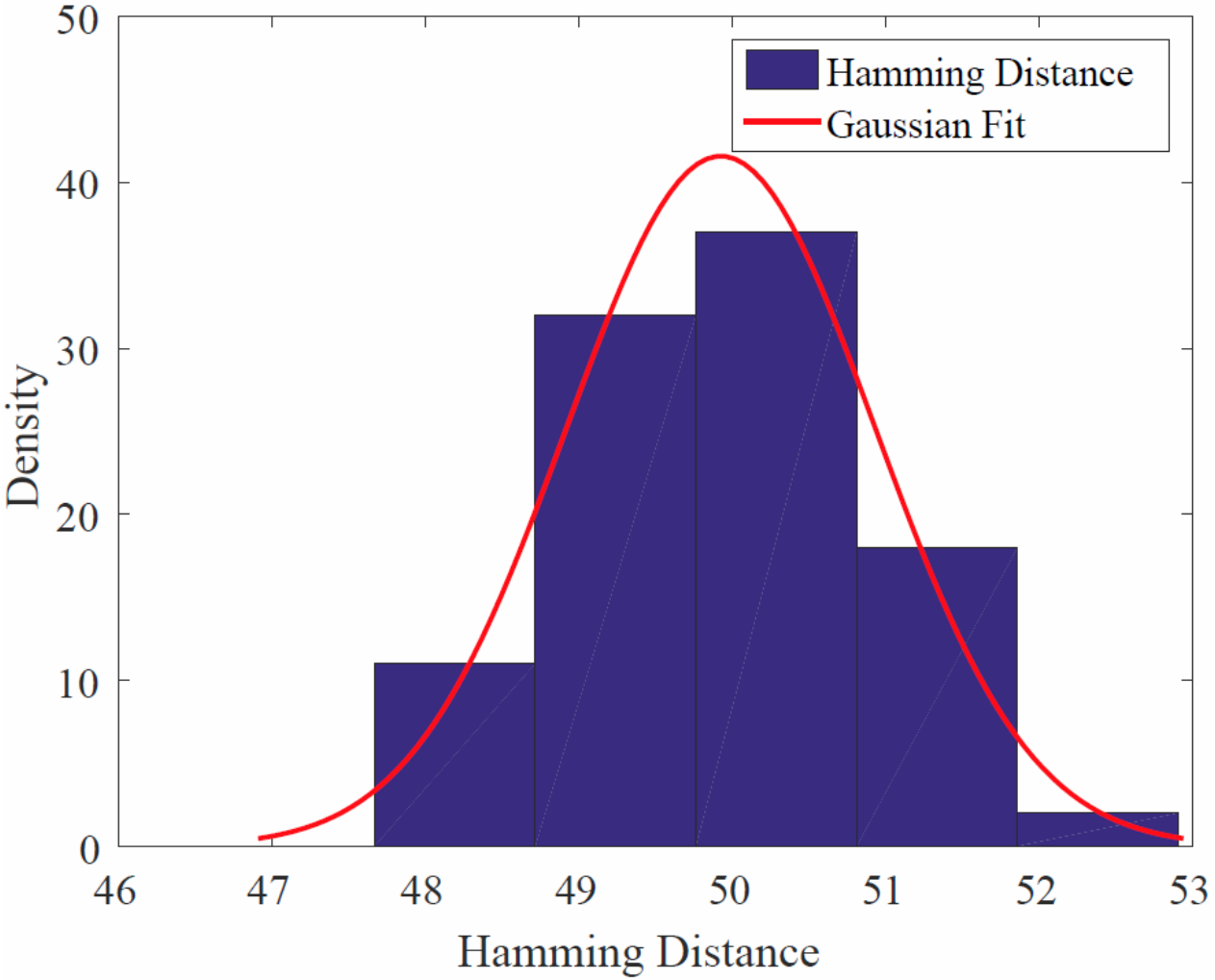
Figure of Merits

- Hamming Distance : The hamming distance between two keys should be 50%.
- Reliability : If the same PUF is run with the same challenge input, with environment variations, the output key should not change – Hamming distance should be 0.
- Average Power consumption.

Frequencies of Ring Oscillators



Inter PUF Hamming Distance of Speed Optimized Hybrid Oscillator Arbiter PUF



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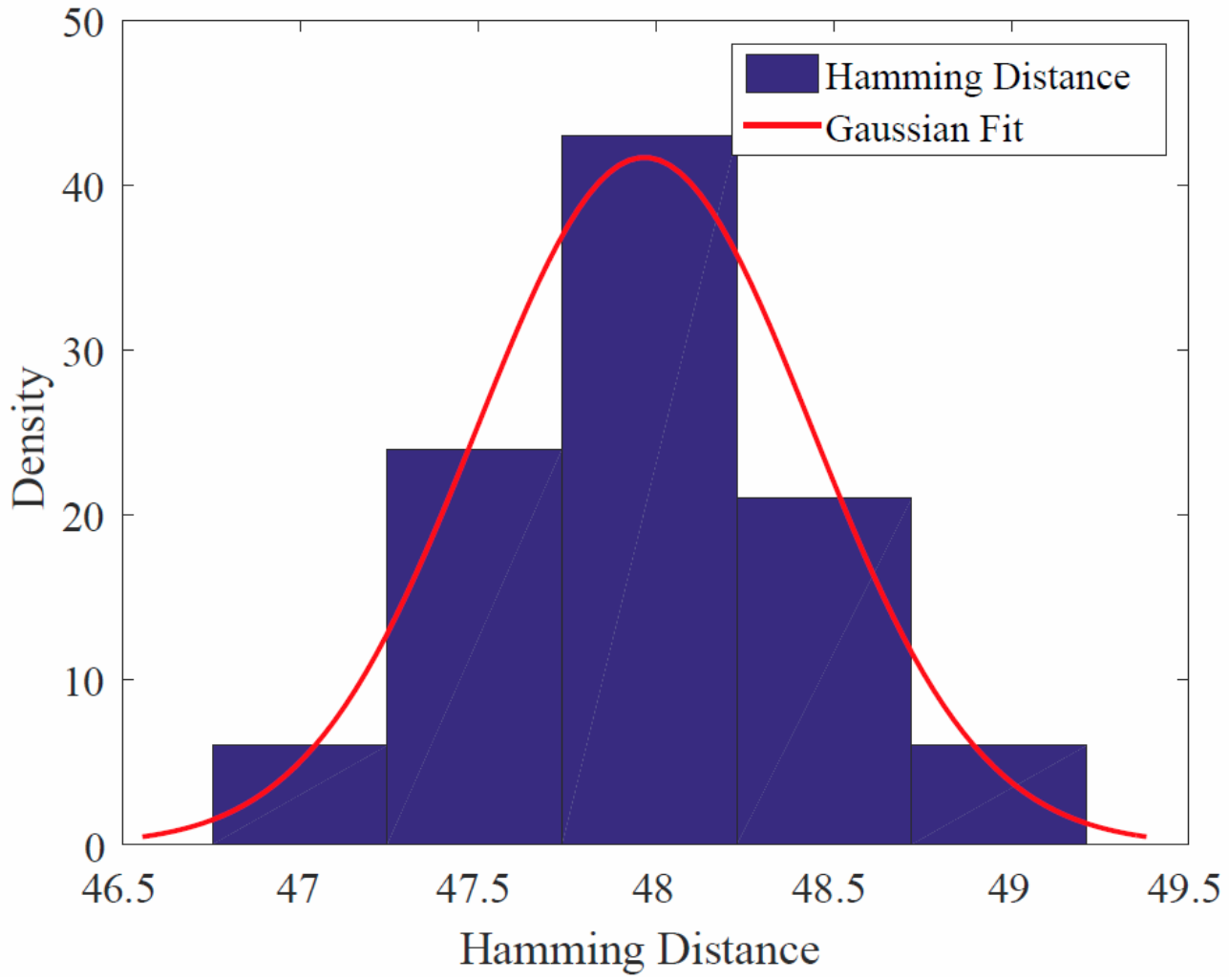
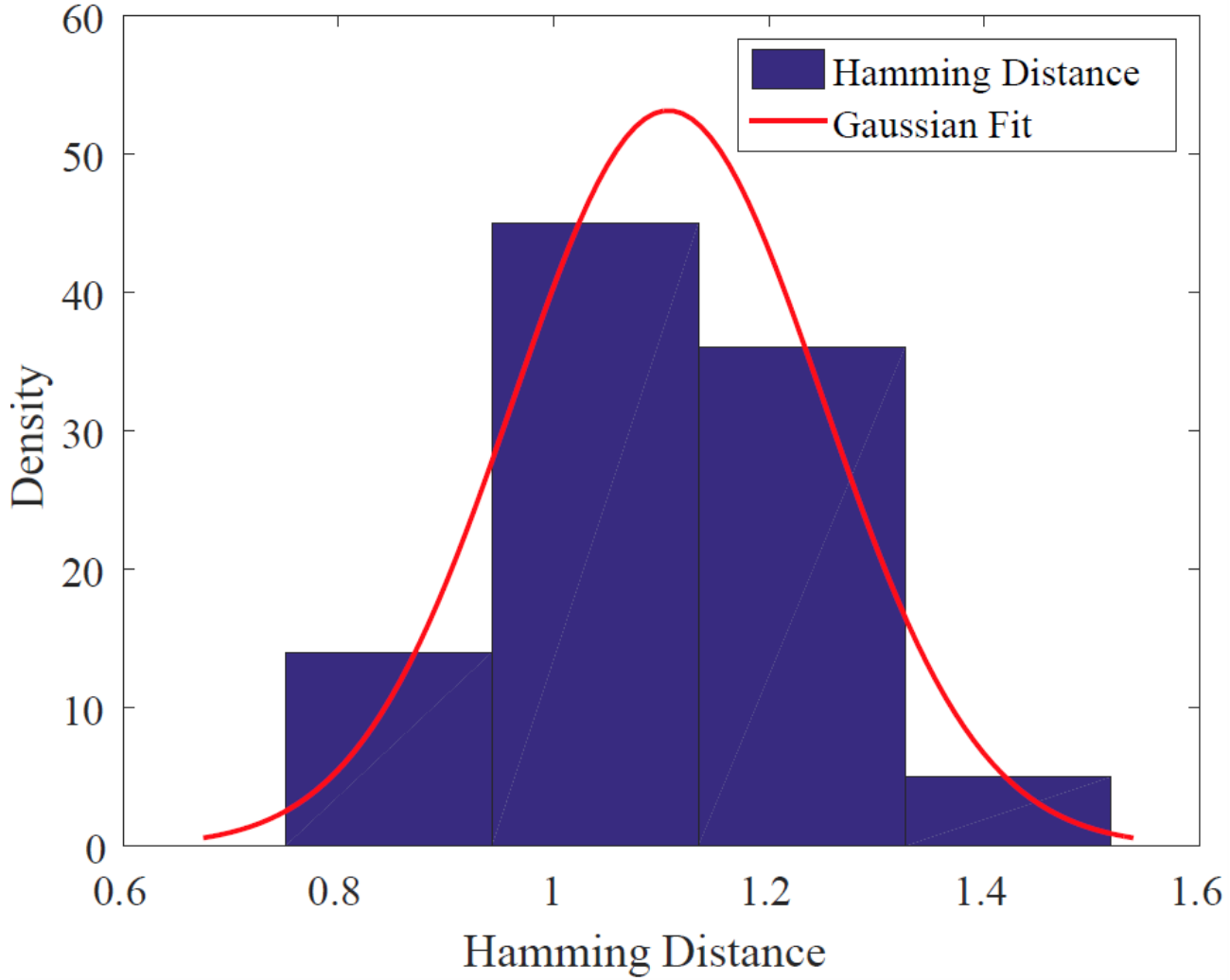
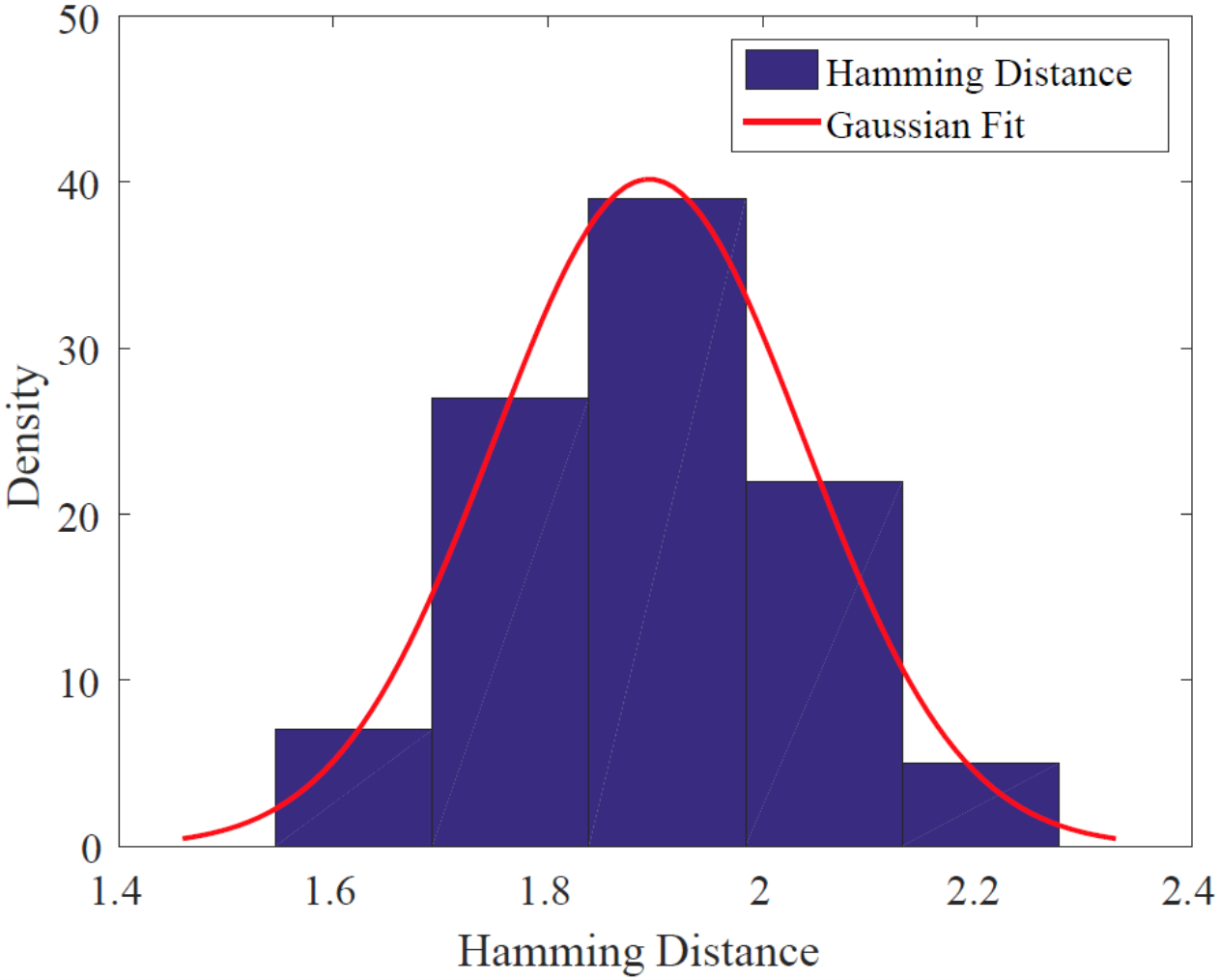


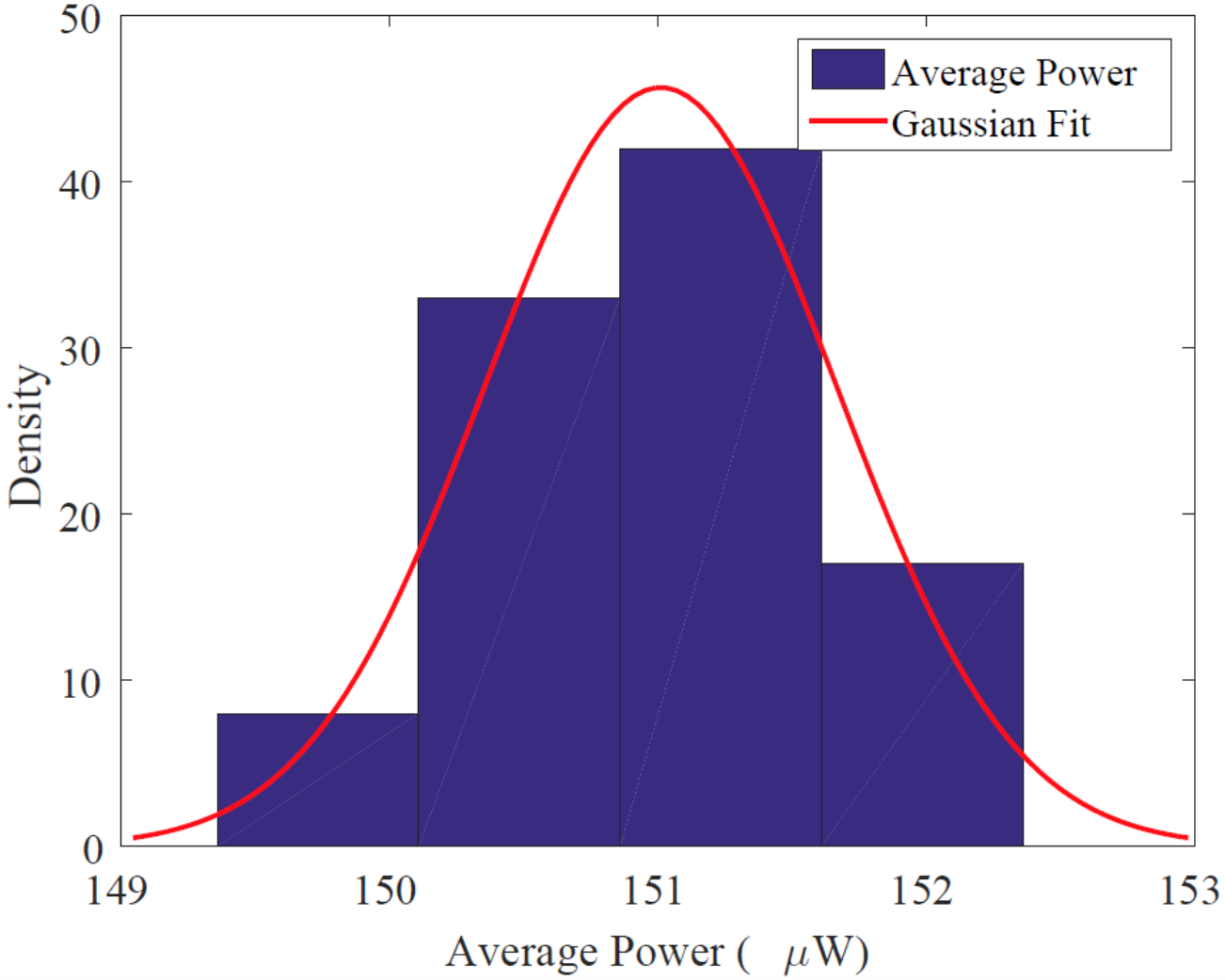
Intra PUF Hamming Distance of Speed Optimized Hybrid Oscillator Arbiter PUF



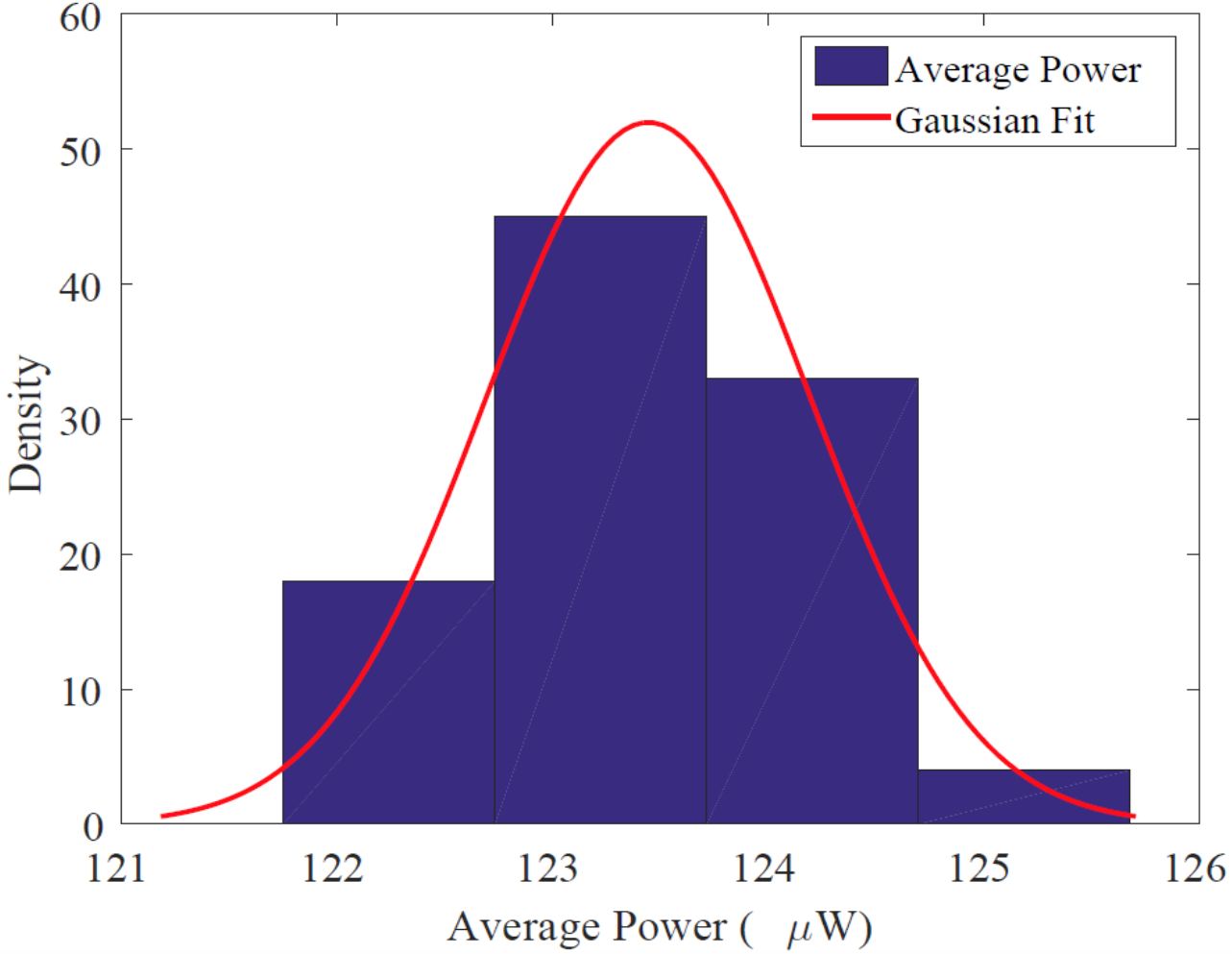
Intra PUF Hamming Distance of Power Optimized Hybrid Oscillator Arbiter PUF



Average Power of Speed Optimized Hybrid Oscillator Arbiter PUF



Average Power of Power Optimized Hybrid Oscillator Arbiter PUF



Characterization Table for PUF Designs

Power Optimized Hybrid Oscillator Arbiter PUF		
Parameter	FinFET	Dopingless Transistor
Average Power	175.5 μW	121.3 μW
Hamming Distance	50.1 %	48
Speed Optimized Hybrid Oscillator Arbiter PUF		
Average Power	251.5 μW	151 μW
Hamming Distance	48.3 %	50 %

Average Power of Speed Optimized Hybrid Oscillator Arbiter PUF

Research Works	Technology	Architecture Used	Average Power Consumed	Hamming Distance (%)
Rahman et al. [23]	90nm CMOS	--	--	50
Maiti et al. [19]	180nm CMOS	Traditional Ring Oscillator	--	50.72
Suh et al. [24]				46.15
Maiti et al. [18]				47.31
Yanambaka et al. (Power Optimized)[20]	32nm FinFET	Current Starved Oscillator	175.5 µW	50.1
Yanambaka et al. (Power Optimized)[10]	32nm FinFET	Traditional Ring Oscillator	285.5 µW	50.9
This paper (Power Optimized)	10 nm Dopingless FET	Hybrid Oscillator Arbiter	121.3 µW	48.0
This paper (Speed Optimized)	10nm Dopingless FET	Hybrid Oscillator Arbiter	151 µW	50.0

Conclusion and Future Research

- This paper presents two designs of hybrid oscillator arbiter PUFs, a speed optimized and a power optimized design using DL-FETs.
- A fair comparison of the two technologies, FinFET and DL-FETs is presented to show the power reduction using these transistors.
- As a future research, an ultra low power design of PUF can be implemented.

THANK YOU