Compact Modeling of Graphene Barristor for Digital Integrated Circuit Design

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Outline

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  - Properties of graphene
- ***Modeling Graphene Barristor***
  - Structure of barristor
  - Equivalent circuit of graphene barristor
- ***Graphene Barristor Based Circuit Design***
  - Modeling of graphene barristor
  - Evaluation of circuit design
- ***Conclusion***

Challenge of VLSI design

- In past decades, the increase in number of transistors follows the Moore's law (the number of transistors doubles approximately every two years).
- Transistor scaling makes more circuits in a single chip.
- Decreasing channel length leads chips to work at higher frequencies.
- Voltage scaling reduces power consumption of ICs significantly.

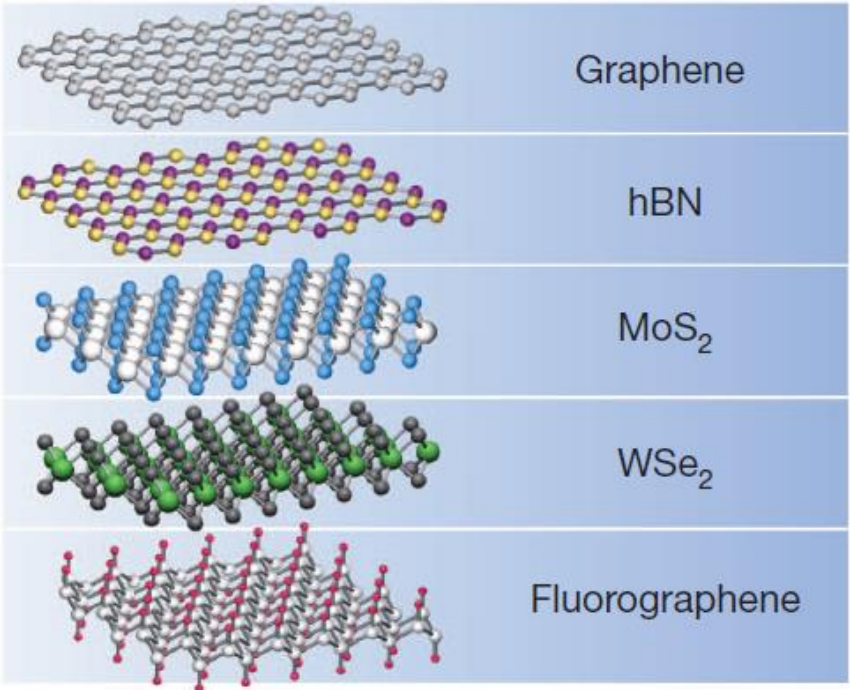
It seems ICs will keep up with Moore's Law in near future.

Challenge of VLSI design

However…

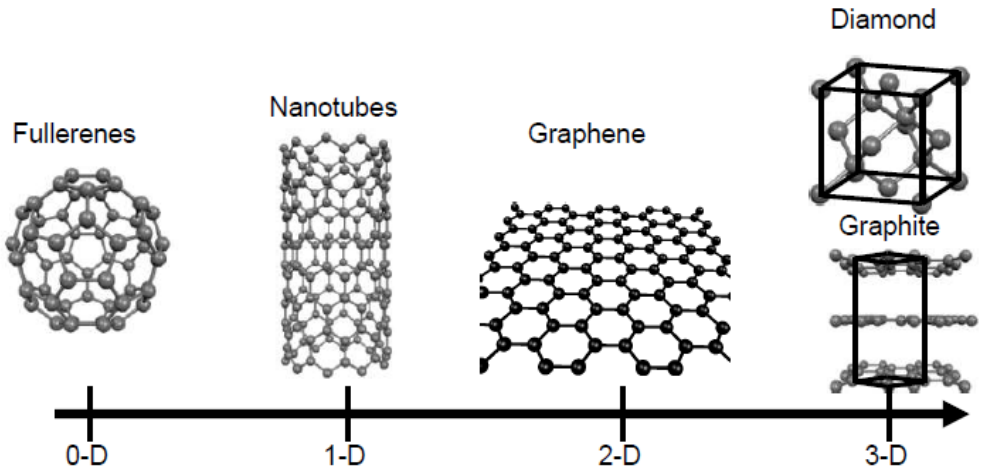
- High transistor density on a single chip challenges the robustness of VLSI design.
- Leakage current increases the static power consumption.
- A low supply voltage makes ICs more sensitive to the variation of threshold voltage.

Thus, emerging materials and devices which have high mobility and low power dissipation need to be researched.



Properties of graphene

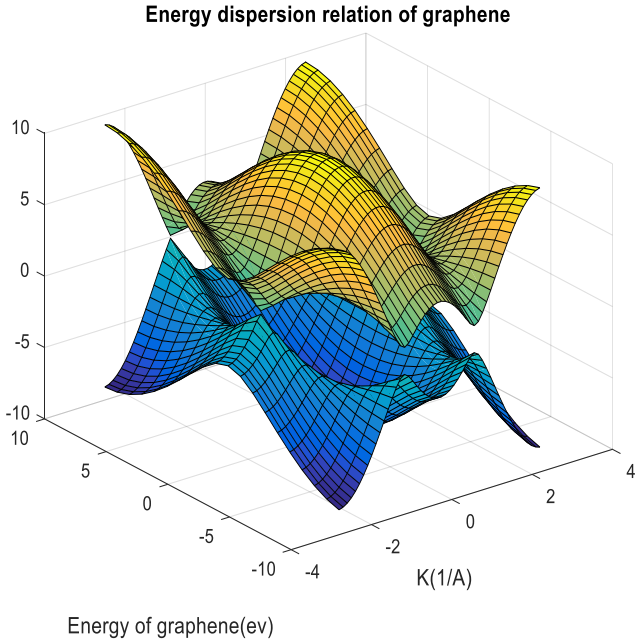
- Graphene is a two dimensional network of carbon atoms.
- It is the basic structure of other allotropes.
  - Fullerene
  - Carbon nanotube
  - Graphite



Properties of graphene

- Linear relationship between energy and momentum.
- Graphene has a high mobility which is nearly 100 times greater than that in silicon.
- Both electrons and holes can contribute to current in graphene transistors.

It is a prospective material in post-silicon era.



Properties of graphene

However…

- Graphene has zero bandgap and is semi-metal.
- The graphene-based FET has very low on/off current ratio with a large leakage current.
- Above two points make graphene-based FET be not suitable for digital VLSI.

In this work, we analyze and model a newly reported structure, called graphene barristor*, which based on Schottky barrier between the silicon and graphene. This barrier height can widen the bandgap and thus is used for digital VLSI design.

*[Yang H, Heo J, Park S, et al. Graphene barristor, a triode device with a gate-controlled Schottky barrier[J]. Science, 2012, 336(6085): 1140-1143.]

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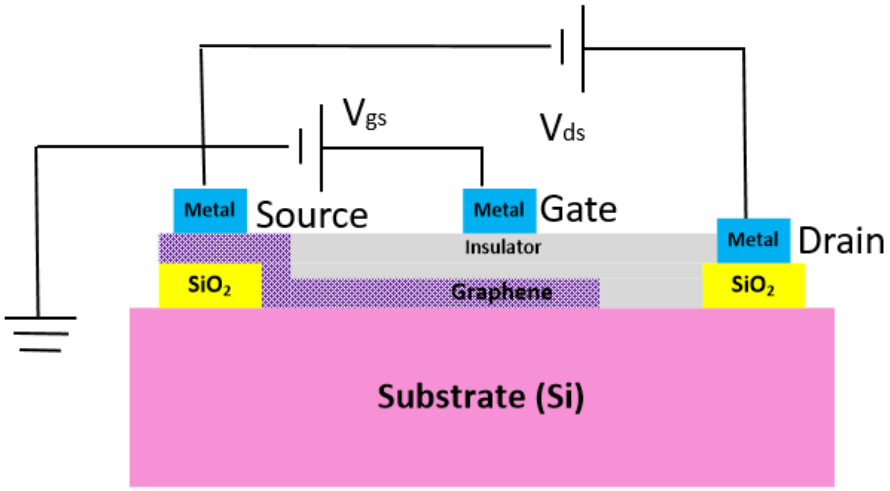
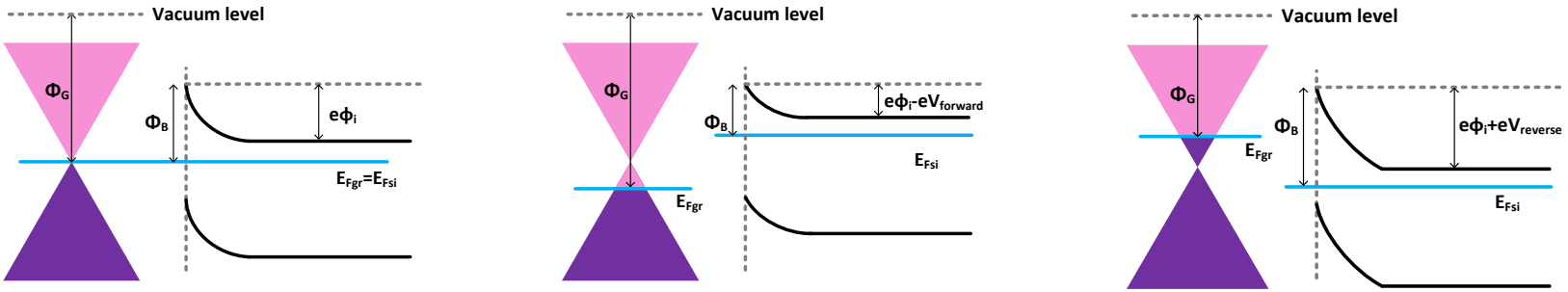
Structure of graphene barristor

- When graphene contacts the silicon, electrons transfer from silicon to graphene, and introduces a built-in potential.
- To achieve three-node device, a drain node is added to extend the diode to form a FET-like structure.
- Source node connects to ground or power according to the FET type.



Cross section view of graphene barristor.

Structure of graphene barristor

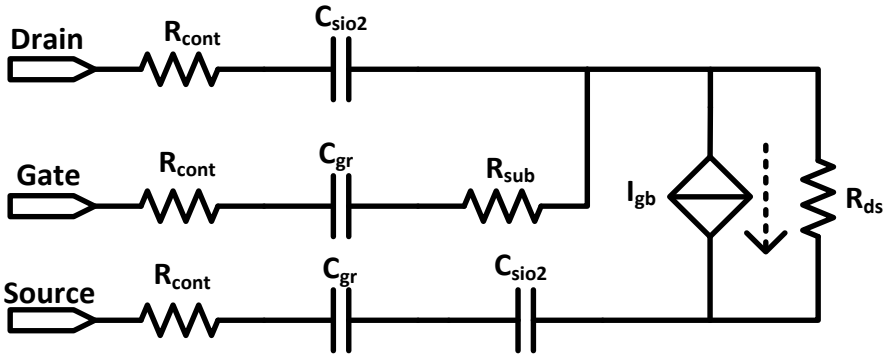


The energy band diagram of graphene/n-type silicon Schottky junction.

- (a) is under thermal equilibrium.
- (b) is under forward bias, the built-in potential will be reduced.
- (c) is under reverse bias, the built-in potential will be increased.

Equivalent circuit of graphene barristor

- The equivalent circuit can be divided into a controlled source and relative passive devices.
- Controlled source only describes the current-voltage behavior, and passive devices reflect the parasite effect in barristor.
- C_{gr} is the graphene capacitance, C_{sio2} is the oxide capacitance, R_{cont} is the contact resistance, R_{ds} is the output resistance, and R_{sub} is the substrate resistance.



Equivalent circuit of a graphene barristor.

Equivalent circuit of graphene barristor

- For the calculation of capacitor in a graphene barristor, the charge balance considering metal, silicon, and oxide silicon can be expressed by:

$$\begin{cases} Q_m + Q_{gr} + Q_{si} = 0 \\ Q_m = \dfrac{\varepsilon_m \left(V_g - V_{gr}\right)}{t_{ox}} \\ Q_{gr} = \dfrac{2q}{\pi}\left(\dfrac{kT}{\hbar v_f}\right)^2 \left[\zeta_1\left(-\dfrac{qV_{gr}}{kT}\right) - \zeta_1\left(\dfrac{qV_{gr}}{kT}\right)\right] \\ Q_{si} = \dfrac{\Phi_d}{|\Phi_d|}\sqrt{2\varepsilon_{si}kTN_d}\sqrt{\left[\exp\left(-\dfrac{q\Phi_d}{kT}\right) + \dfrac{q\Phi_d}{kT} - 1\right] + \dfrac{n_i^2}{N_d^2}\left[\exp\left(\dfrac{q\Phi_d}{kT}\right) - \dfrac{q\Phi_d}{kT} - 1\right]} \end{cases}$$

- Besides, to obtain the value of capacitor, it is obvious that in above equations, both Φ_d and V_{gr} are required to be obtained:

$$\Phi_d = \Phi_{bo} - V_{gr} + V_{ds} + \frac{kT}{q}\zeta_{1/2}^{-1}\left[\frac{N_d h^3}{2\left(2.16\pi m_o kT\right)^{3/2}}\right]$$

- Solving all these equations, we can get the graphene capacitances versus gate voltage.

Equivalent circuit of graphene barristor

- The current density can be obtained by:

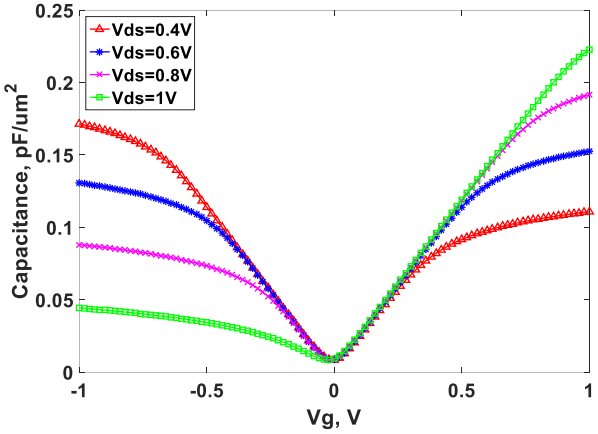
$$J = A^{*}T^{2}\exp\left(\frac{q\left(V_{gr}-\Phi_{bo}\right)}{kt}\right)\left[1-\exp\left(-\frac{qV_{ds}}{kt}\right)\right]$$

- The resistance of the substrate is described as follows:

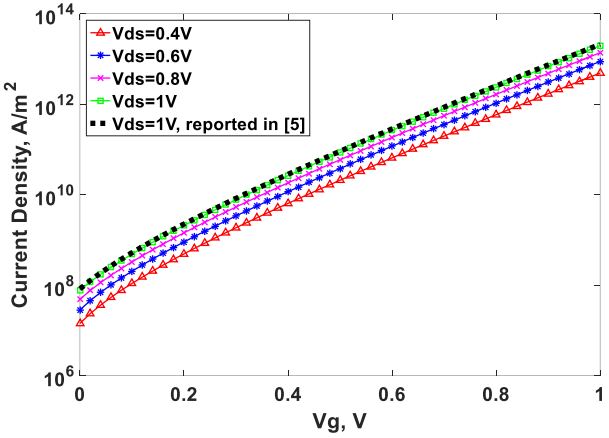
$$R_{sub} = \frac{2t_{sub}}{q\mu_{e}N_{d}A_{cont}}$$

- The contact resistance is set as 800Ω in our modeling.
- The output resistance between the drain and source can be obtained by the derivative of the current function with the drain voltage.

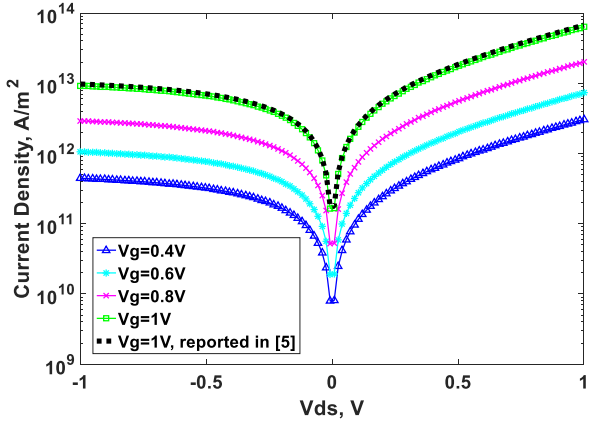
Equivalent circuit of graphene barristor



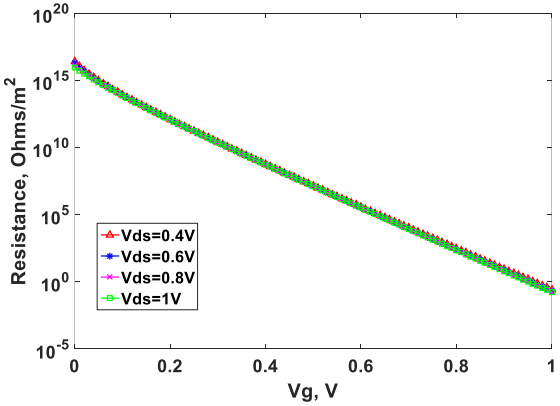
Graphene capacitor variation versus gate voltage.



Current density variation versus gate voltage.



Current density variation versus drain-source voltage.



Output resistance variation versus gate voltage.

Equivalent circuit of graphene barristor

- We use Φ_{b0} =0.5V, t_{ox}=1nm, T=300K, and N_d=$10^{22}m^{-3}$ to calculate each required value for our simulation and modeling.
- The transfer and output characteristics is simulated. The on/off current ratio is closed to 10^5 which is safe to digital VLSI design.
- The output resistance of graphene barristor is not sensitive to the drain-source voltage. This fact is due to the modulation by the potential of the silicon layer and the potential of the graphene layer.
- The current simulation is highly matched to the previous work regarding the graphene barristor fabrication.

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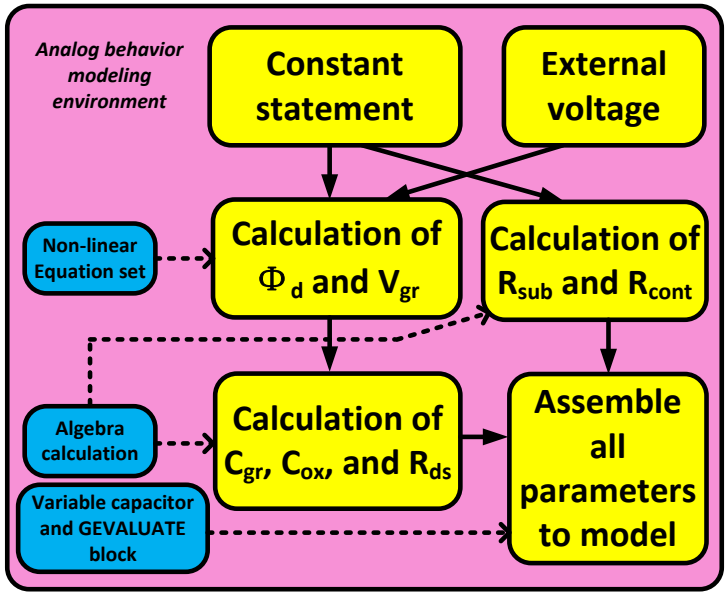
Modeling of graphene barristor

- Above analysis is based on the theoretical equation, but it cannot be directly used in circuit level simulation.
- There are several modeling methods which can simulate the emerging devices and their circuits.
  - Simple controlled source (e.g. VCCS, CCCS, VCVS, and CCVS)
  - Verilog-A
  - Lookup table (LUT).
- In this work, we use analog behavior modeling (ABM) in *PSPICE* to model the graphene barristor.
  - This method can dynamically adjust each current and voltage in the device according to the variation of voltages.
  - The passive devices can be adaptively changed due to voltage/current variation and so increase the simulation accuracy.
  - The device modeling using block diagram is more intuitive than that using coding method.

Modeling of graphene barristor



Modeling flow of a graphene barristor.

- The modeling flow of graphene barristor is shown as below:

1) State all constants globally.

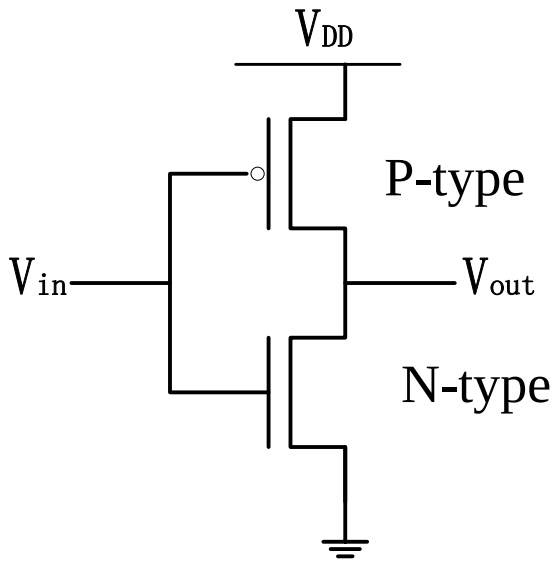
2) Calculate the potentials of silicon surface and graphene surface.

3) Using stated constants and the results from step 2, calculate all capacitances and device current. Then, using constants to calculate substrate and contact resistances.

4) Combine all calculated parameters in step 3 to form the final device model.

Evaluation of circuit design

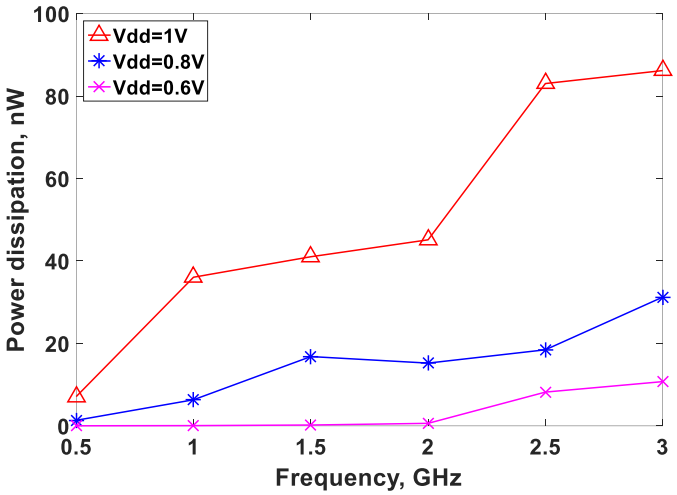
- The proposed modeling method can build both n-type and p-type graphene barristor.
- In our modeling, the length is 20nm, width is 1μm, the thickness of the silicon oxide and the substrate are 1nm and 0.3 mm, respectively.
- To evaluate the performance of digital circuit, an inverter is designed using the proposed model.



Graphene barristor based inverter.

Evaluation of circuit design

- The current under reverse bias is smaller than under the forward bias. The signal integrity in reverse bias condition is much worse than in forward bias condition. Thus, the forward bias is more suitable for the digital logic design.
- The logic design using graphene barristors is same as in traditional CMOS and FinFET, which has both pull-down n-type tree and pull-up p-type tree combined to obtain a complementary topology.
- The voltage applied to the graphene barristor based circuits can be lowered to 0.6V.



Graphene barrister based inverter performance: power dissipation dependence on frequency.

Evaluation of circuit design

Comparison between graphene barristor and emerging devices.

	FinFET			Bilayer Graphene FET	This work		
	By the Year				By the Supplied Voltage		
	2019	2024	2027		1V	0.8V	0.6V
t_{ox} (nm)	0.9	0.8	0.8	N/A	1	1	1
L_{ch} (nm)	12	8	6	40	20	20	20
V_{dd} (V)	0.7	0.5	0.45	0.2	1	0.8	0.6
I_{on}/I_{off}	5.5×10^{7}	2×10^{7}	8.5×10^{6}	2.91×10^{3}	0.94×10^{5}	0.93×10^{5}	0.92×10^{5}
C_g (fF)	1.47	1.24	1.24	0.32	1.12	1.07	1.06
E_{switch} (fJ)	1.89	0.94	0.63	0.013	1.1	0.607	0.52

Conclusion

- In this work, the compact current transport model with passive devices of the graphene barristor is presented.
- Using analog behavior modeling, an accurate SPICE model is proposed. The proposed model can be adjusted dynamically by the voltage variation used for circuit simulations.
- Both inverter simulation and device comparison prove that the graphene barristor is a competitive candidate for low power digital VLSI design.

Thank you