Graphene Nanoribbon Field Effect Transistor based Ultra-Low Energy SRAM Design

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Outline of the talk

- Introduction and Motivation
- Static Random Access Memory
- GNR-FET Transistors
- Novel Contribution
- SB-Type GNR-FET
- SRAM Test Bench Configuration
- Results

Introduction and Motivation

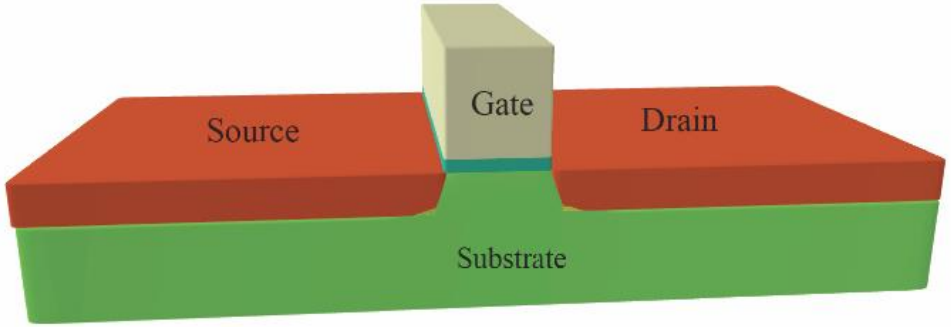
- Requirements of Digital Embedded Systems :
  - Low power/energy.
  - Small form factor.
  - High performance.
- Besides these, every embedded system has a memory.

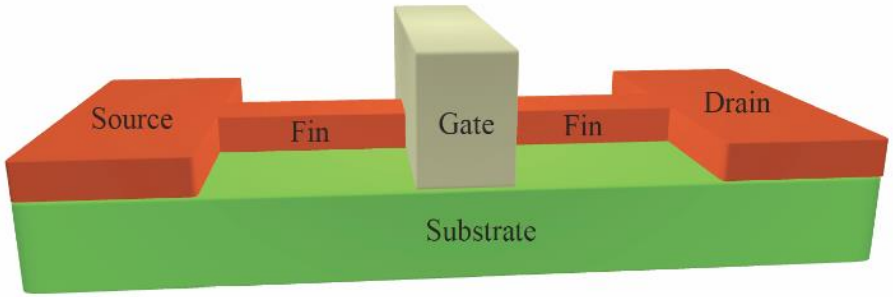
Introduction and Motivation

- Memory in a modern SoC occupies 95% of chip area.
- Memory also is one of the major power hungry component on SoC.
- Higher system performance means increased memory.
- This is a challenging task for future nanoelectronics.

Transistors and Issues

- Scalability of the devices.
- Sub 22nm regimes CMOS increases leakage, temperature dissipation, etc.,
- FinFETs already reached 10nm and 8-Billion on a single chip.



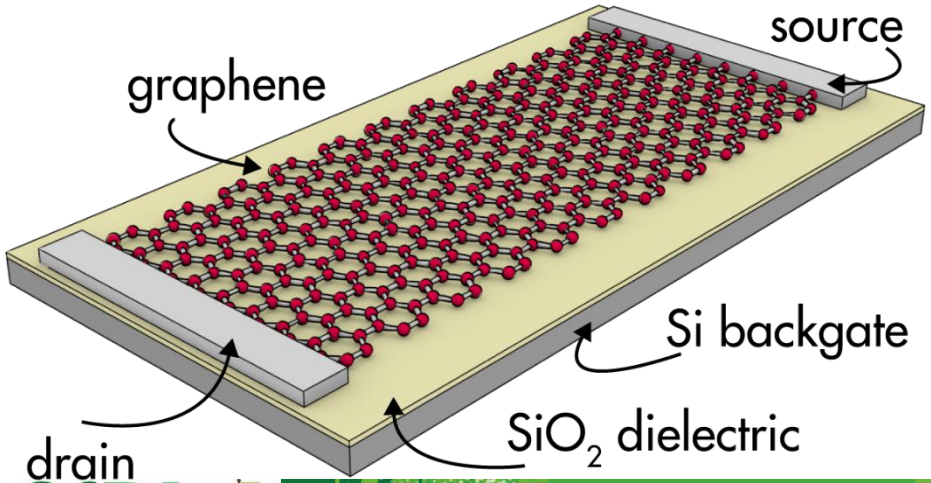


Static Random Access Memory

- SRAM is the widely used Random Access Memory.
- SRAM does not need a burst of power every few milliseconds like DRAM.
- Power, density and performance needs to be carefully optimized while designing.
- Device scalability is much helpful in SRAM design.

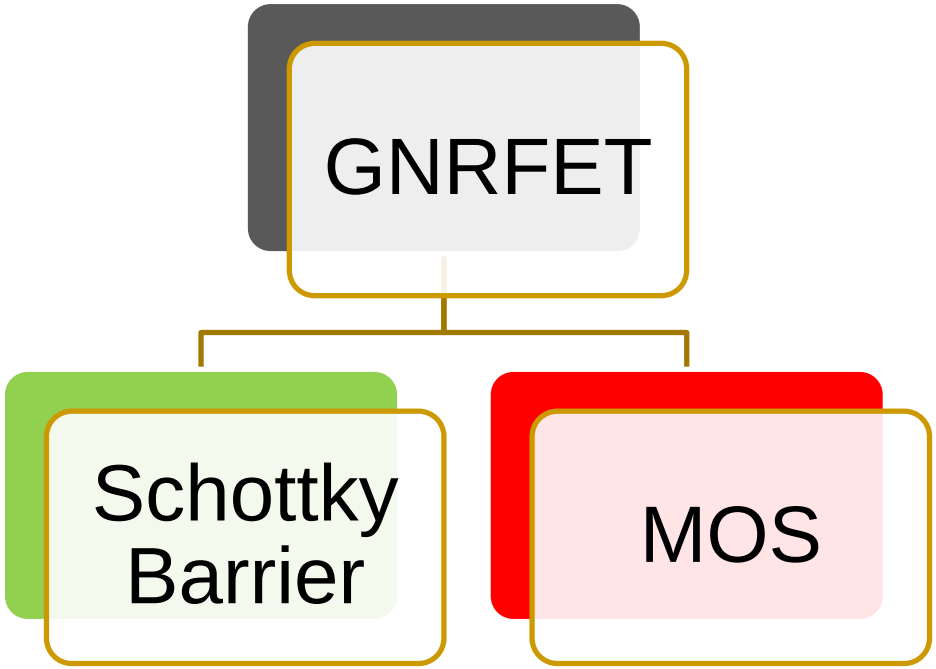
Graphene Nano Ribbon Transistors

- High strength
- Highly conducting material
- Zero band gap allowing for analog applications
- Very difficult to turn-off
- Less applications in Digital



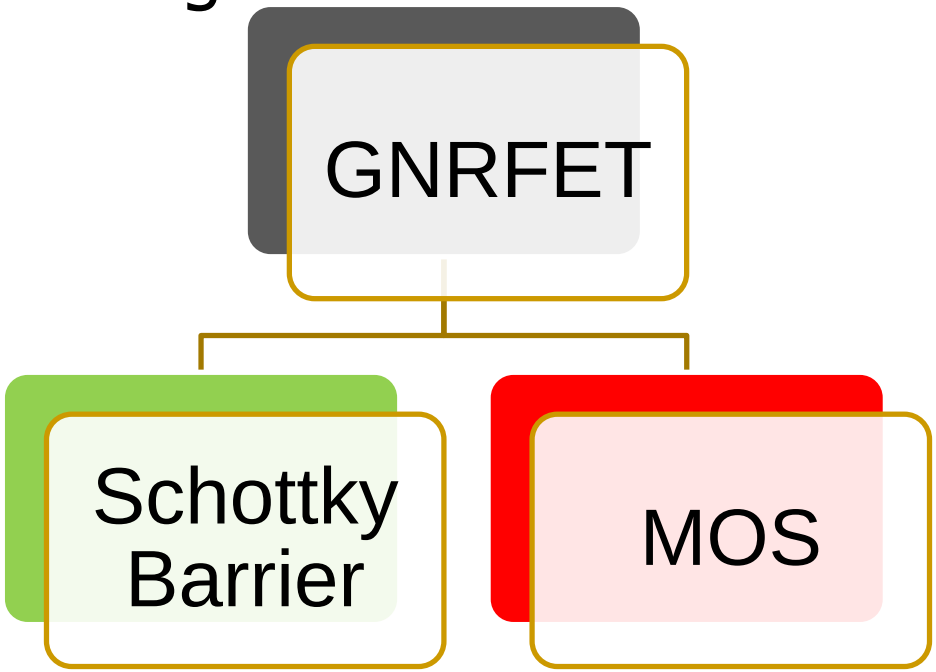
Graphene Nano Ribbon Transistors

- MOS type is much better than Schottky Barrier.
- MOS type GNRFET has larger on-off ratio making it better for digital applications.
- Much larger on current in MOS type.
- Very less delay.
- Large transconductance.



Graphene Nano Ribbon Transistors

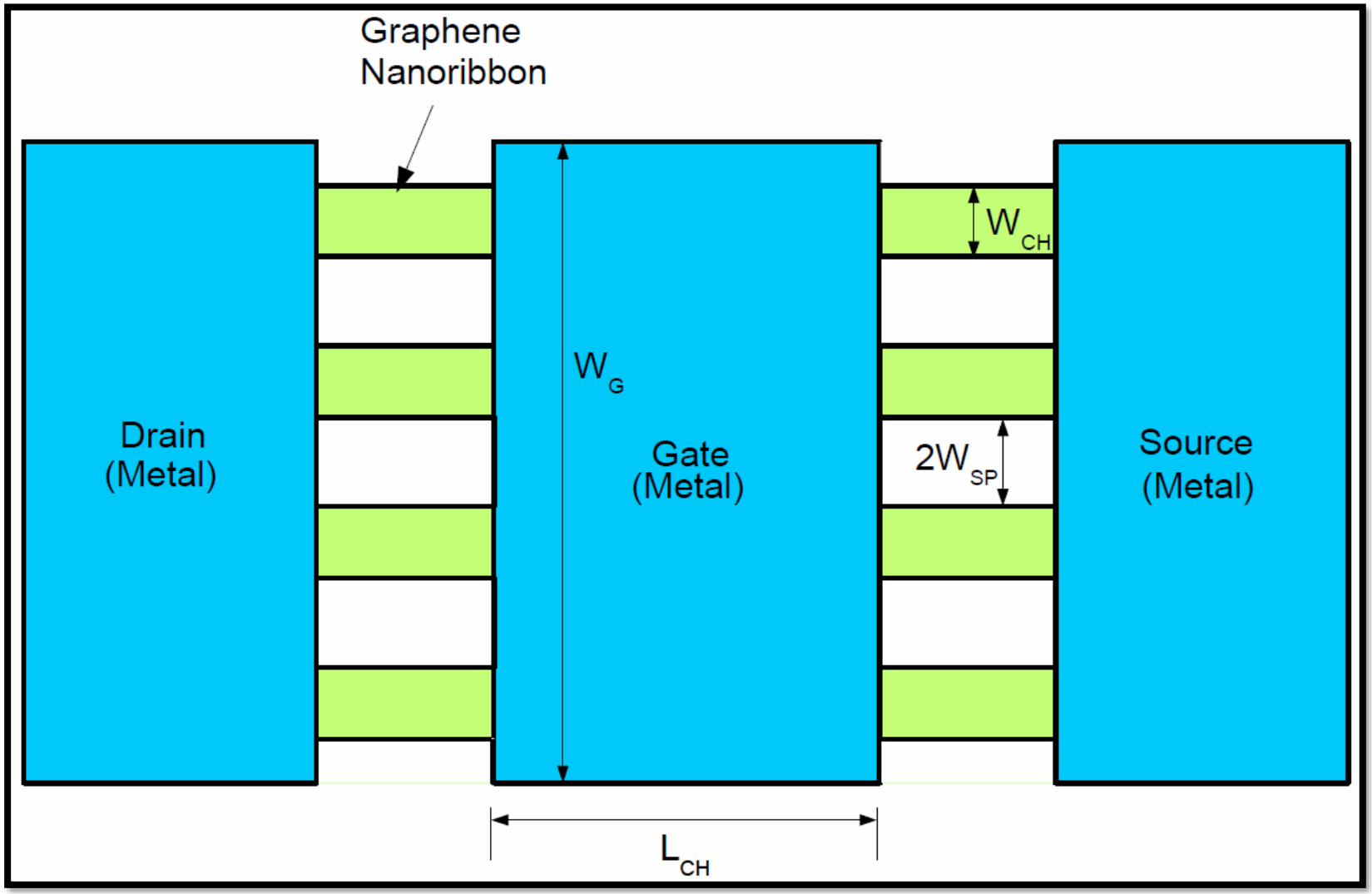
- Schottky Barrier Graphene Nanoribbon Transistors need no doping.
- Less difficulty in manufacturing.
- No doping – Less variability.



Novel Contributions

- Comparison of GNRFET SRAM with Silicon based SRAM.
- A detailed comparison is provided which is first time presented in this paper.

SB-type GNRFET



SB-type GNRFET

- Increasing number of nanoribbons increases drive current strength.
- Band gap in GNRFET is inversely proportional to Graphene Nanoribbon width.
- Hence if width is increased beyond 10nm, GNR properties revert to graphene sheet.
- In current work, GNRFET is incorporated in SRAM so width is less than 10nm.

Parameters of GNRFET

Device Parameter	Default Values
Physical channel length	10 nm
Substrate oxide thickness	20 nm
Tog-gate dielectric material thickness	0.95 nm
Spacing between adjacent GNRs	2.0 nm
Number of GNRs	6-10
Number of dimer lines in GNR lattice	12
Edge roughness percentage	0 (Ideal)

6T SRAM Configuration

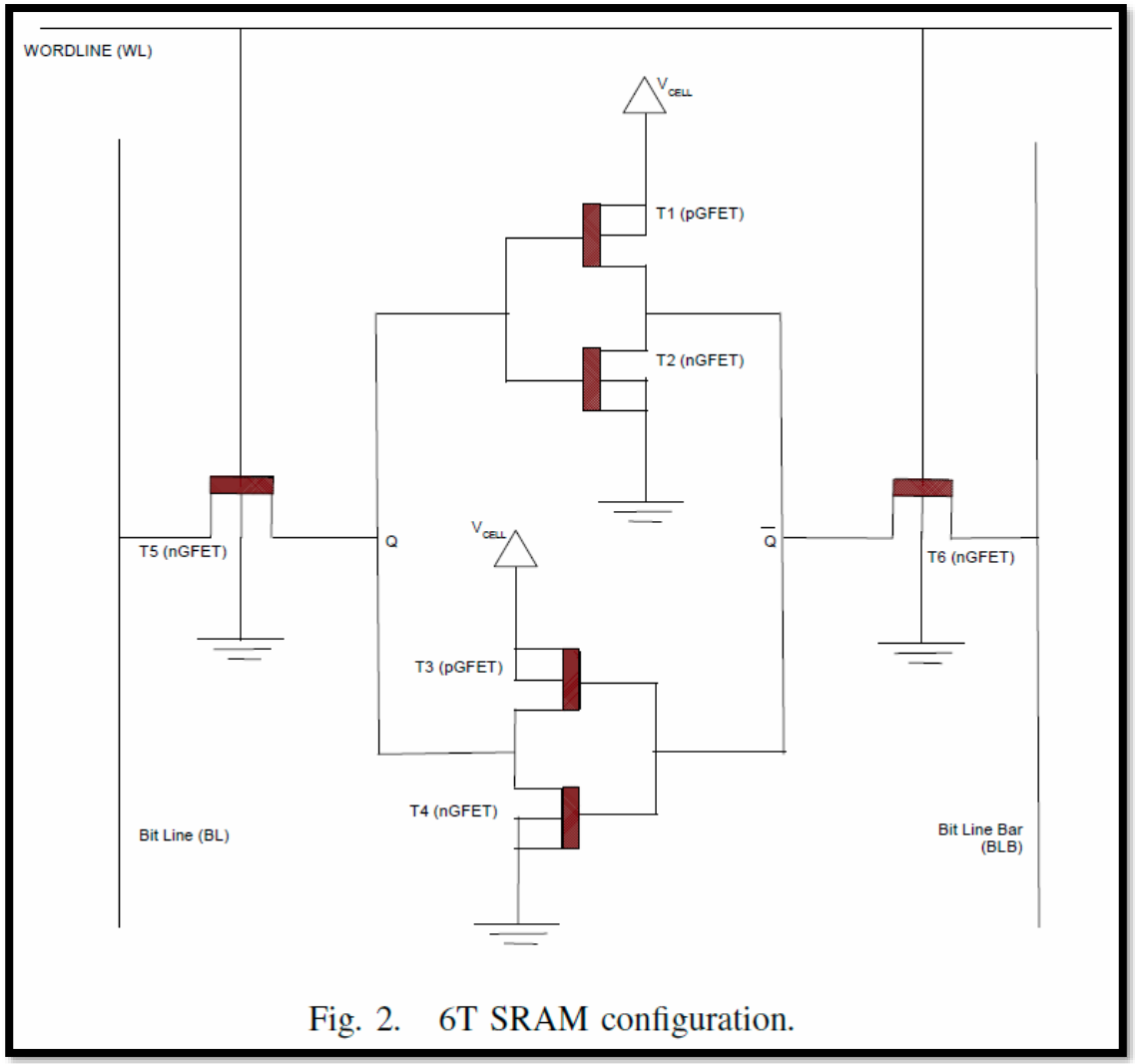
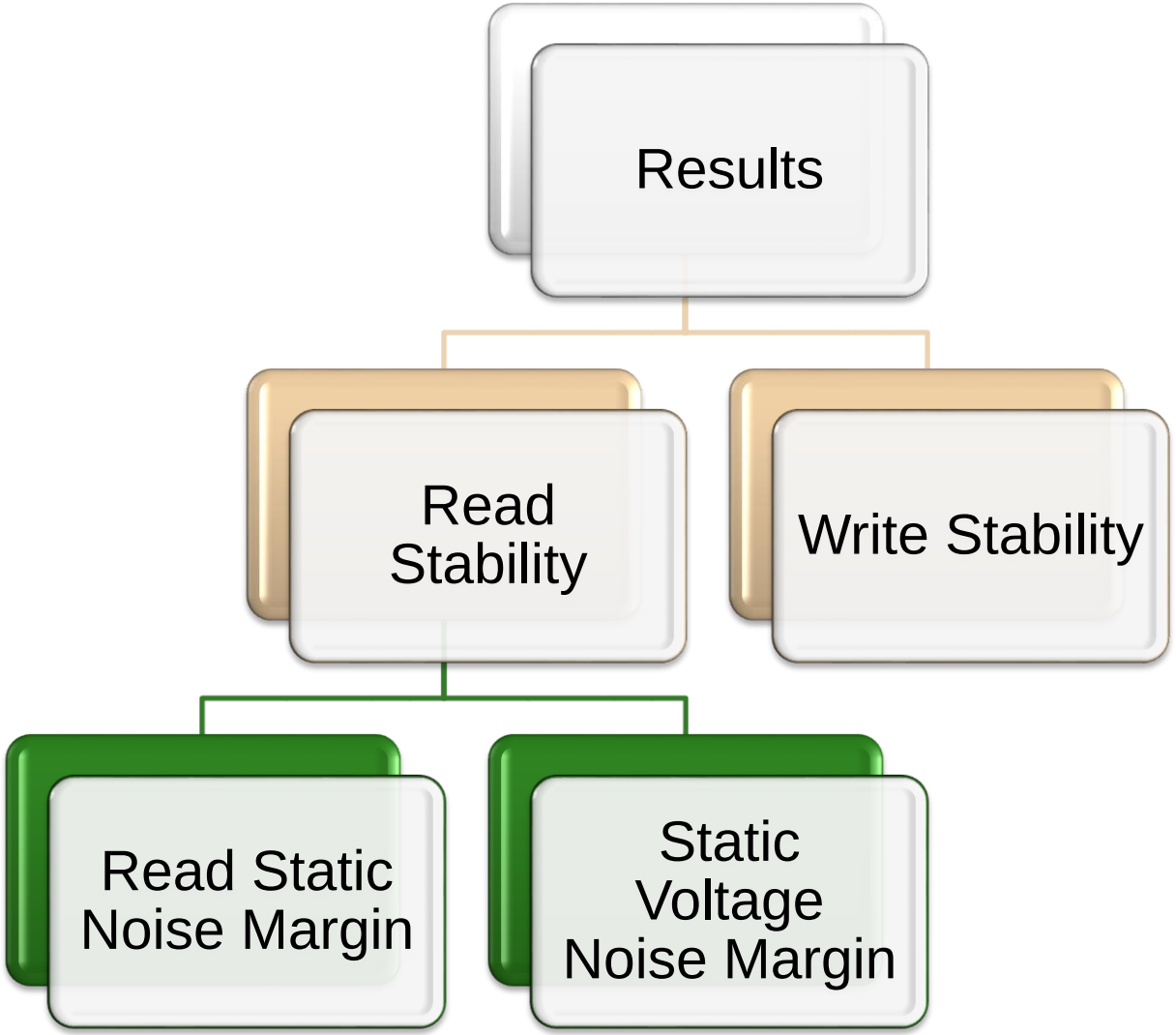


Fig. 2. 6T SRAM configuration.

Results


Results
Read Stability
Write Stability
Read Static Noise Margin
Static Voltage Noise Margin

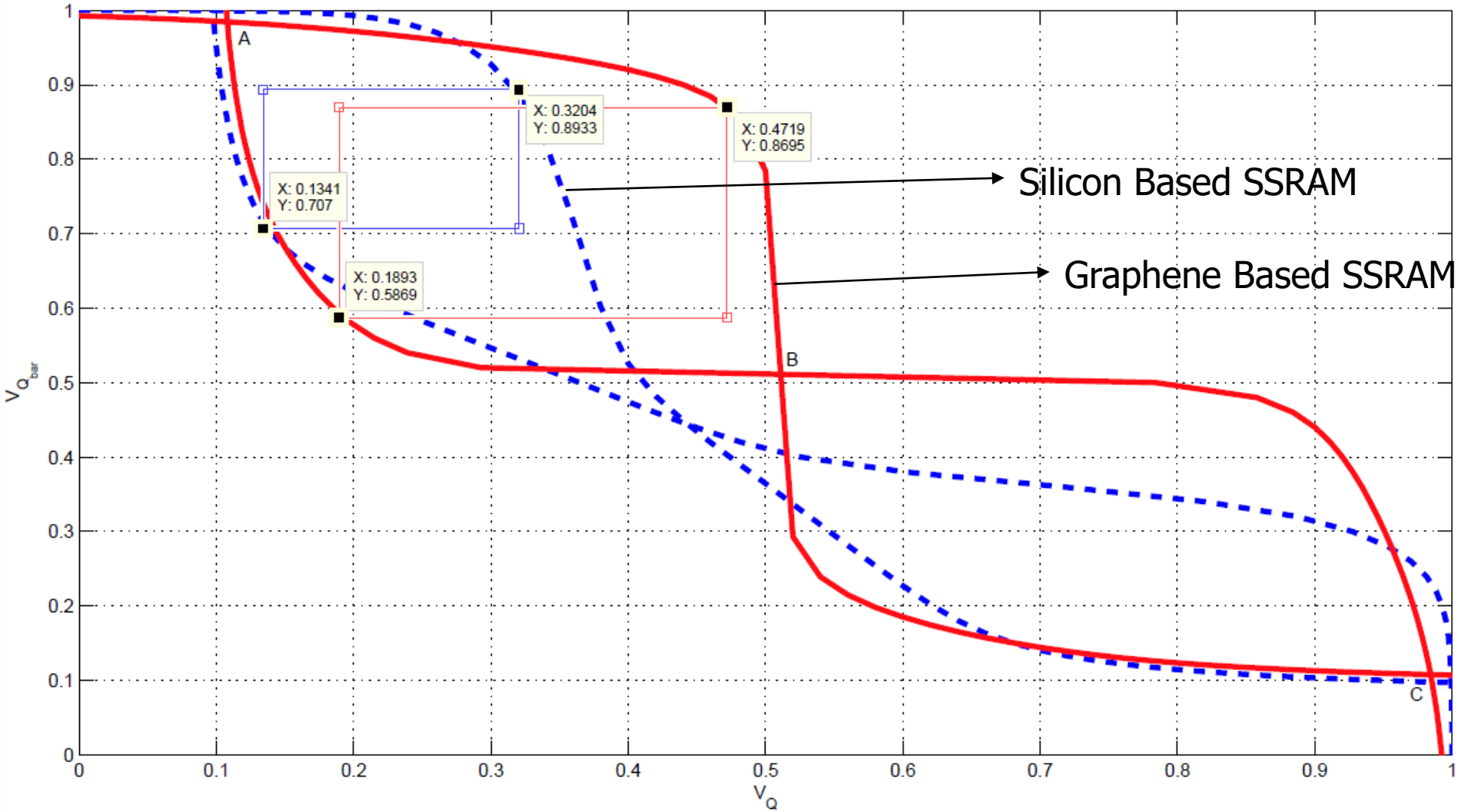
Read Stability

- SRAM becomes less stable with scaling due to low supply power.
- Considering Q is holding 0.
- During read, Q rises above 0V to a voltage determined by T_5 and T_4.
- Voltage at which memory cell flips its stored state is called Cell Trip Point.
- If voltage at Q > trip point, cell flips its state (read upset).

Read Static Noise Margin (RSNM)

- Extracted from Read Voltage Transfer Characteristics.
- Used to quantify Read Stability of the SRAM.
- RSNM represents the maximum voltage tolerated before read upset.
- Butterfly curve is obtained by sweeping nodes Q, $\bar{Q}$.
- Side length of biggest square that fits in butterfly curve is RSNM

Butterfly Curve



SVNM and SINM

- N – Curve can also be used to measure the stability of an SRAM.
- Voltage at storage node $Q\ or\ \bar{Q}$ is swept keeping Word Line and Bit Lines biased at VDD and measuring external current sourced at $Q\ or\ \bar{Q}$.
- Three zero crossings A, B and C are obtained.

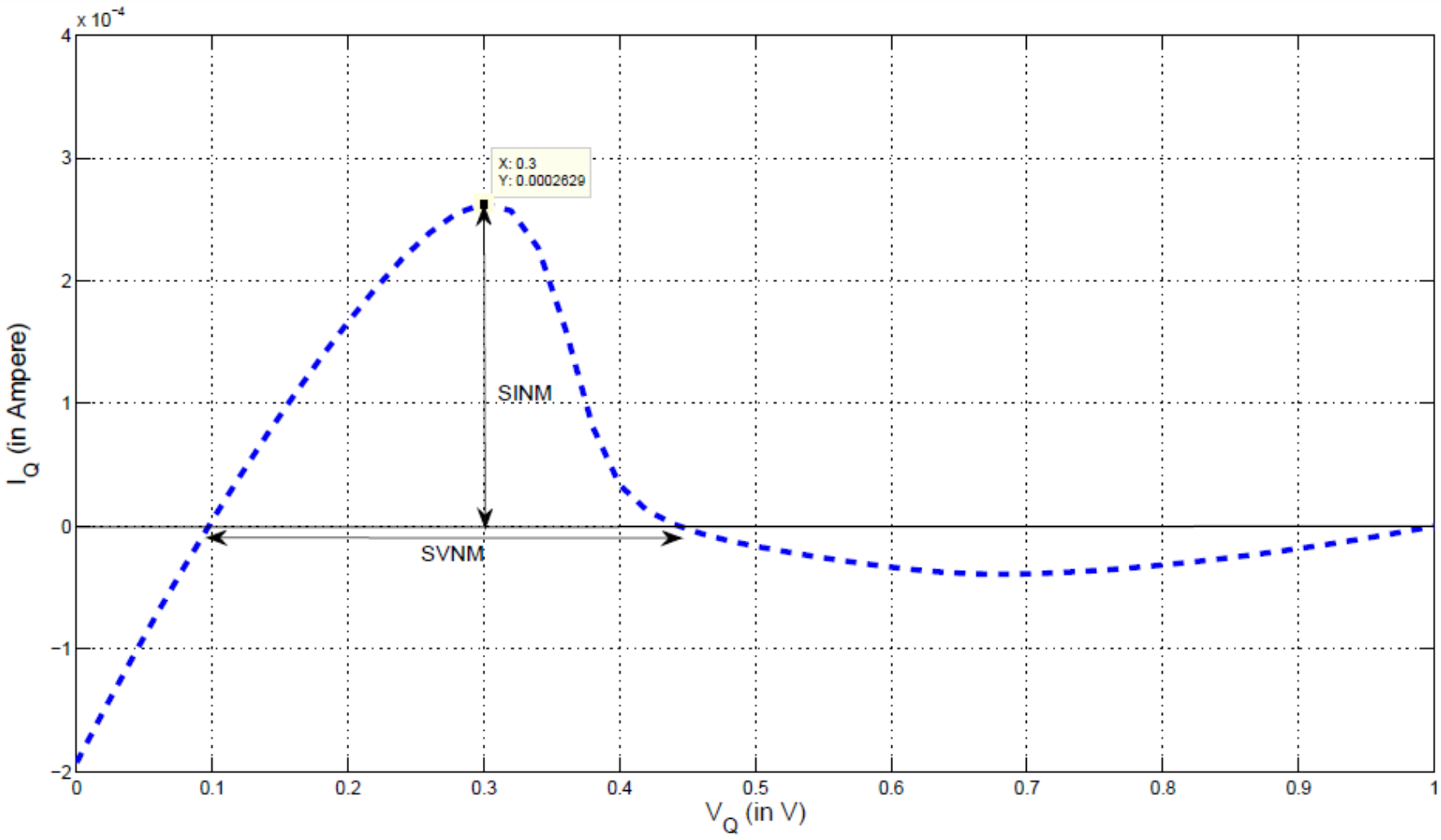
SVNM and SINM

- A – determined by cell ratio.
- B – determined by pull-up and pull-down ratio.
- C – determined by aspect ratio of pull-down and access transistors.
- Voltage difference between A and B indicates maximum tolerable DC Voltage before changing content which is Static Voltage Noise Margin (SVNM).

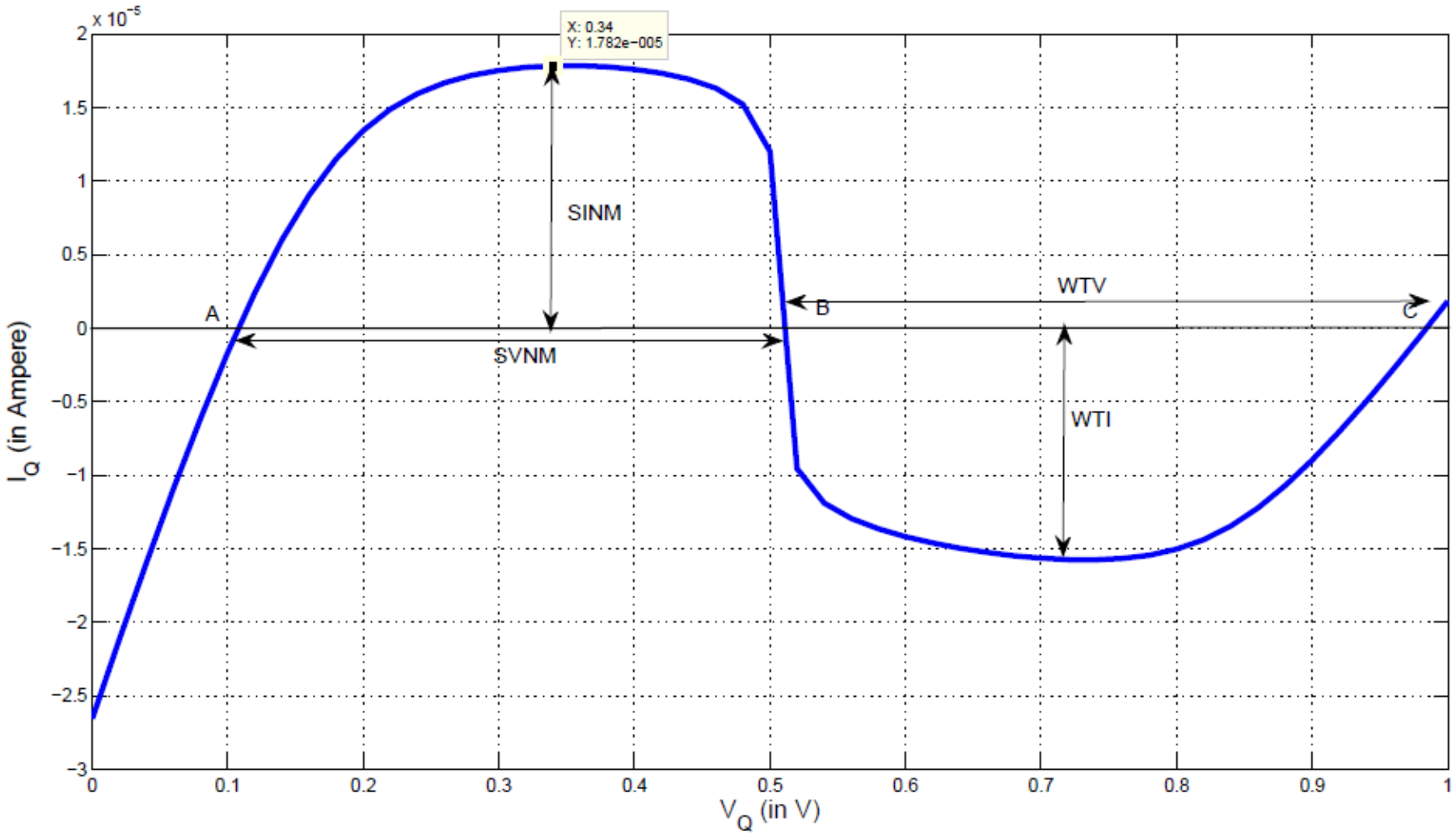
SVNM and SINM

- Current difference between A and B indicates maximum tolerable DC Current before changing content which is Static Current Noise Margin (SINM).
- SVNM and SINM together can give read stability of an SRAM.
- In Graphene based SRAM, SVNM is 400 mV while in Silicon based SRAM is 340 mV.
- But SINM is greater in Silicon based SRAM than Graphene.

Static Current Noise Margin (Silicon)



Static Current Noise Margin (Graphene)



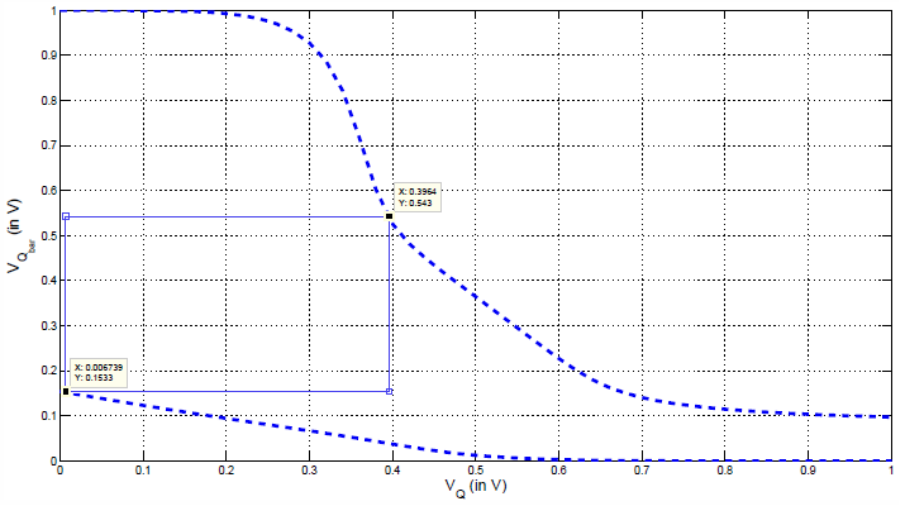
Write Ability

- Write Trip Point – Maximum voltage required at bit line to flip content in the cell.
- Considering 0 at Q.
- If T_5 and T_1 pull voltage at $\bar{Q}$ below trip point, successful write can be performed.
- So Write Noise Margin (WNM) can be extracted from write VTC and read VTC.

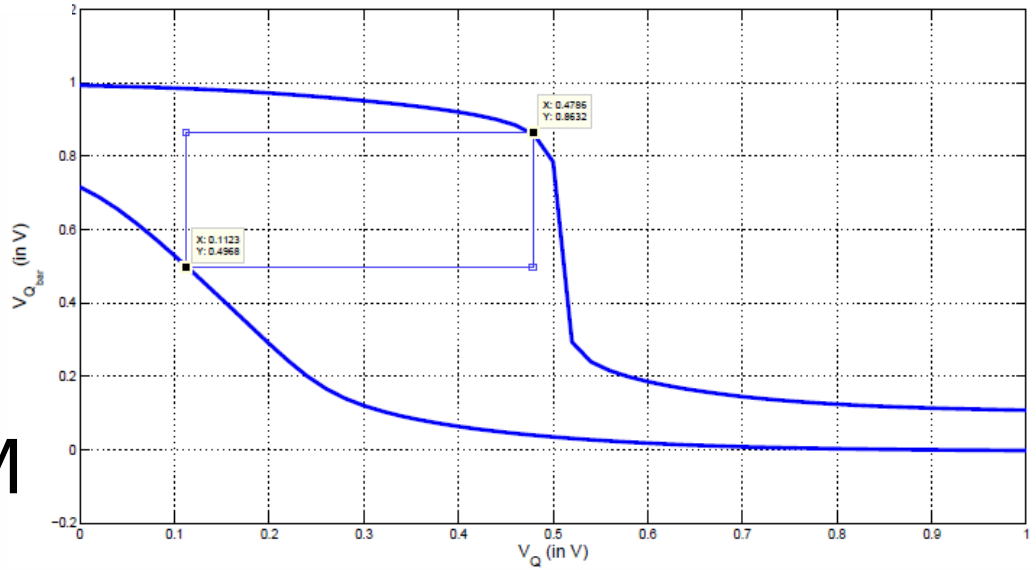
Write Ability

- Write VTC can be measured by sweeping Q with BL and WL at V_{dd}, BLB at 0 and monitoring voltage at Q.
- If Write VTC and Read VTC intersect with each other, cell is not able to write properly.
- Write ability can also be characterized using an N – curve.

Write Noise Margin



Silicon Based SSRAM

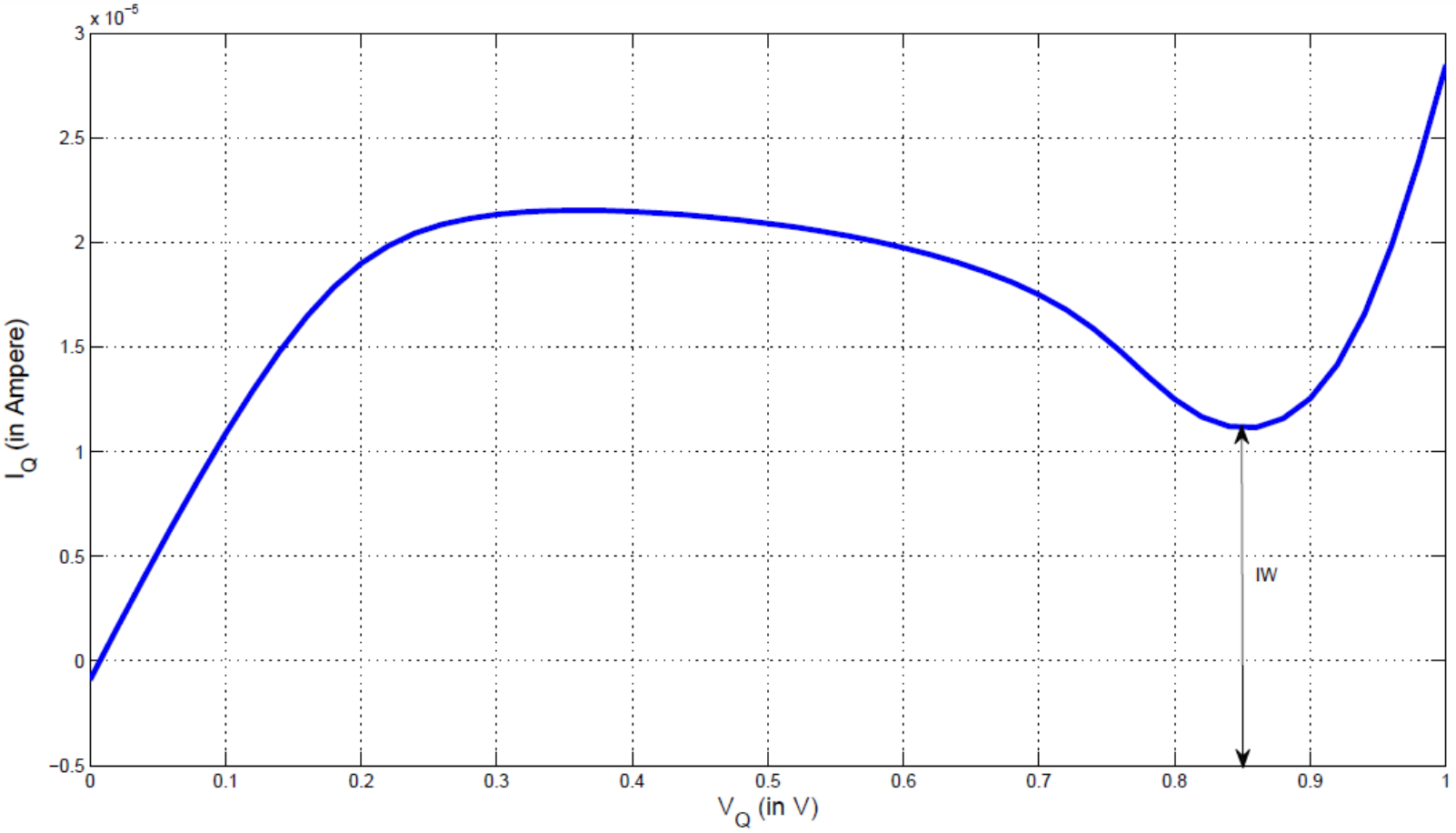


Graphene Based SSRAM

Write Ability

- Write ability of SRAM can also be measured using the N – Curve.
- Measured by sweeping storage nodes while WL and BL are at V_{dd} and BLB at ground and measure current at storage nodes.
- If Write Current < 0, it means Write failure.

Writeability Current Calculation



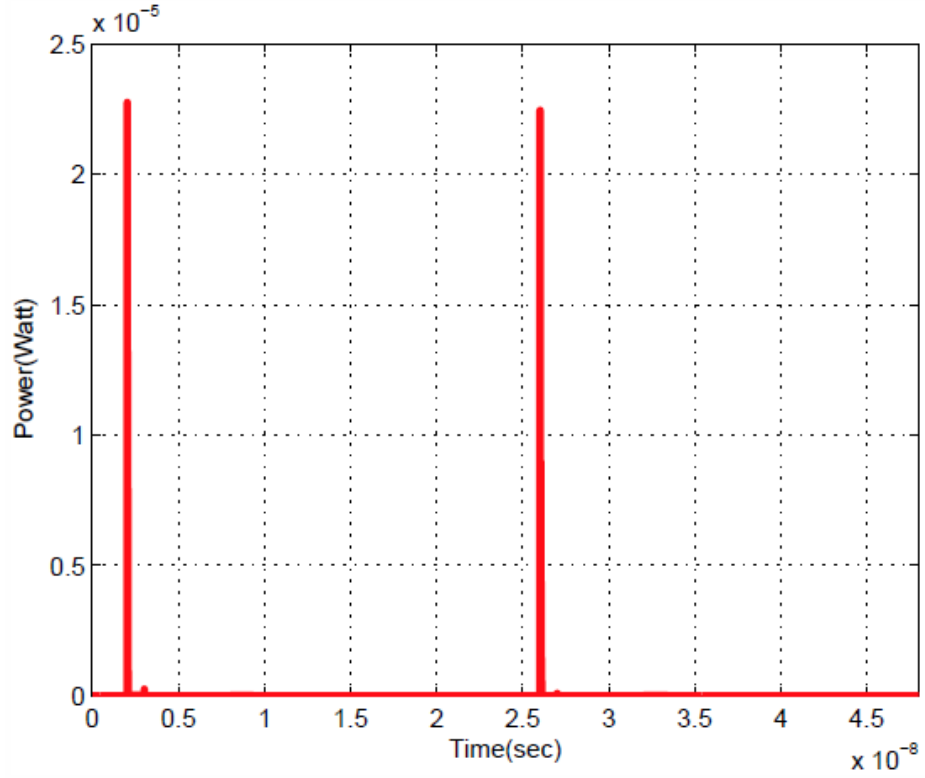
(a) Graphene based SRAM

Stability Comparison

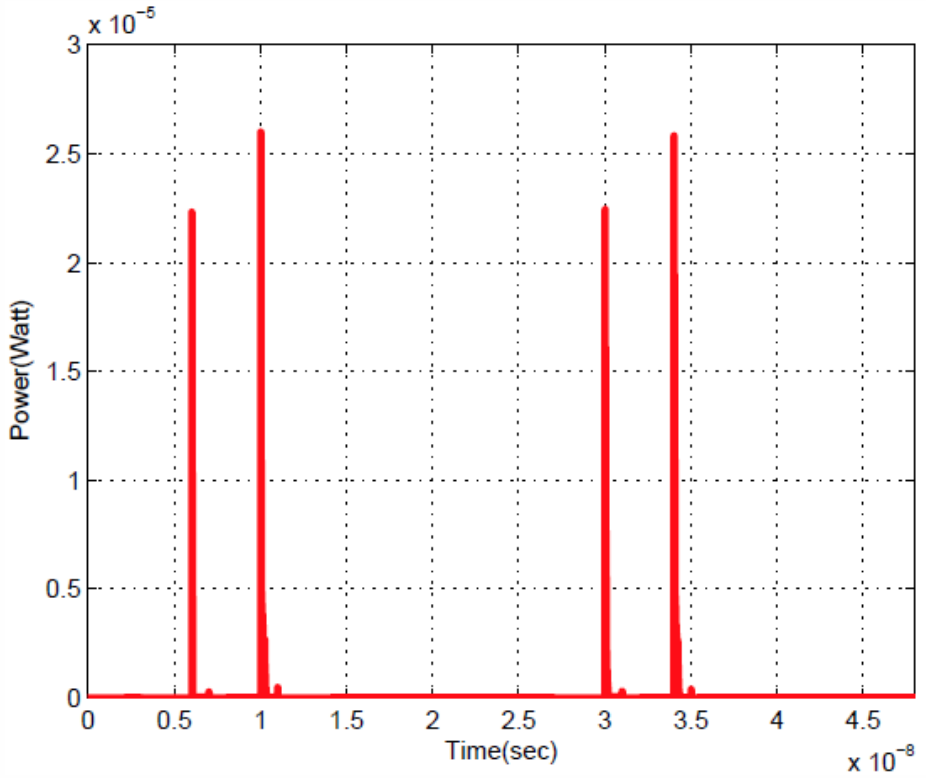
CELL STABILITY COMPARISON

Description	GFET Based SRAM	Silicon FET Based SRAM
RSNM	282.6 mV	186.3 mV
WNM	366.4 mV	389.7 mV
SVNM	400 mV	340 mV
SINM	17.82 μA	262.9 μA
WTV	470 mV	430 mV
WTI	-16 μA	-40 μA

Power Consumption

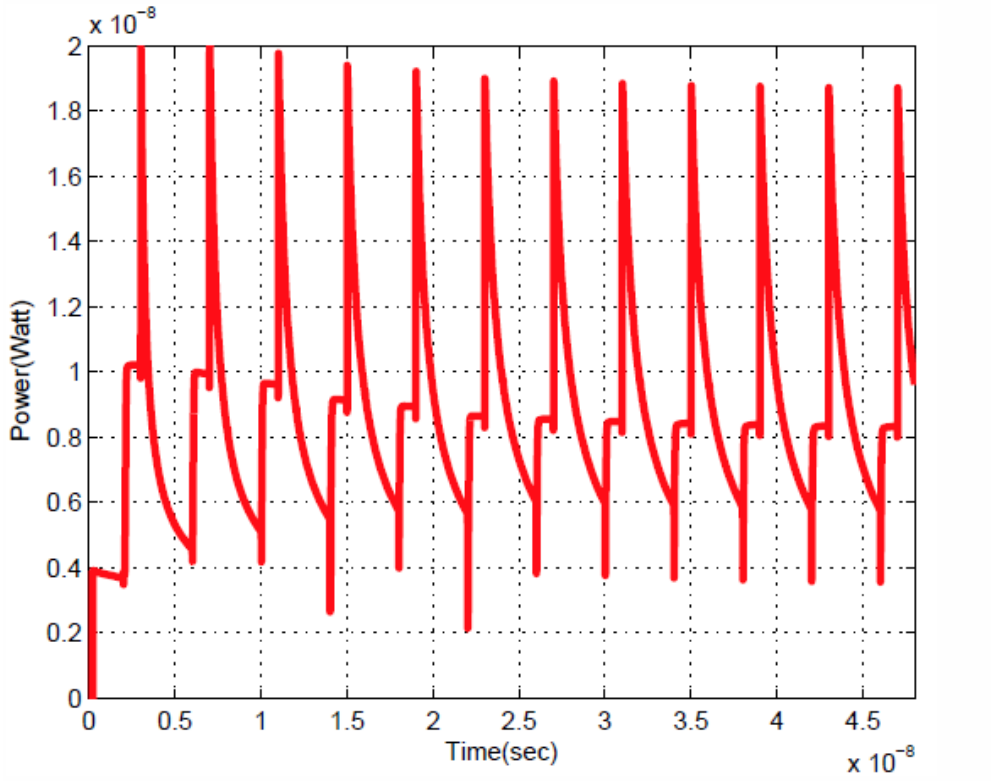


(a) Cell storing '0'

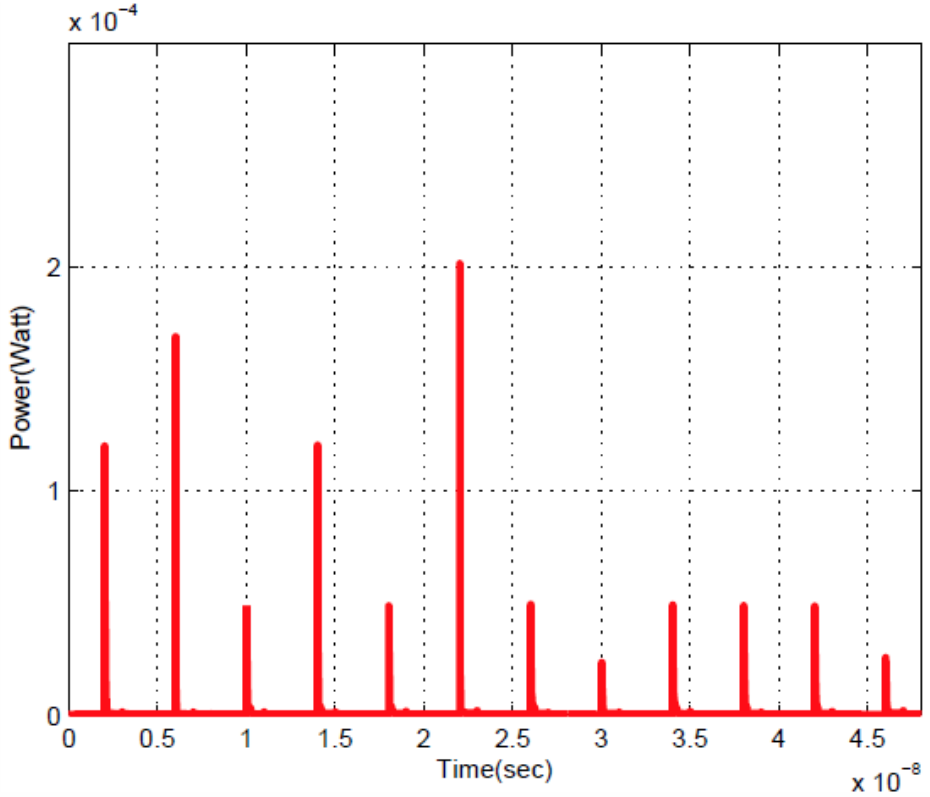


(b) Cell storing '1'

Power Consumption

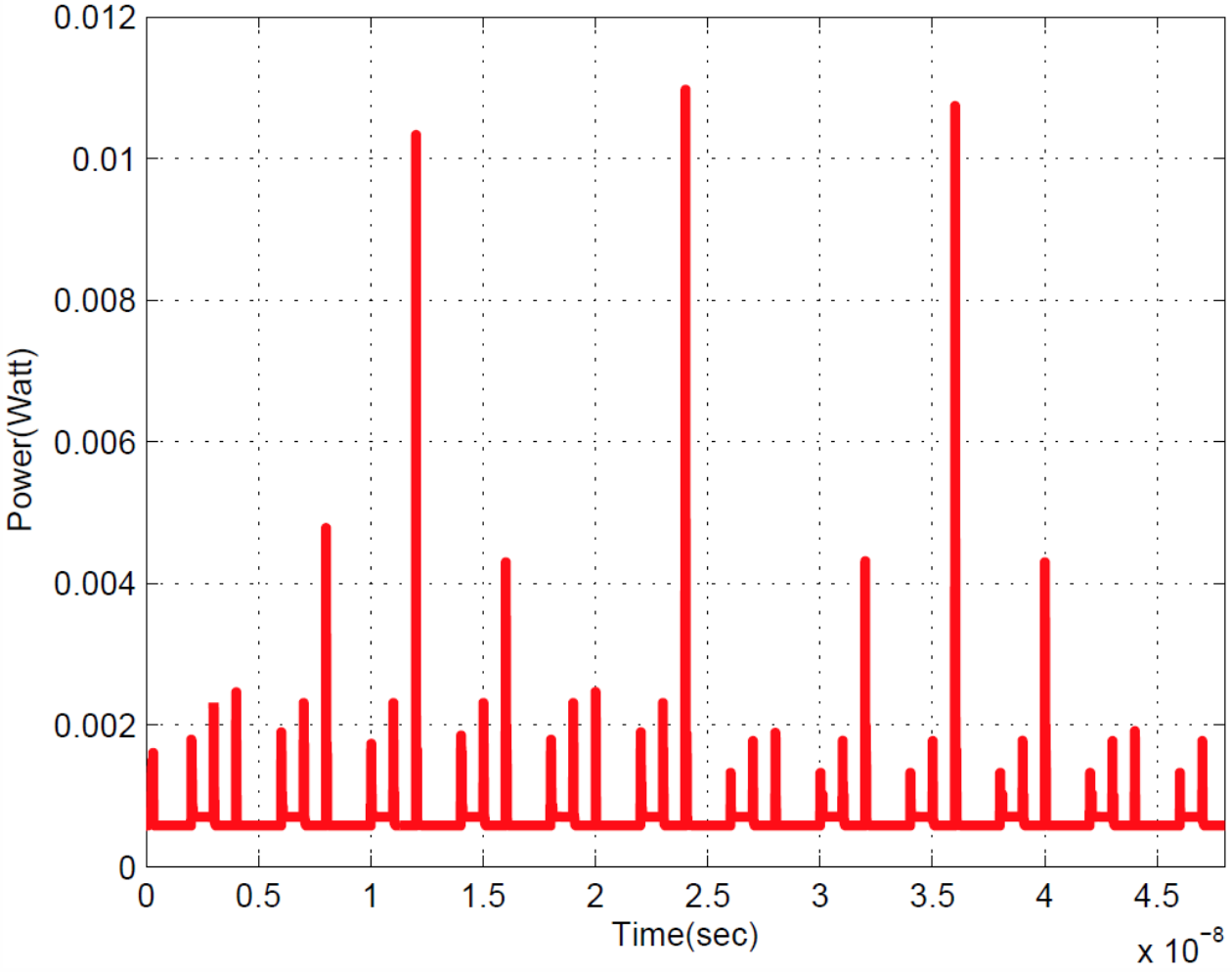


(c) Other cells



(d) All Cells

Power Consumption



(e) All circuits

Stability Comparison

AVERAGE POWER CONSUMPTION COMPARISON OF SRAM.

Description	GFET Based SRAM	Silicon FET Based SRAM
Cell storing 0	28.71 nW	221.3 nW
Cell storing 1	84.7 nW	330.5 nW
Other cells	8.686 nW	137.4 nW
Array	796.4 nW	11.49 μW

Conclusion and Future Work

- Silicon based and Graphene Nanoribbon based FETs are used to design a 6T SRAM.
- A comparative analysis is provided.
- The Stability and Power Consumption are used as metrics for comparison
- GNR-FET is 93% efficient than a 45 nm Silicon Technology.
- In future work, a fully functioning 1K8 array with GNRFET periphery will be designed and characterized

THANK YOU