Compact Behavioral Modeling and Time Dependent Performance Degradation Analysis of Doping and Junction Less Transistors for Analog Designs

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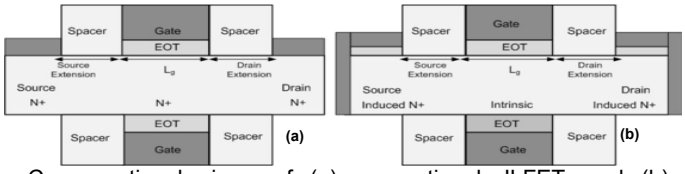
Introduction

- The dopingless (DL) JLFET has recently been proposed as a potential candidate that relaxes the requirements of high work function of gate metal electrode and heavy doping throughout from source, channel and drain regions.
- Previous studies revealed that the DL-JLFET shows better immunity towards process variation induced random dopant fluctuations in contrast with conventional JLFET because of intrinsic silicon nanowire for formation of source, channel and drain regions.
- The time dependent performance degradation of DL-JLFET against channel hot carrier (CHC) effect is not yet analyzed.
- Therefore, time dependent performance degradation of DL-JLFET and its comparative study with conventional JLFET is performed analyzed at circuit level through compact behavioral models.

Major Contributions

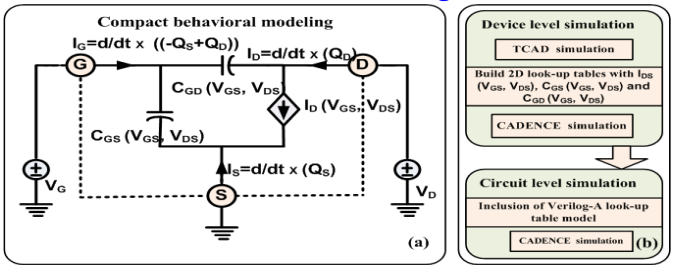
- Investigated the impact of CHC stress at device and circuit level in DL-JLFET and conventional JLFET.
- Proposed a device-circuit co-simulation approach that is suitable for emerging devices for which compact analytical or SPICE models are not available.
- Developed compact behavioral models of both devices capture both DC and transient effects accurately as well these models are computationally efficient.
- We observed that the DL-JLFET device and circuit experiences less CHC stress in contrast to conventional JLFET.

Device Structures



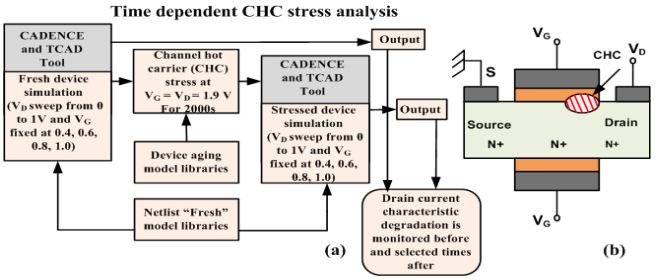
Cross-sectional views of (a) conventional JLFET, and (b) dopingless JLFET.

Compact Behavioral Model and Simulation Framework Design

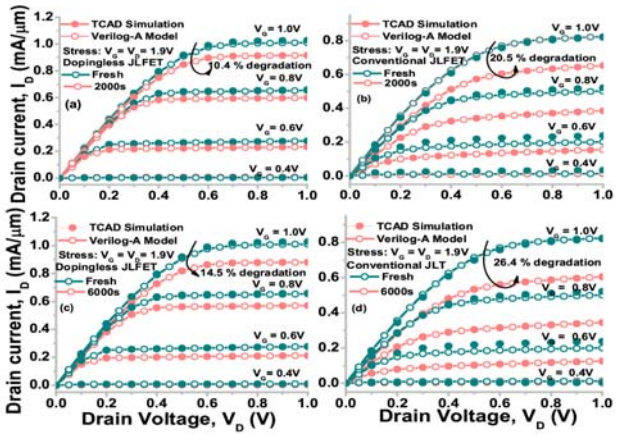


Device-circuit co-simulation approach (a) compact behavioral model for conventional and dopingless JLFETs, and (b) TCAD (ATLAS) device and Cadence (circuit) co-simulation framework

Time dependent performance degradation Analysis

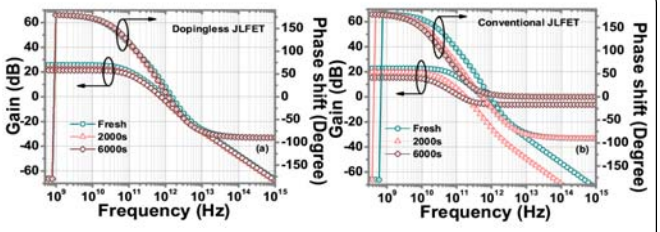


Time dependent CHC stress (a) analysis, and (b) simulation set-up, showing CHC effect near drain side.



Output characteristics of conventional and dopingless n-type JLFETs fresh and stressed (VG = VD = 1.9V) for 2000 seconds (a-b), and 6000 seconds (c-d).

Analog Circuit Simulation Results



Gain and phase shift response of (a) Dopingless, and (b) conventional JLFET based common source amplifier under CHC stress of VG = VD = 1.9V for 2000 and 6000s.

Conclusions

- This study revealed that the DL-JLFETs can sustain sever CHC stress without compromising the circuit performance.
- The developed device-circuit co-simulation approach can be employed for simulation of complex circuits efficiently and accurately.
- Outcome of this work may provide incentives and guidelines for further exploration of DL-JLFETs

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