### Energy-Efficient Design of the Secure Better Portable Graphics Compression Architecture for Trusted Image Communication in the IoT

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### Contributions

**The novel contributions include the following:** 

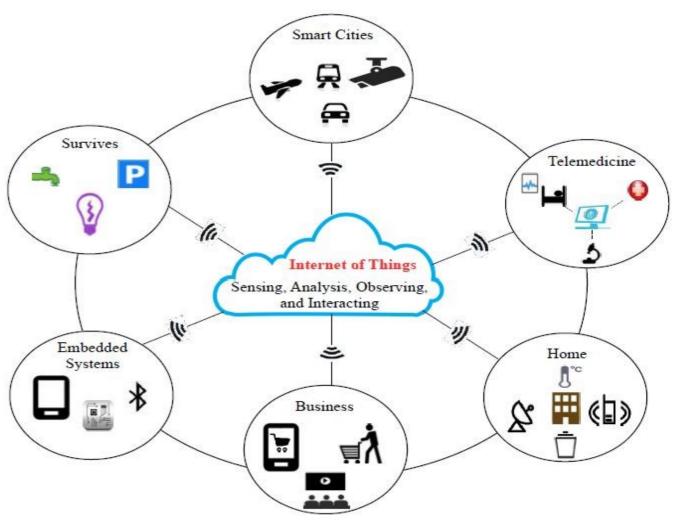
- 1. The first ever attempt to propose an energy efficient hardware architecture of SBPG compression integrated with SDC.
- 2. The concept of SBPG compression integrated with SDC, which is suitable for low power intelligent traffic surveillance.
- 3. A Simulink®–based prototype of the algorithm implementation.
- 4. An experimental analysis and evaluation of the proposed architecture.





### **Applications of the IoT**

- Up to now, the concepts that make the IoT have been incorporated in a wide range of fields including transportation, logistics, energy, agriculture, defense, and smart environments such as personal residences, offices, buildings, or infrastructure.
- When things, as envisioned by the IoT, become part of the same network, many smart services and processes will become easily possible and will be able to change how people understand and deal with the economy and environmental issues.



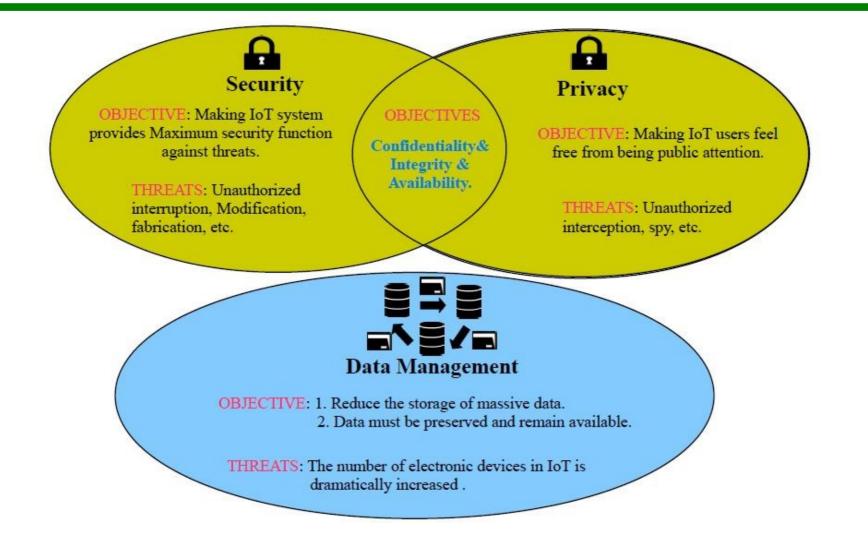
#### **Application of the IoT**

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### **IoT Challenges**



#### **IoT Challenges**

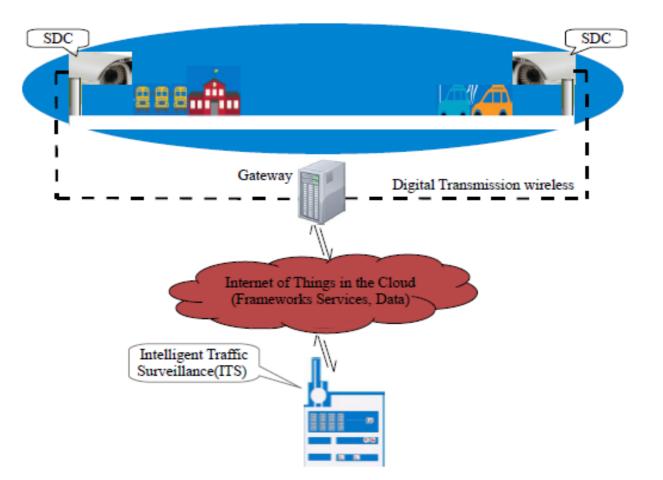
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# Framework Overview of SDC Integrated with SBPG in the IoT



#### **Components of Intelligent Traffic Surveillance in the IoT**

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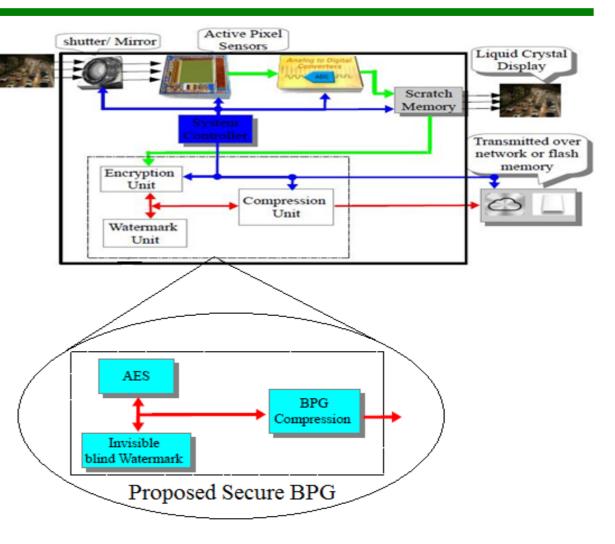
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### **Architectural Overview of SBPG integrated SDC**

□ Secure Digital Camera is a novel approach in capturing images .

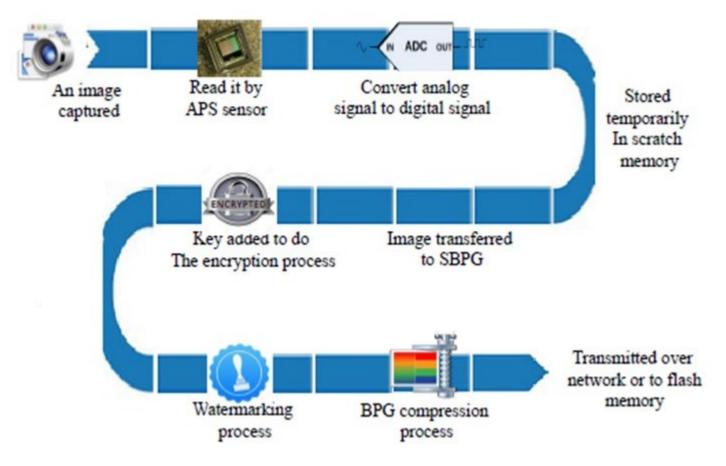
- the proposed framework architecture offers:
- 1. Double-layer protection: encryption and watermarking that will address all issues related to security, privacy and digital rights management (DRM), including ownership rights, tracking usage, extent of tampering, and facilitation of content authentication.
- 2. Introduces a new hardware architecture of the Better Portable Graphics (BPG) Compression, which is integrated with SDC.



#### **Proposed Secure Better Portable Graphics**



### **Proposed Secure BPG Architecture**



**Stages of the SBPG Integrated with SDC** 

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### **Better Portable Graphics (BPG)**

#### **What is Better Portable Graphics (BPG) compression?**

BPG is a new image format offering several advantages over the JPEG format. It achieves a higher compression ratio with smaller size than JPEG for similar quality.

□ Since its introduction in 1987, the Joint Photographic Experts Group (JPEG) graphics format has been the *de facto* choice for image compression. However, the new compression technique BPG outperforms JPEG in terms of compression quality and size of the compressed file.

### The reference BPG image library and utilities (libbpg) can be divided into four functions: [1]

- 1) BPG encoder
- 2) BPG decoder
- 3) Javascript decoder
- 4) BPG decoding

[1] F. Bellard, "The BPG Image Format," http://bellard.org/bpg/, last Accessed on 09/20/2015.

### Why BPG?

□ Why BPG compression instead of JPEG? Attributes that differentiate BPG from JPEG and make it an excellent choice include the following:

- 1) Meeting modern display requirements: high quality and lower size.
- 2) BPG compression is based on the High Efficiency Video Coding (HEVC), which is considered a major advance in compression techniques.
- 3) Supported by most web browsers with a small embedded Javascript decoder.





### Why BPG?

■ Why BPG compression and not JPEG?

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4) It is open source. No patent issues (unlike JPEG 2000).

5) BPG is close in spirit to JPEG and can offer lossless compression in the digital domain.

- 6) Different chroma formats supported include grayscale, RGB, YCgCo, YCbCr, Non-premultiplied alpha, and Premultiplied alpha.
- 7) BPG uses a range of metadata for efficient conversion including EXIF, ICC profile, and XMP.

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### Hardware vs. Software Encoding

- The advantages of hardware versus software implementation:
  1. Minimal hardware is used to encode real-time images.
- 2. Power usage is reduced significantly compared to a general purpose processor.
- 3. The host is not slowed down by the dedicated circuity.
- 4. Hardware implementation is not affected my malicious software such as worms, Trojans, etc.



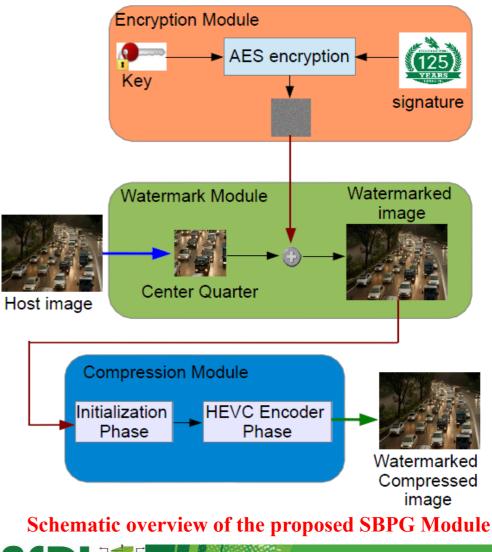


### **SBPG: Algorithm and Architecture**

#### **Encryption and watermark module:**

The invisible-robust-blind watermarking algorithm is summarized as follows:

- 1. Optimization for robustness, quality, and computational load because of the use of the center portion of the image.
- 2. Watermarking is done in the frequency domain using the Discrete Cosine Transform (DCT) that will increase watermarking insertion speed.
- 3. The insertion of the watermark is done in the midfrequency of the image block so that will increase the robustness since any removal of high or low frequency components of the watermarked image does not significantly affect the watermark.



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### Watermarking Module (Insertion Algorithm)

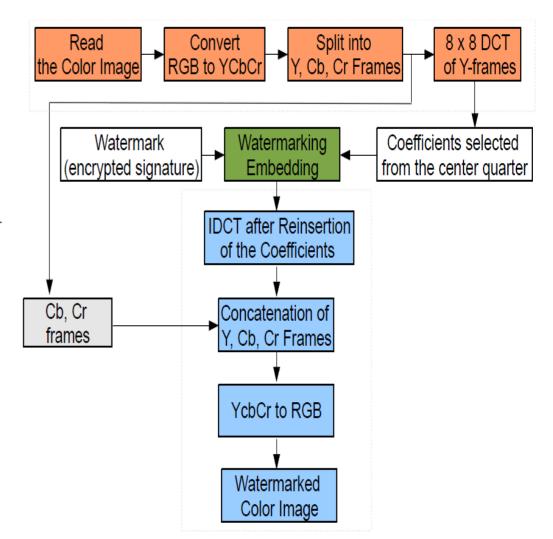
- ✓ Four mid frequency coefficients are chosen from each block in the center quarter of the image.
- ✓ A vector R of size K is generated where K is the number of blocks in the center quarter of the image given in:

$$R = \{r_{1,i}, r_{2,i}, r_{3,i}, r_{4,i}, \dots, r_{1,K}, r_{2,K}, r_{3,K}, \dots, r_{4,K}\}$$

✓ A pseudo random sequence is chosen from bits in the encrypted signature, which will be used as the watermark represented shown in:

 $A = \{a_1, a_2, a_3, \dots, a_{4 \times K}\}$ 

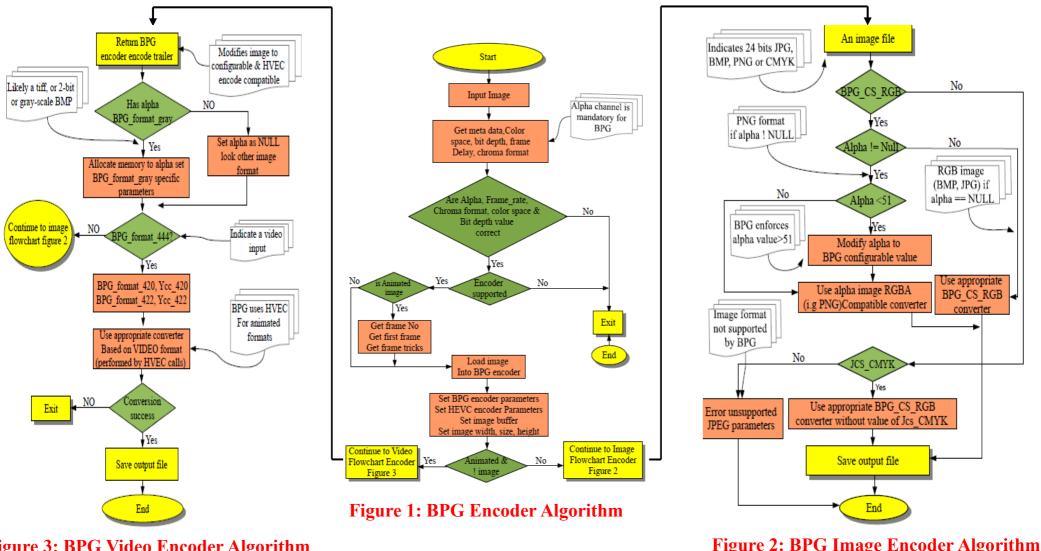
✓ The watermark A is inserted into the DCT coefficients of the image of vector R according to Eqn:



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 $r_i' = r_i + \alpha \mid r_i \mid a_i,$ 

### Simplified Analysis of the BPG algorithm



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**Figure 3: BPG Video Encoder Algorithm** 

### **Proposed Hardware Architecture for the BPG Encoder**

Algorithm 1 BPG Encoder Algorithm.

1: input imageX

- 2: get Parameters ← {PixelDpth, ColorSpace, Alpha}
- 3: calculate Resolution  $\leftarrow \{pixels/inch\}$
- 4: calculate  $ColorType \leftarrow \{TrueColor, GrayScale\}$
- 5: if Length > 2 then
- 6:  $Bitdepth \leftarrow \{MateData/numChannel\}$
- 7: if  $Bitdepth \neq 8$  then
- 8:  $AlphaChannel \leftarrow \emptyset$
- print "ERROR: while opening bitdepth encoder"

#### 10: else

- 11: if  $Bitdepth \neq 8$  then
- 12:  $AlphaChannel \leftarrow \emptyset$
- 13: print "ERROR: while opening bitdepth encoder"
- 14: if ColorType < 1 then</p>
- 15: print "ERROR: Color space is not supported"

#### 16: end

- 17: print "Bit Depth and color space is supported"
- 18: print "Image accepted for BPG compression"
- 19: if AlphaChannel  $\neq$  Null then
- use appropriate BPG CS RGB converter

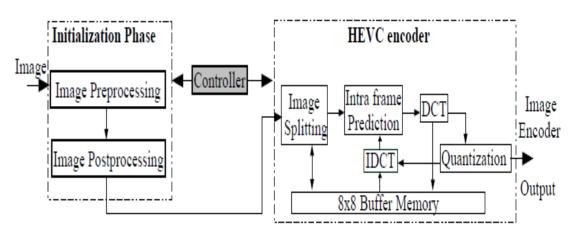
#### 21: else

- 22: if AlphaChannel < 51 then</p>
- 23: modify alpha to BPG configurable

#### 24: end

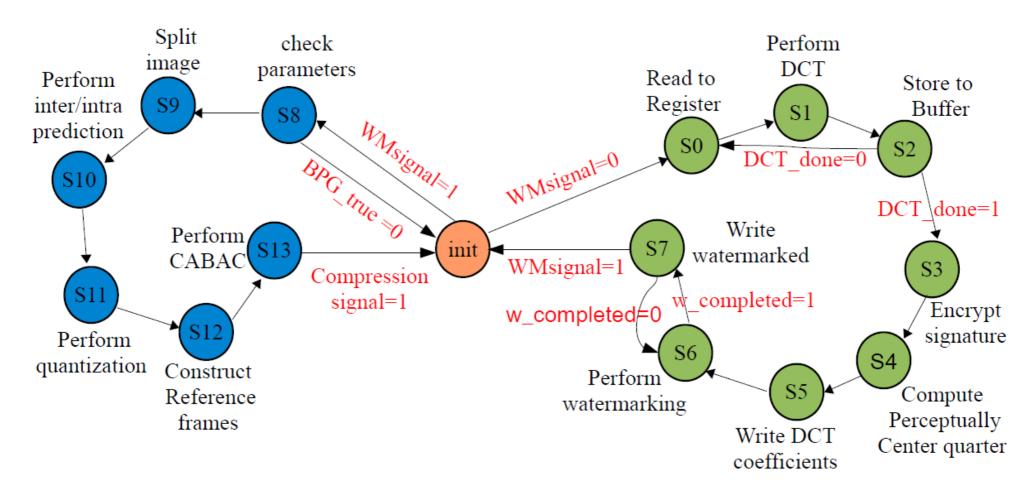
- 25: **use** alpha image RGBA compatible HEVC
- 26: save output file BPG image
- 27: end

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#### System Level Architecture of the Proposed Algorithm

### **SBPG**



Finite State Machine Presenting the Controller of the SBPG Architecture

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### **Motivation for Energy-Efficient Design**

- > Power consumption has become a major concern in any portable application.
- Low power consumption means extended battery life, which increases portability. Moreover, low power consumption results in a decrease of the packaging cost, and it is beneficial for cooling in both portable and non-portable applications.
- The aim of this paper is to optimize the SBPG baseline design, which is presented in the previous slides, to achieve an energy-efficient SBPG design.





### **Digital System-on-Chip (SoC) energy Optimization**

- The higher the level of abstraction level, the higher is the possibility of optimization and the bigger is the granularity as the large building blocks or basic elements are used. At the same time, more time is required for design iterations for low-power optimization.
- The higher the abstraction level, the lower is the accuracy and vice versa. The lower the level of abstraction, the lower is the optimization possibility.

Digital Abstraction Levels	System Level	Behavioral Level		Transistor Level	Layout Level	
Optimization Mechanism	Battery Scheduling Backlight Management Subsystem Shut-down Variable Voltage Variable Frequency	Loop transformation Memory Architecture Data Mapping Low-Power Scheduling	Gate Remapping Pin Reordering Gate Guarding Clock Gating Input Vector Control	Multiple Supply Voltage Multiple Threshold Voltage Variable Threshold Voltage Multiple-Oxide Thickness		
Optimization Possibilities	10 - 20x	10 - 20x Increasin	2 - 5x g Power saving	20% - 50%	20% - 50%	
Optimization Time	Seconds to Minutes		Minutes to Hours Design Iteration Time	Ī	Hours to Days	

Power Reduction at Different Abstractions of Digital SoC

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### Proposed Low-power SBPG: Optimization Perspective

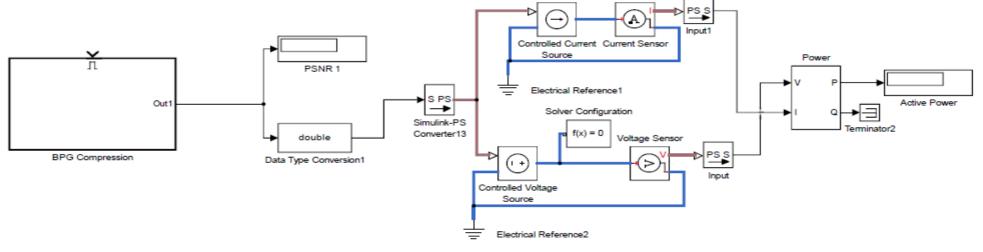
- DCT Optimization: the aim is to minimize the number of arithmetic operations by reconstructing the image just with the DC component along with few AC component of low frequencies that leads to computationally efficient operations without compromising quality.
- Sub-Sampling: it is the process of encoding the image by implementing less resolution for chroma information than Luma information. It takes advantage of the fact that the human eye is less sensitive to colors than brightness.
- In the intra Prediction: the design simplified the mode decision by defining constant values as integers using round-off.
- In the inter Prediction: advanced Motion Vector Prediction (AMVP) is used to remove duplicate motion vector candidates.

Quantization: increasing the sampling size to reduce the computational operations. In addition, the quantization block uses a parallel structure.

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### **Mechanism of Power Measurement**

- Power estimation can be broadly categorized into pattern-dependent and pattern-independent. In the pattern-dependent method, the simulation results are considered for estimating the power dissipation.
- ➢ In this design we have adopted pattern-independent method i.e. many simulations were run in the design with different inputs and the average of the power dissipated was considered.
- The design is considered as a black box and the current and voltage values are considered from the design, in order to calculate power. This was achieved with the help of sensors and power blocks available in Simulink ®. The design is simulated using the ode45 solver configuration.



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**Mechanism of Power Measurement** 

### Simulink® Based Modeling

- $\bullet$  The proposed algorithm is prototyped in Simulink  $\mathbb{R}$
- The methodology that is used to represent the high level system modeling is bottom-up.
- The first step is focused on building functional units; the next step is to integrate these units into subsystems.
- Finally, verifying and testing overall system functionality.





- Five standard images are selected randomly from a large set of images of the Joint Picture Expert Graphics (.jpg) with different spatial and frequency characteristics.
- The cover image, watermarked image, and corresponding BPG image are shown for a sample image.



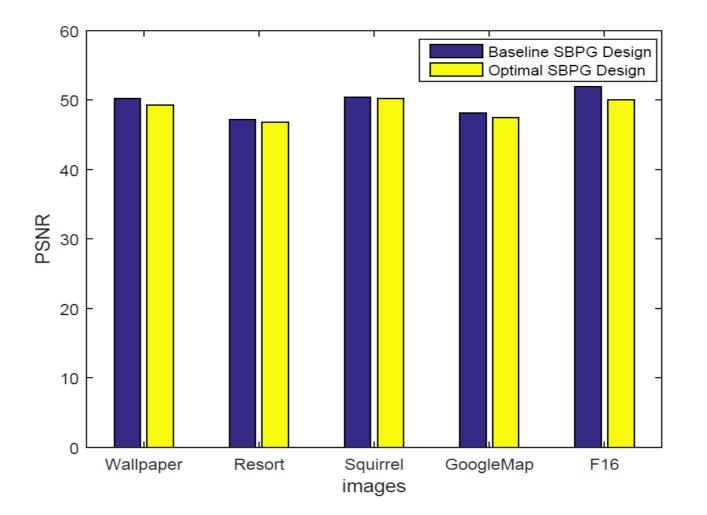
(a) Cover Image.
 (b) Watermarked Image
 (c) Watermarked Compressed Image
 Secure BPG Compression of Resort Image (256×256).

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**TABLE1:** Quality metrics for the proposed architecture and comparative perspective with baseline design:

Test	SBPG Baseline Design		SBPG Optimal Design		Power
Image	PSNR	Power (nW)	PSNR	Power (nW)	Reduction
Wallpaper 128×128	50.2	8.09	49.31	6.63	18%
Resort $256 \times 156$	47.14	8.2	46.82	6.89	16%
Squirrel $256 \times 256$	50.37	8.22	50.19	6.85	17%
GoogleMap $256 \times 256$	48.09	8.3	47.5	6.90	17%
F16 512×512	51.9	8.55	50.03	6.94	19%

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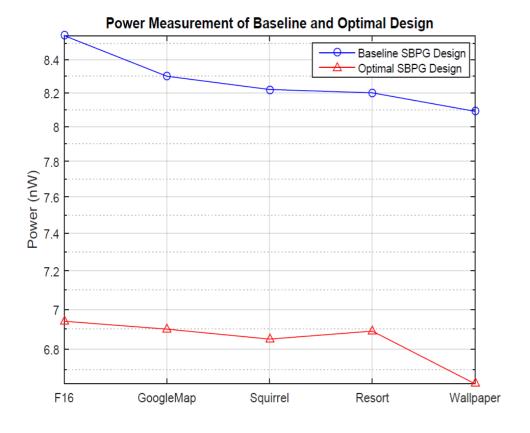
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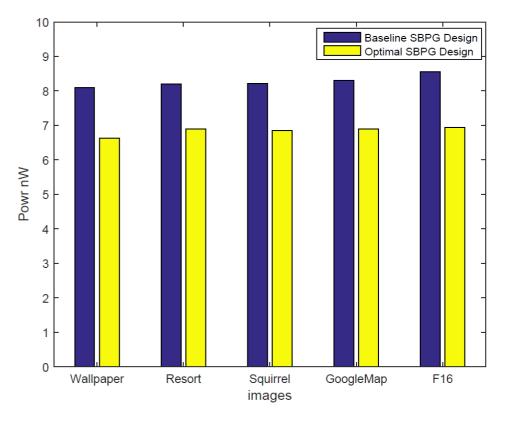
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### Conclusions

- This paper proposes frameworks for secure digital camera in the IoT. The objectives of this work are twofold:
- 1. The proposed framework architecture offers double-layer of protection: encryption and watermarking that will address all issues related to security, privacy, and digital rights management (DRM) with applying hardware architecture of state-of-the-art image compression technique of Better Portable Graphics (BPG), which achieves high compression ratio with small size.
- 2. The proposed framework of SBPG is integrated with Digital Camera. Thus, the proposed framework of SBPG integrated with SDC is suitable for high performance imaging in the IoT, such as Intelligent Traffic Surveillance (ITS) and Telemedicine.
- ➤ As the visual quality of the watermarked and compressed images improves with the larger value of PSNR, the results show that the proposed SBPG substantially increases the quality of the watermarked compressed images.

### **Future Work**

- The proposed methodology could be extended to energy-efficient design of secure image sensors in the IoT communication that could act as a wireless sensor framework.
- Designing the proposed SBPG in a hardware description language such as Verilog, then implementing it using Field Programmable gate Array (FPGA).
- Exploring mechanisms to integrate these SBPG and SDC in diverse Internet of Things (IoT) and smart cities applications is also future research.

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# Thank you!!