Simscape® based Ultra-Fast Design Exploration of Graphene Nanoelectronic Systems

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Presented By
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Introduction and Motivation

Demand driven industry

Consumer requirements → Designer actions

Smaller, cheaper and low power consuming devices

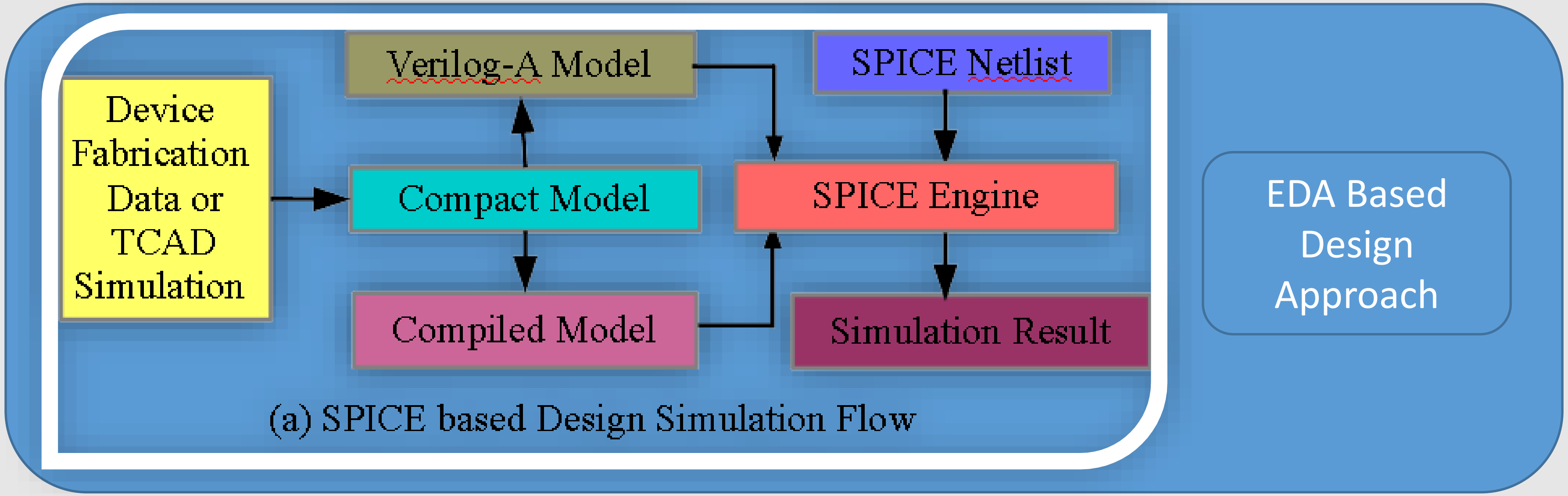
Solutions:

- Analog Mixed Signal-System on Chip (AMS-SoC)
- Graphene based technologies

Two Solutions:

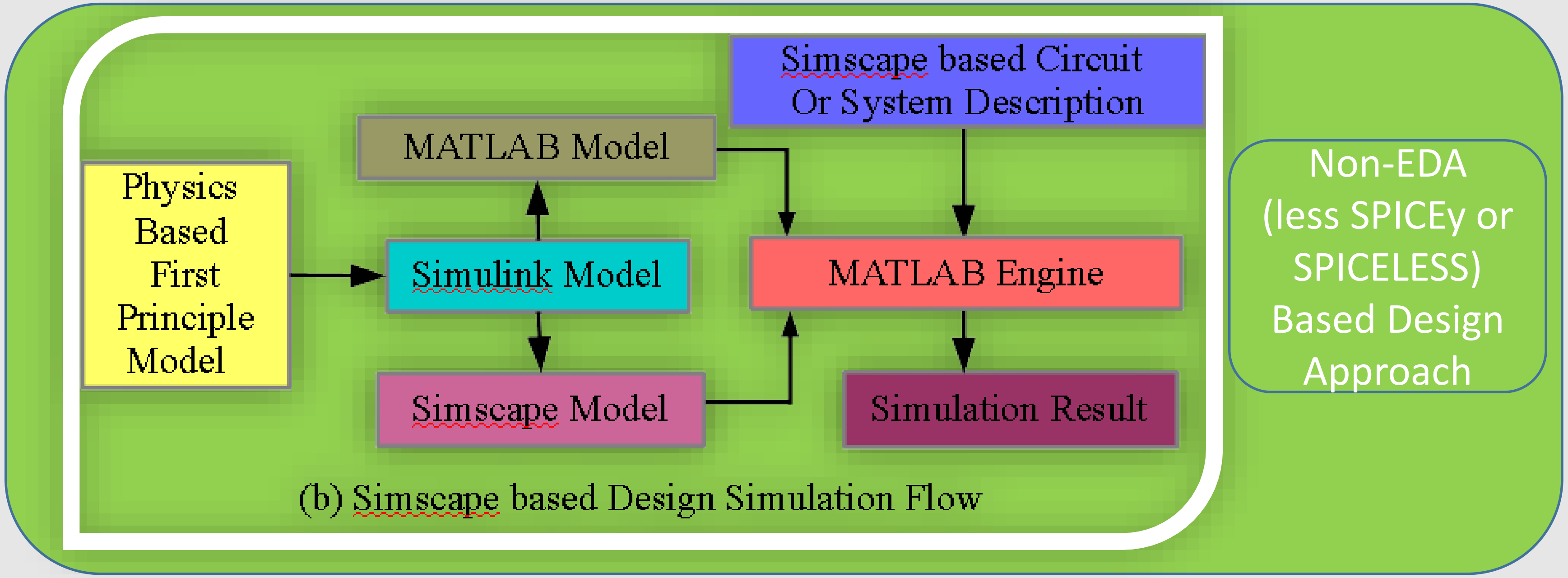
	1. AMS-SoC	2. Graphene based Technologies
WHY	Analog, Digital and RF components within a single chip for miniaturization and low power.	Silicon reaching its fundamental limits beyond 10nm
PROBLEM	Extensive simulation for accuracy (analog domain simulation: very complex, time consuming)	Graphene still in experimental stage
INDUSTRIAL REQUIREMENTS	Suitable simulation tools for faster and efficient testing and implementation	

Standard SPICE based Flow



- Drawbacks associated with SPICE simulation:
  - Heavy computational needs → Prolong design time + Increase non-recurrent design cost
  - Need of fab data or TCAD simulations → Not always available for new or emerging technologies,
  - Limited design optimization support

Proposed Simscape® based Flow

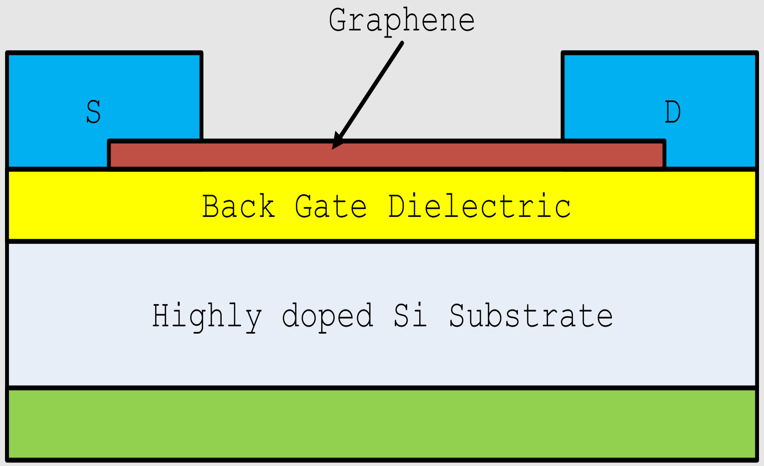


- Simscape® based design flow offers distinct advantages over conventional SPICE:
  - No need of fab data → Good platform to model emerging technologies
  - Fast and easy optimization at system level.

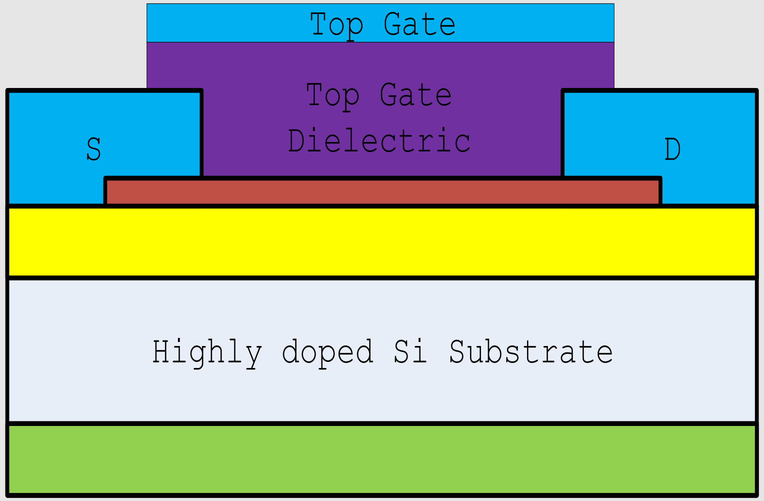
Novel Contributions

1. A non- EDA (Simscape®) based ultra-fast design flow is explored.
2. Modeling of GFETs using Simscape® .
3. Modeling of a GFET based LNA using the Simscape® graphical environment.
4. Experimental validation of the Simscape® device level models with results obtained in MATLAB®[I. Meric,2008], SPICE[R. Doe ,2013], VHDL-AMS[I. J. Umoh,2011] or Verilog-A[M. A. Khan,2014] models.
5. Characterization of GFET based case study circuit (LNA) and comparison with Verilog-A based designs.

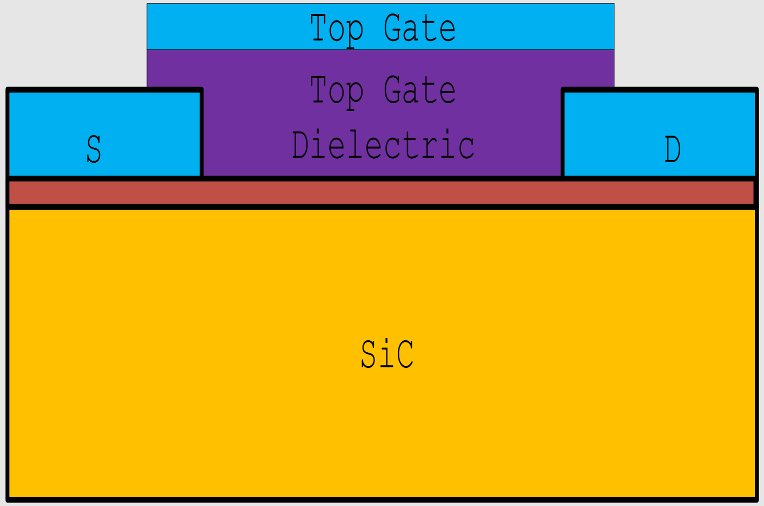
Graphene FET



(a) Back-gated graphene transistor



(b) Dual-gate graphene transistor



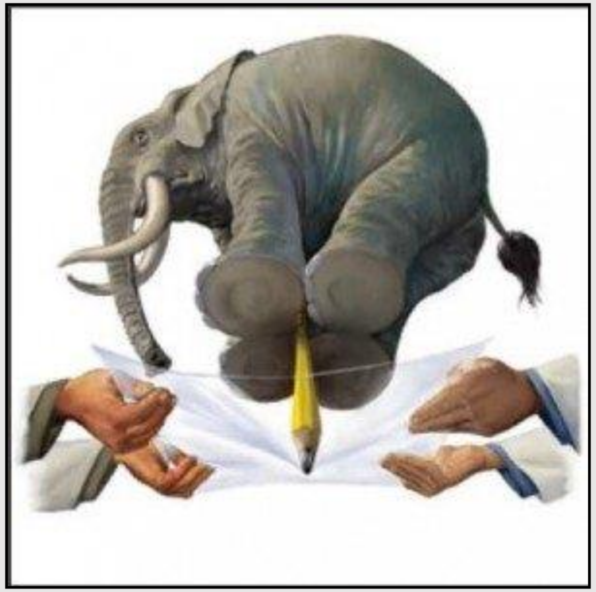
(c) Epitaxial graphene from SiC and transistor structure

- ❑ Semi-metallic nature → $\rho_{ON}/\rho_{OFF} \sim 6$ → $I_{ON}/I_{OFF} < 10$ at room temperature
- ❑ Attractive for high-speed analog electronics, where transistor current gain is more important than I_{ON}/I_{OFF}
- ❑ Transistors having cut-off frequencies as high as 350 GHz

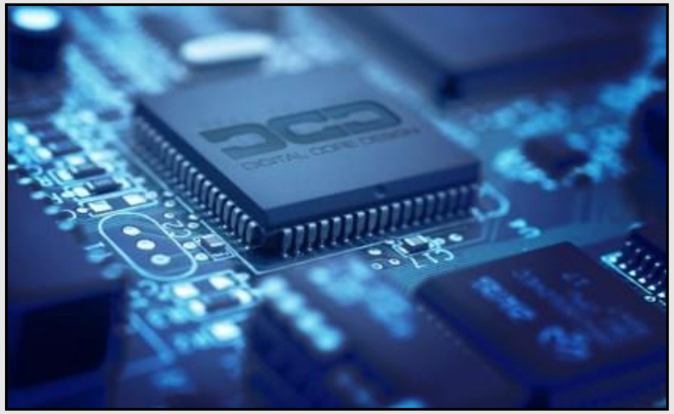
How graphene can address future devices?

(a) Lightweight

(b) Flexible



(c) Strong



(d) Faster and High packing density

(e) Transparent

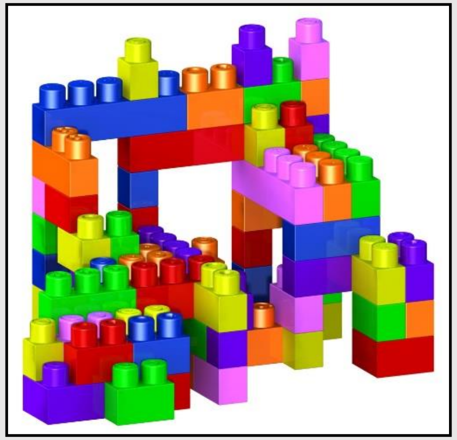
All this with little change in current processing techniques !

Simscape® Modeling of GFET

- Two ways to build custom Simscape® models:

(i) Graphical method using fundamental Simulink®/Simscape® blocks

- Hard to build: may not be precise, interfacing problem linking different domains together.
- Less robust: May not work for all models and for all application.
- Not reusable: May not be used for different applications.



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(i) Textually with the Simscape® physical modeling language

- Simscape® physical modeling language based on physical network approach.

- Offers better portability and is easier to maintain
  - Does not depend on the location of the input in the system.
  - Can handle algebraic constraints easily.
  - Easier modeling in multiple domains.

- Makes hierarchical modeling and simulation of complex system easier as well.

Graphene FET: Structure

For a negative V_{bs}, the source/drain region is P-type
mobility = 700 cm^2/V s,
R_s = 800, and
E_c = 4.5 kV/cm.

Case 1

Top-gate voltages of 0 V, -1.5 V, -1.9 V and -3 V were used and V_{ds} is varied from 0 to -3 V.

For positive V_{bs}, the source/drain region is n-type
mobility = 1200 cm^2/V s,
R_s = 1500 , and
E_c = 15 kV/cm.

Case 2

Top-gate voltages of -0.8 V, -1.3V, -1.8 V, -2.3 V, and -2.8 V were used and V_{ds} is varied from 0 to -3 V.

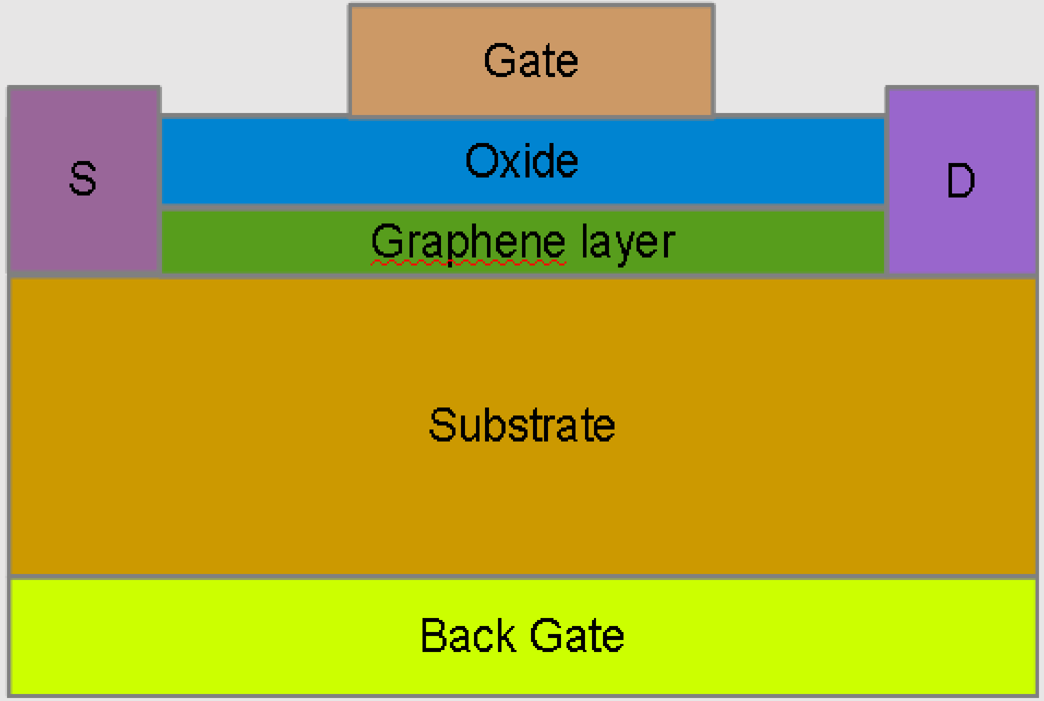


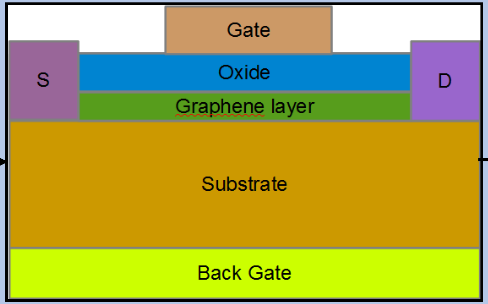
Fig. 1. Dual-gate GFET cross-section

The device parameters were selected are based on published results [5]

Simscape® based Graphene Device Simulation

Simscape® Language (.ssc file)

Build the library
>>ssc_build



Simulink®

COMPONENT MODEL

Declaration Section

- Nodes: electrical
- Inputs, Outputs
- Variables (through, across and internal)
- Parameters

Setup

- Parameter Checking
- Define relationship between component variable and nodes
- Initial Condition
- Derived Parameters

Equation

- Algebraic, discontinuous, differential

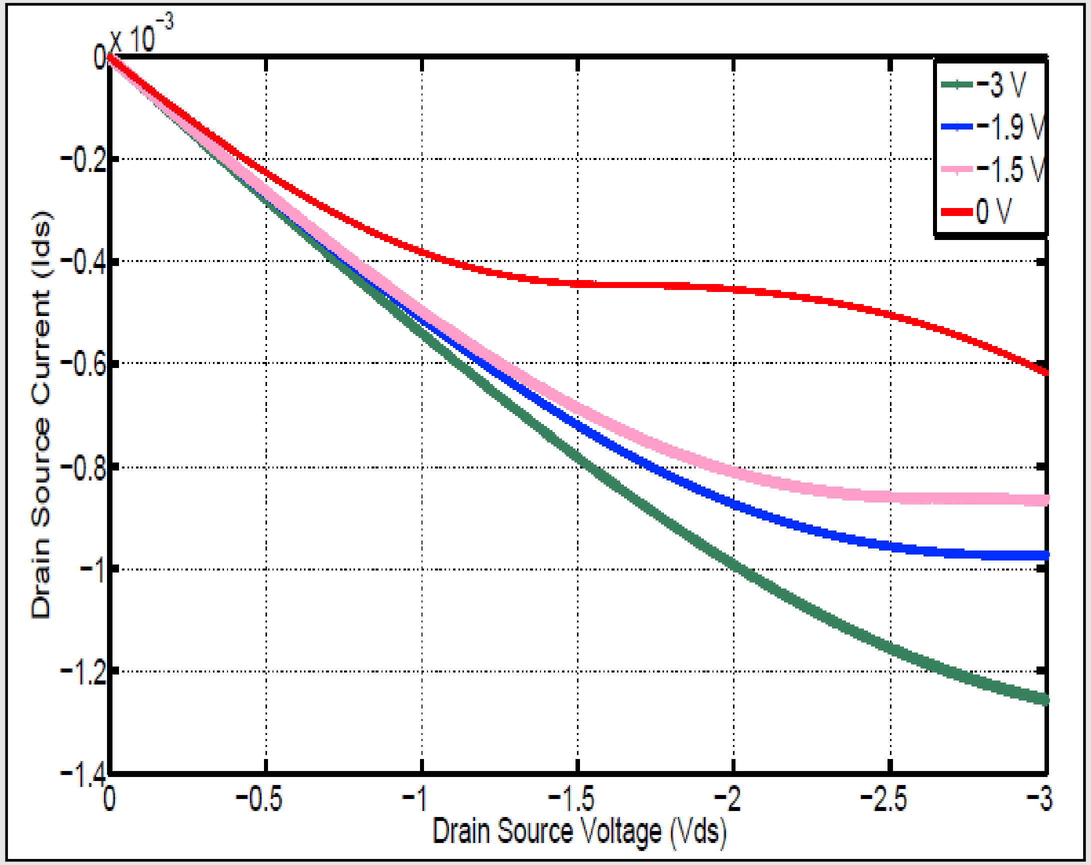
Parameters

Rs = {800, 'Ohm'};
mu = {700,'cm^2/s/V' };
Ec = { 4.5e5,'V/m' };
Hsub = { 285.0e-9,'m' };
tox = { 15e-9, 'm' };
L = { 1e-6, 'm' };
W = { 2.1e-6, 'm' };
ntop = { 2.1209e16,'cm^-3' };
Vgs0 = { 1.45, 'V' };
Vbs0 = { 2.7, 'V' };
and so on…

Variables

Vds= {1,'V'};
Ids={1,'A'};
Vgs= {1,'V'};
Vbs= {1,'V'};
Ctop ={1,'F/cm^2'};
Cback ={1,'F/cm^2'};
Vo ={1,'V'};
Vg0 ={1,'V'};
Vc ={1,'V'};
Rc ={1,'Ohm'};
Gamma ={1,'1'};
Vdsat ={1,'V'};
Io={1,'A'};
and so on…

Case 1: For negative V_{bs}



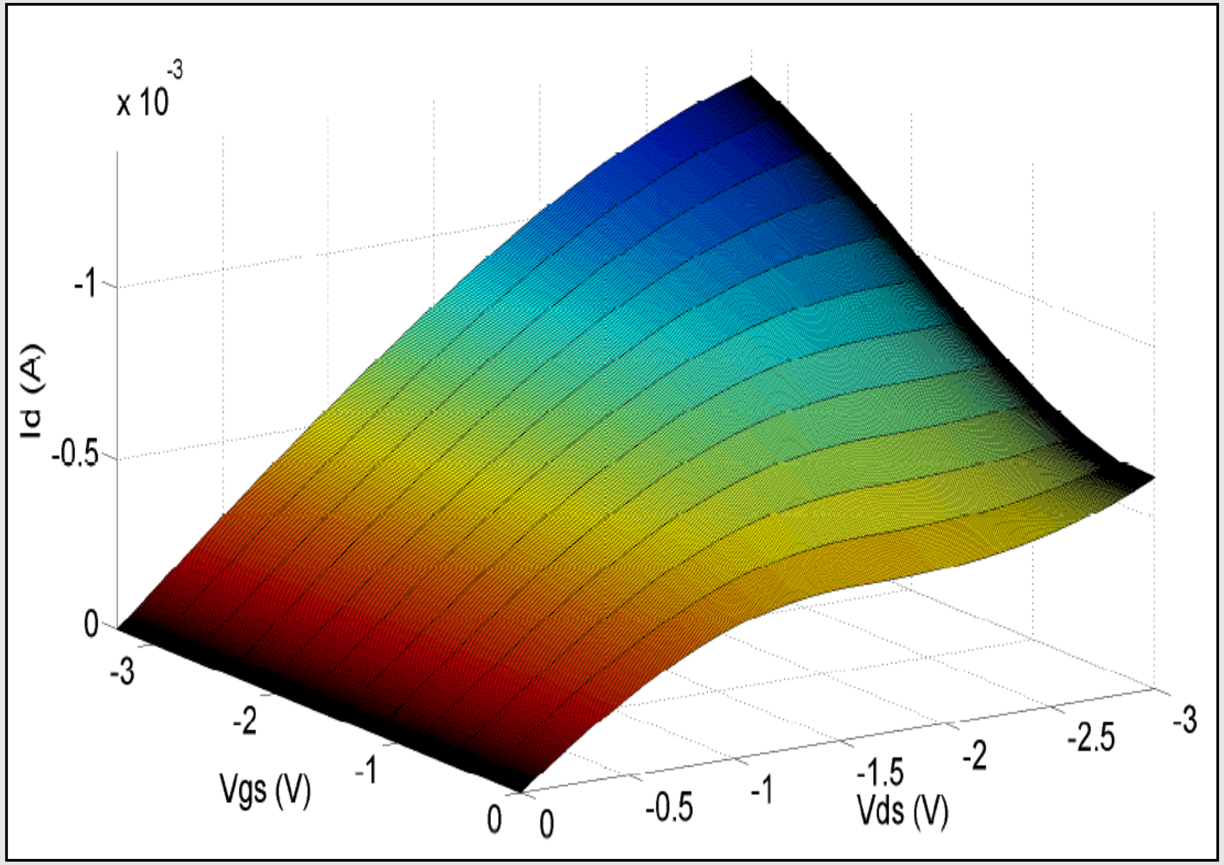
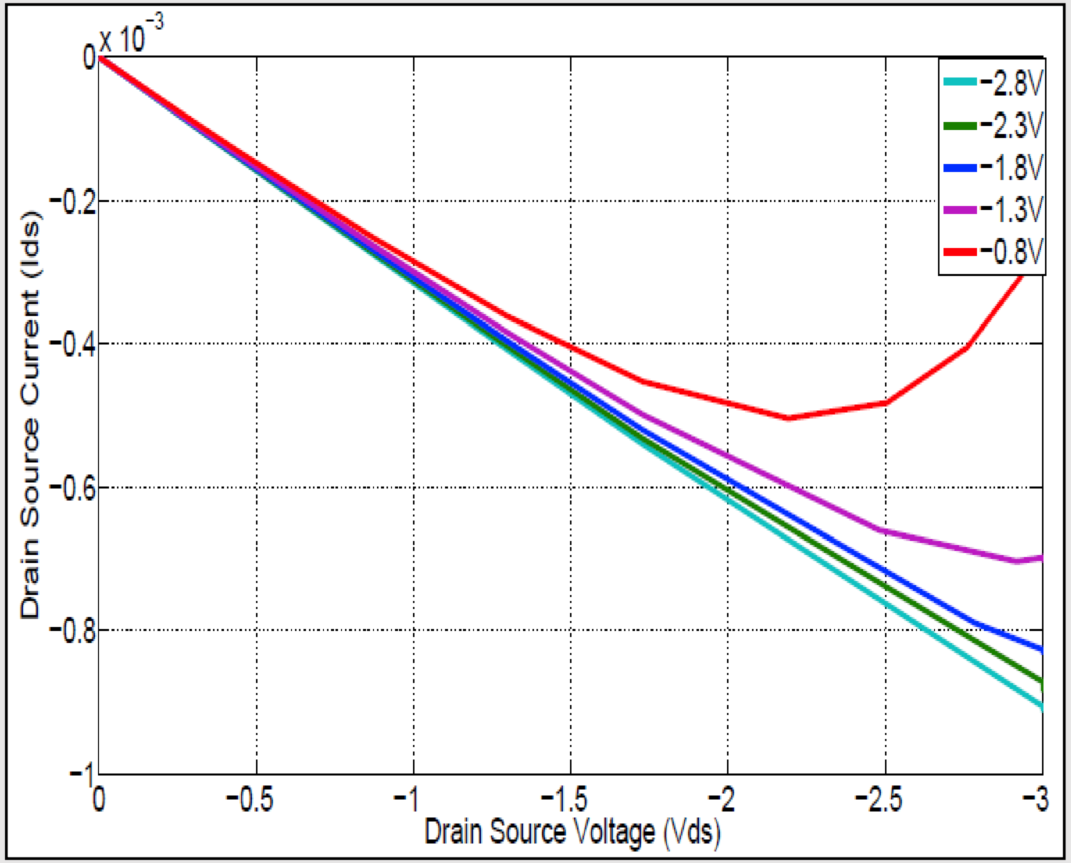


Fig. 2. I-V Characteristics of continuous and discrete values of V_{gs} for P-type GFET

Case 2: For positive V_{bs}



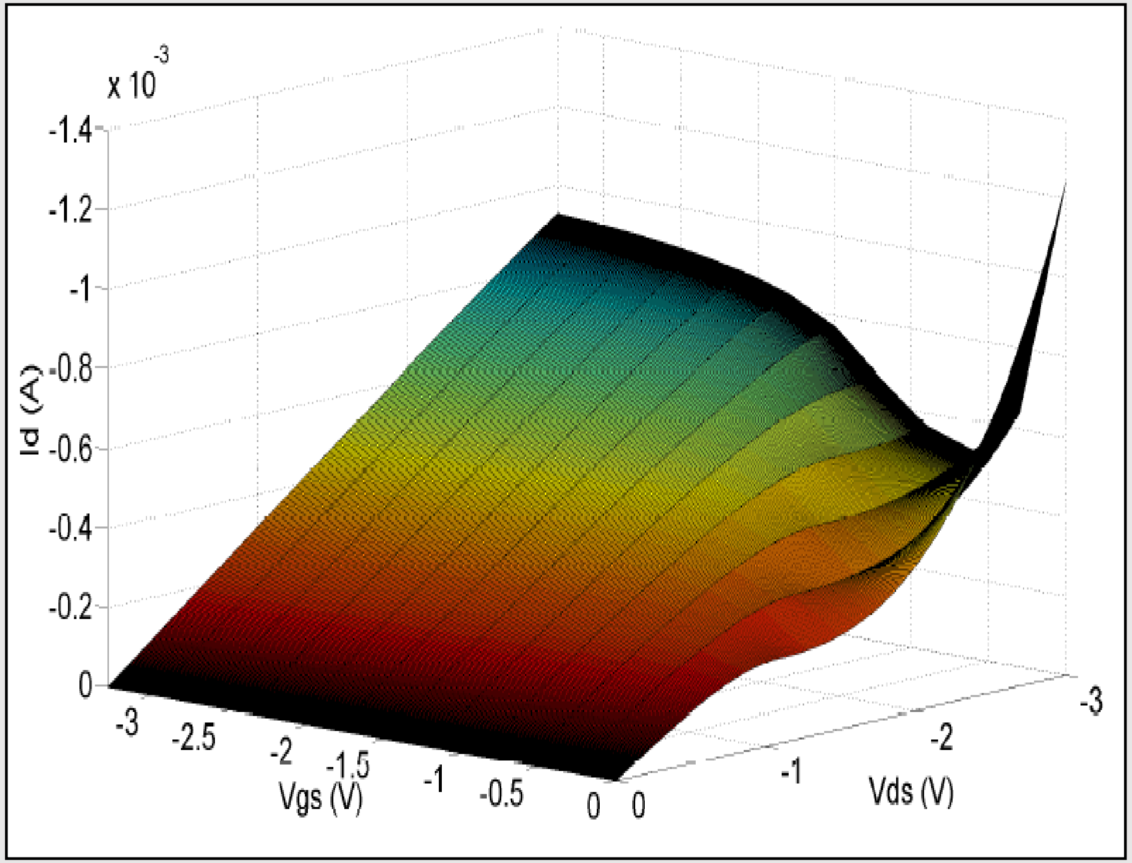


Fig. 3. I-V Characteristics of continuous and discrete values of V_{gs} for N-type GFET

Comparison with Results from VHDL-AMS[Umoh, 2011]

❑The result obtained from Simscape® is identical:

- For a top-gate voltage of 0 V, -1.5 V, -1.9 V and -3 V and a back gate voltage (Vbs) = -4.0 V, the drain current decreased with increase in the Vds and decrease in the top gate voltage.
- For a top-gate voltage of -0.8 V, -1.3 V, -1.8 V, -2.3 V and -2.8 V and a back gate voltage (Vbs) = +4.0 V, the drain current decreased with decrease in the top gate voltage.

I. J. Umoh and T. J. Kazmierski, “VHDL-AMS Model of A Dual Gate Graphene FET,” in Proceedings of the Forum on Specification and Design Languages, 2011, pp. 1–5.

GFET based LNA Circuit Design

- ❑High gain: better processing of signal for subsequent circuit stages and low noise
- ❑Low NF: better reception of signal
- ❑Non-linearity: Avoids blocking and intermodulation problems
- ❑Impedance matching: Maximizes power transfer and minimizes reflection

Note:

- ➢Both gain and NF vary with the operating frequency
- ➢Trade-off between gain and NF

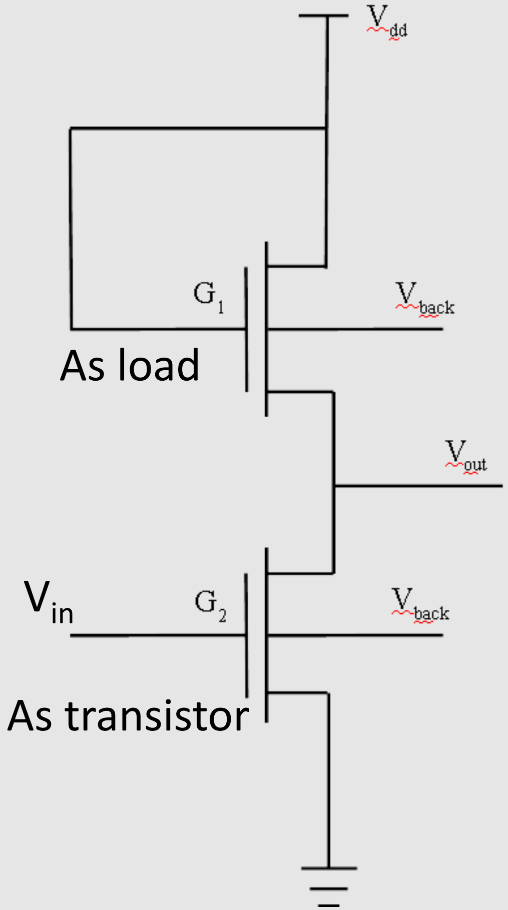


Fig. 4. Schematic of a GFET based LNA circuit

Simscape® modeling of the LNA

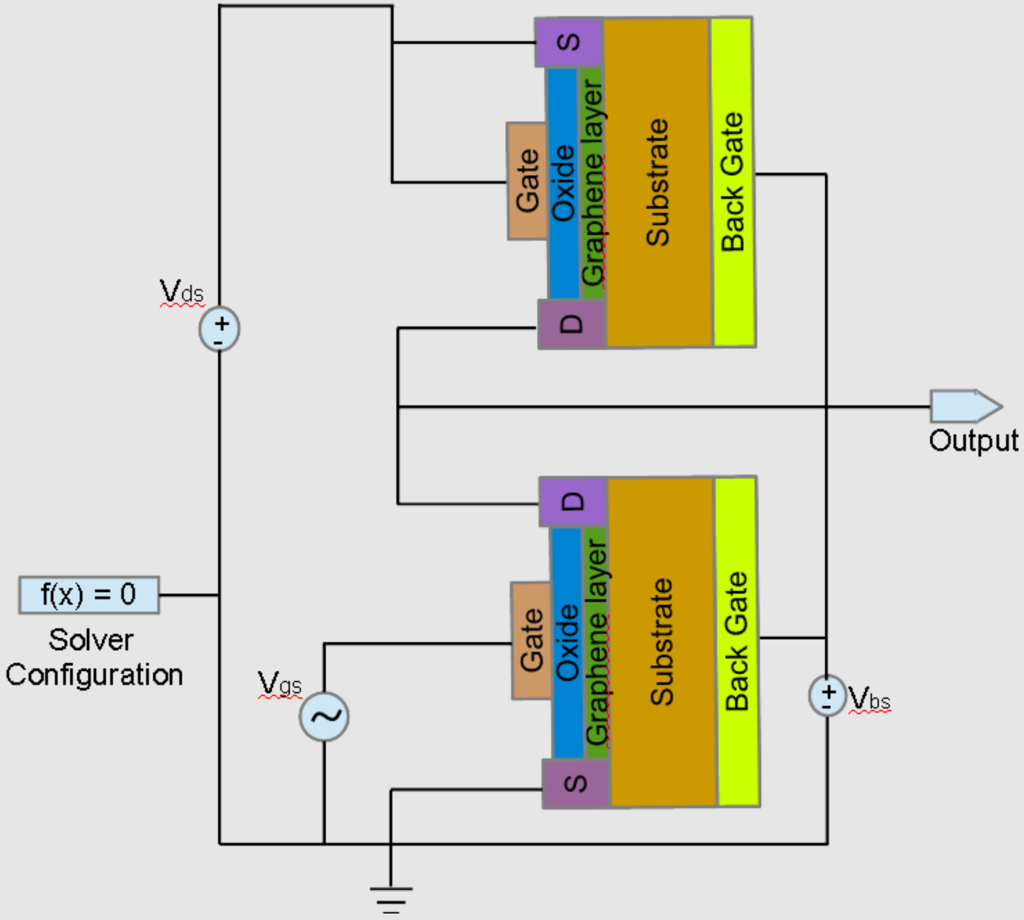
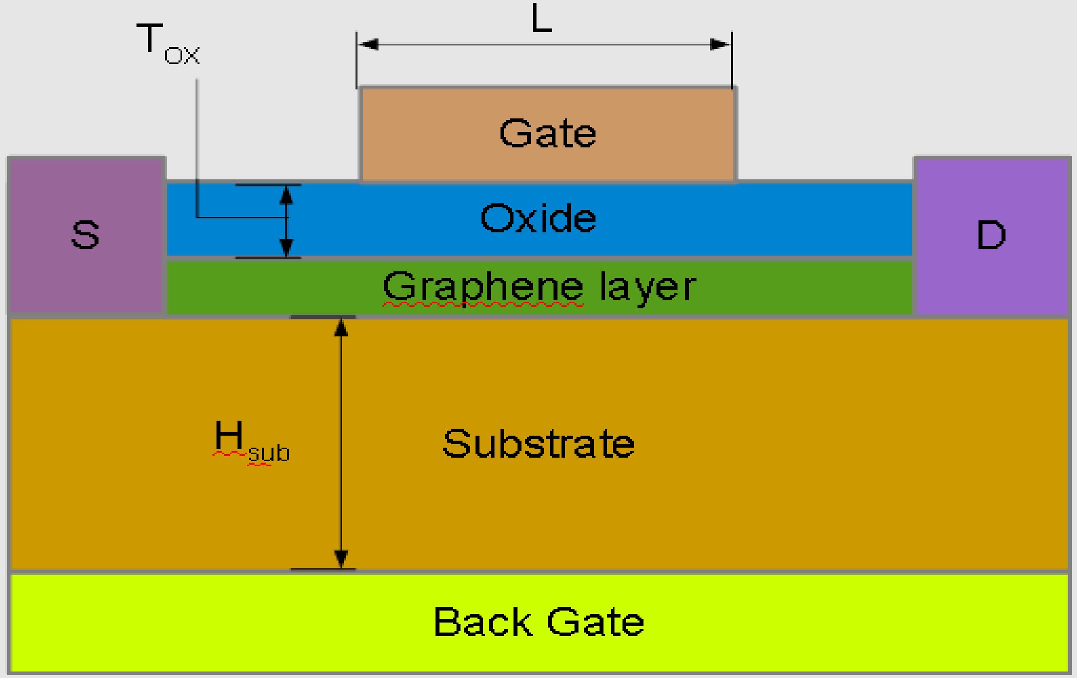


Fig. 5. Simscape® Experimental Setup for LNA modeling

Key Points:

- Solver configuration is needed
- Simulink-PS and PS-Simulink converter needed (for Simulink® Simuscape® block connection)

Simscape® modeling of the LNA



Parameters	Values	Values
W_1	20 nm	30 nm
W_2	10 nm	15 nm
Gain (G)	14.54 dB	15.41 dB
Bandwidth (f_T)	3.12 GHz	3.12 GHz
Power (P_{LNA})	23.8 mW	27.2 mW

Table 1. GFET based LNA FoMs

<u>Note</u> : T_{ox} = 1 nm
H_{sub} = 2.85 nm
L = 50 nm

Simulation Results

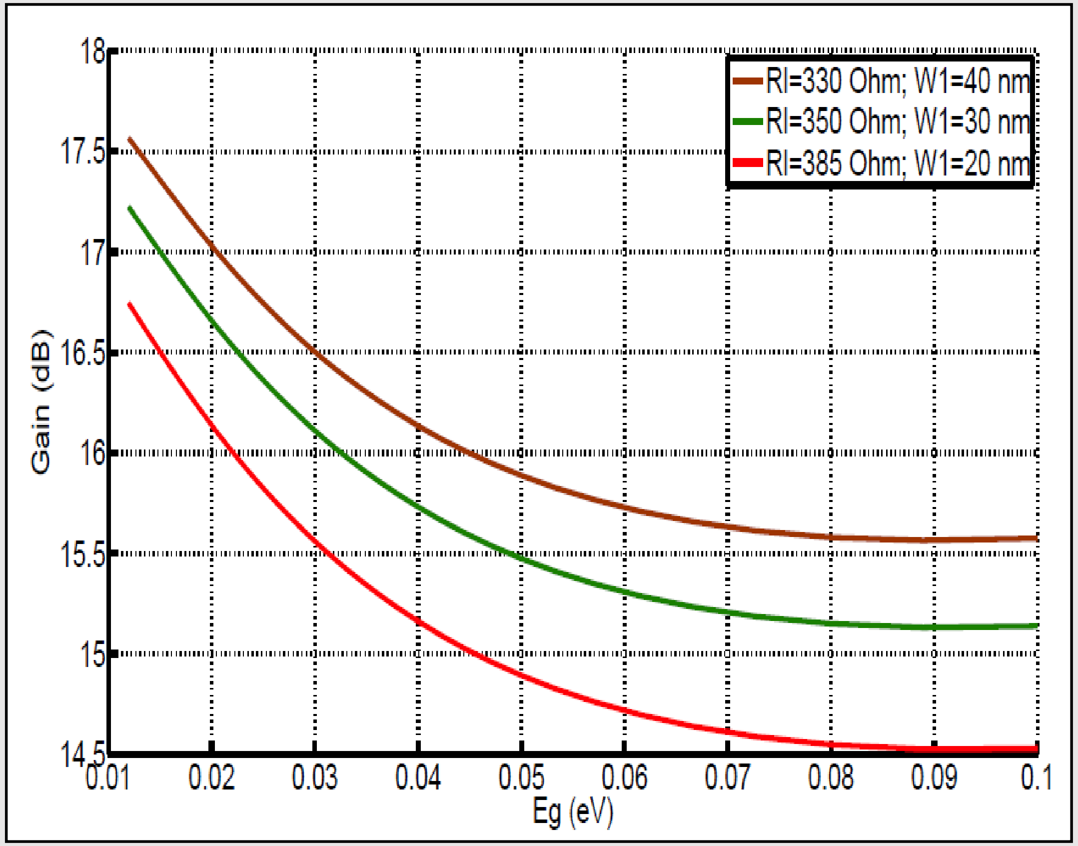


Fig. 6. Gain (G) vs E_g for different loads (R_L)

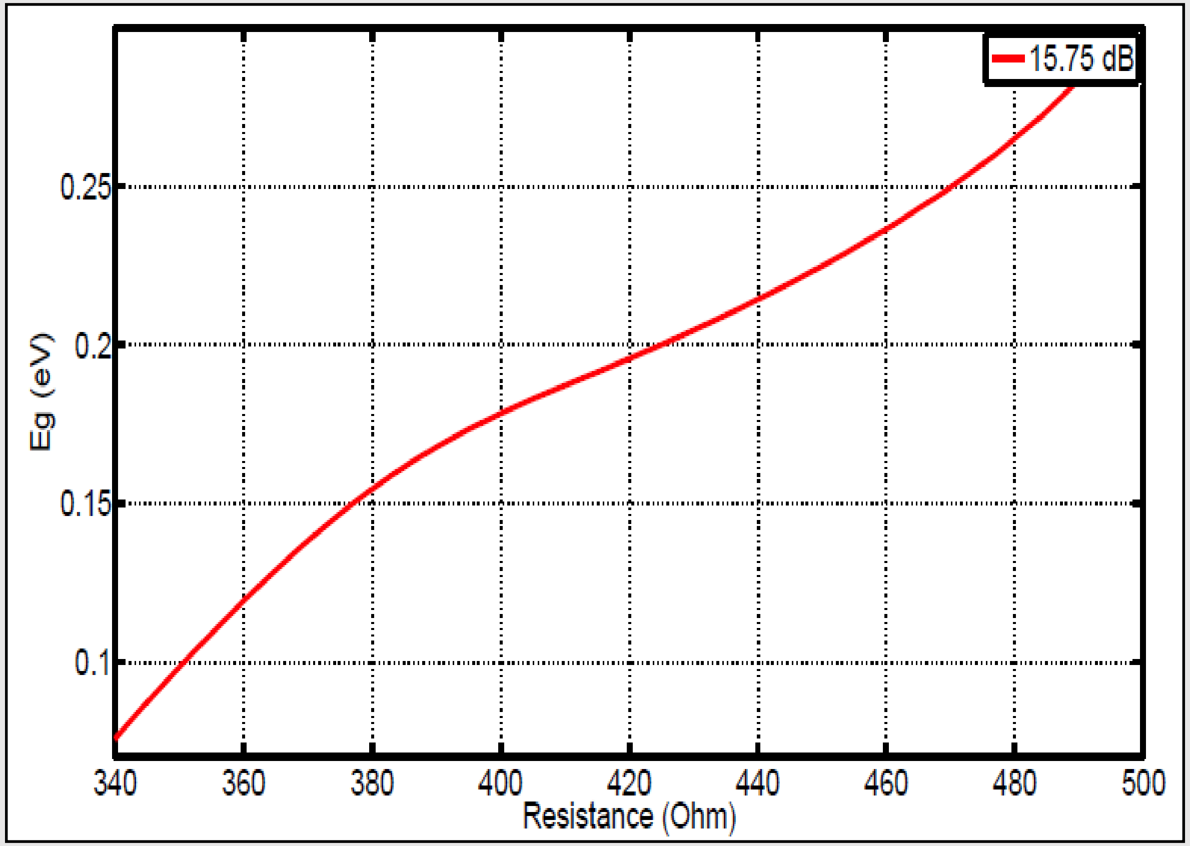


Fig. 7. E_g vs R_L at constant G = 15.75 dB

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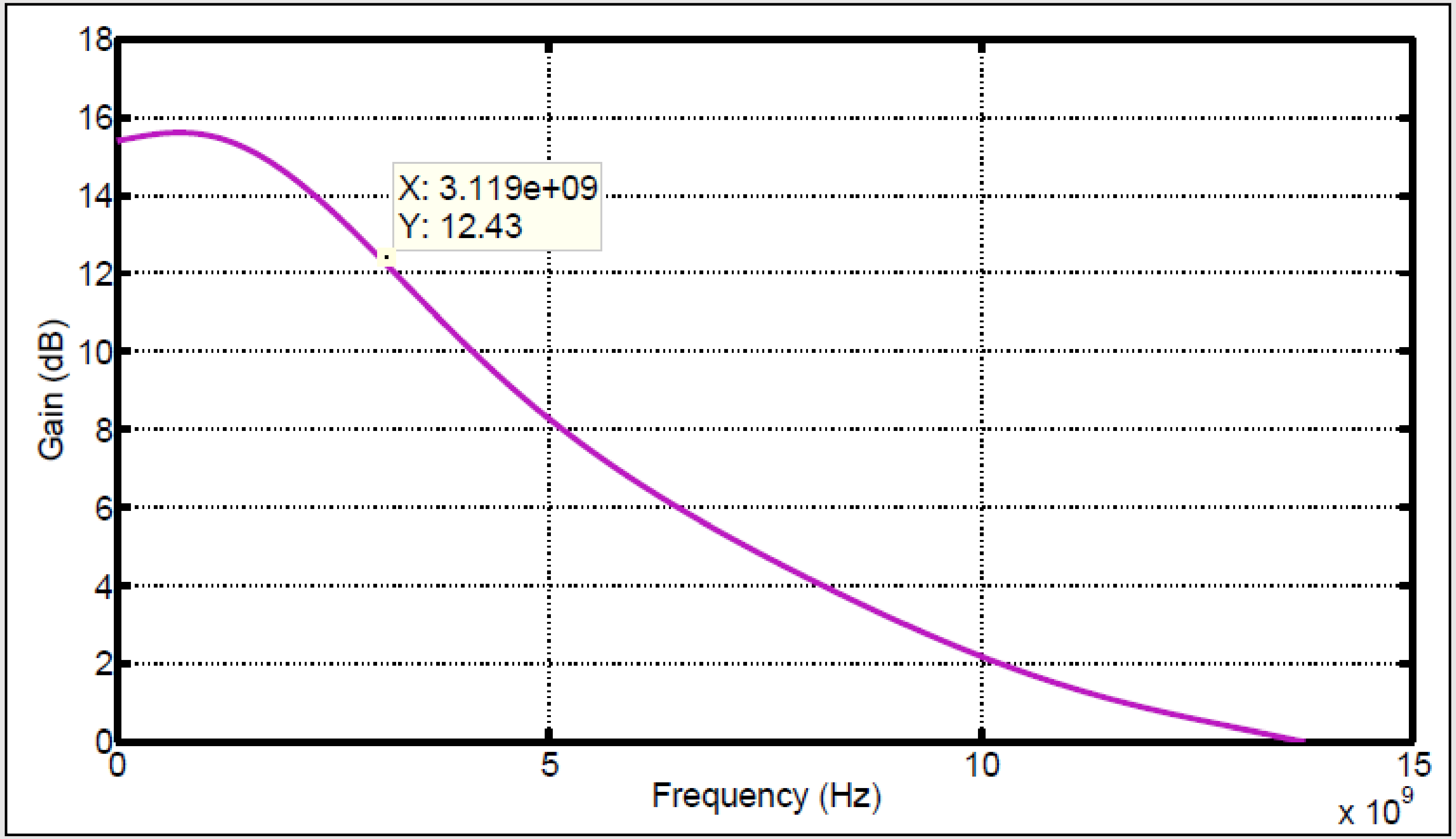

Fig. 8. Simulated frequency characteristic of GFET based LNA

Comparison with Results from [Das, 2011]

- The result in Fig. 6 shows the inverse relationship between the band-gap and gain as given in [Das, 2011].

- Similar result is obtained in Fig. 7 for bandwidth vs load resistance at a constant gain G = 15.75 dB.

S. Das and J. Appenzeller, "An All-graphene Radio Frequency Low Noise Amplifier," in Proceedings of the IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2011, pp. 1–4

Conclusions and Directions for Future Research

- Results show that Simscape® based models can be a substitute for EDA based models for exploratory design.
- As a future research, additional functionality for noise, transfer function and non-linear RF analyses such as periodic and quasi-periodic steady state can be incorporated within the Simscape® model.
- Particle swarm-based optimization (PSO) algorithms such as artificial bee colony and ant colony optimization for GFET based circuits will be explored within MATLAB® /Simscape® .

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Thank you !!!