Multi-Swarm Optimization of a Graphene FET Based Voltage Controlled Oscillator Circuit

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Introduction

- CMOS suffer a fundamental limit beyond 10 nm technology.
  - Non scalability of
    - Thermal voltage
    - Threshold voltage
    - Supply voltage

- Beyond 10 nm node, graphene is a viable solution
  - High field-effect mobility (>15000 $cm^2/V\ s$)
  - High Fermi velocity (10^8 cm/s)

Related Prior Research

- Graphene based devices
  - LNA [4],
  - Mixer [5],
  - High frequency graphene amplifier [6],
  - Frequency doubler [7]
  - LC-VCO [8]
- Various optimization techniques for analog circuits
  - Swarm optimization[9],
  - Bee colony optimization [10], and
  - Simulated annealing[11]

Novel Contributions

- ❑First attempt to propose a design flow for GFET based cross coupled version of an LC oscillator.

- ❑A new optimization algorithm called multi-swarm optimization (MSO) is used in the design flow

- ❑Gives proper sizing of the GFET device to achieve maximum frequency.

Design and Characterization of a Graphene LC-VCO

Device Parameters	Default Values
μ (Mobility)	0.3 m^2/Vs
Length	6.0 μm
Width	1.6 μm
R_s (p-channel)	600 Ω
R_s (n-channel)	4000 Ω
V_{supply}	9 V
I_{bias}	0.7 mA

Table 1. GFET Device Parameters

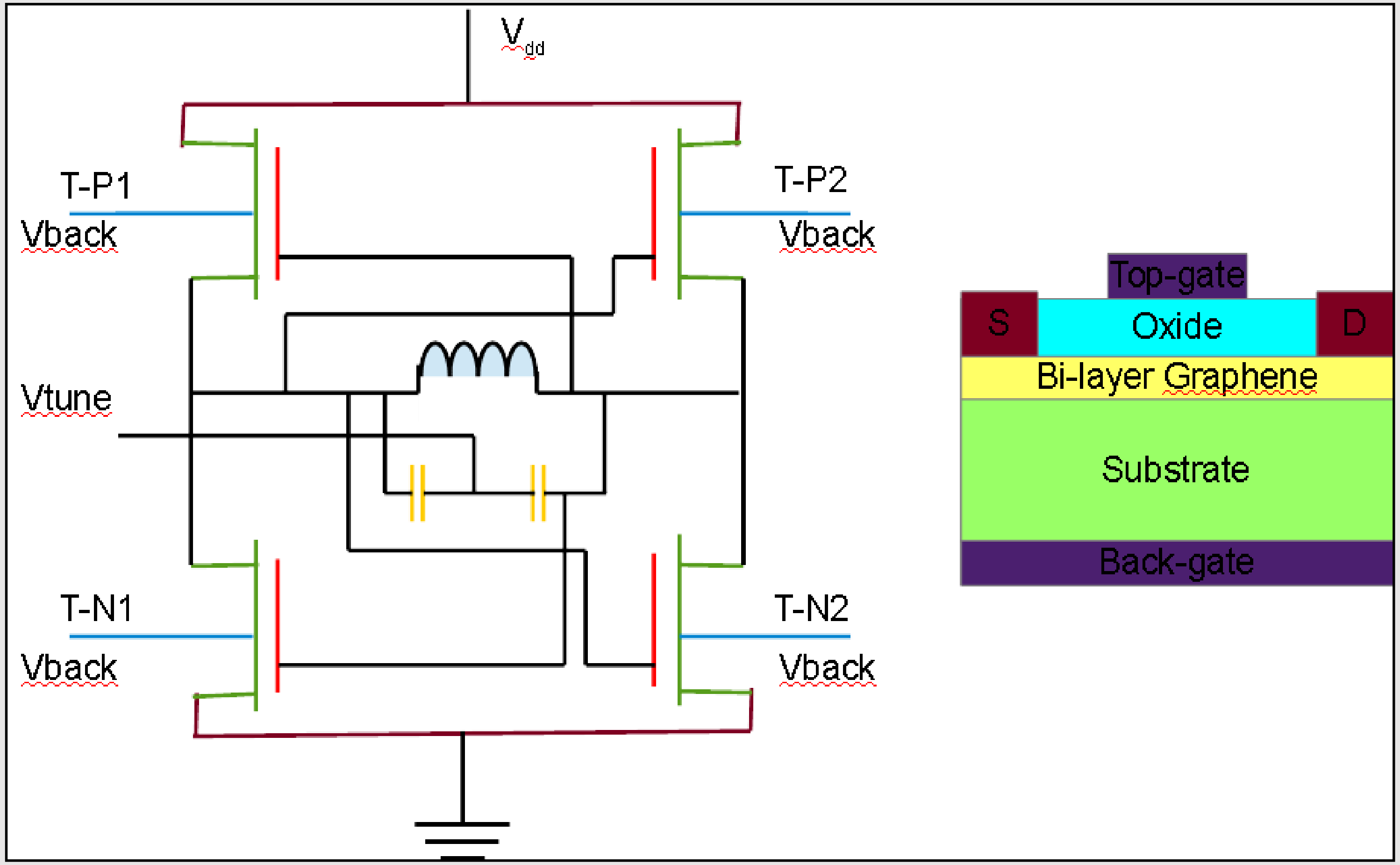
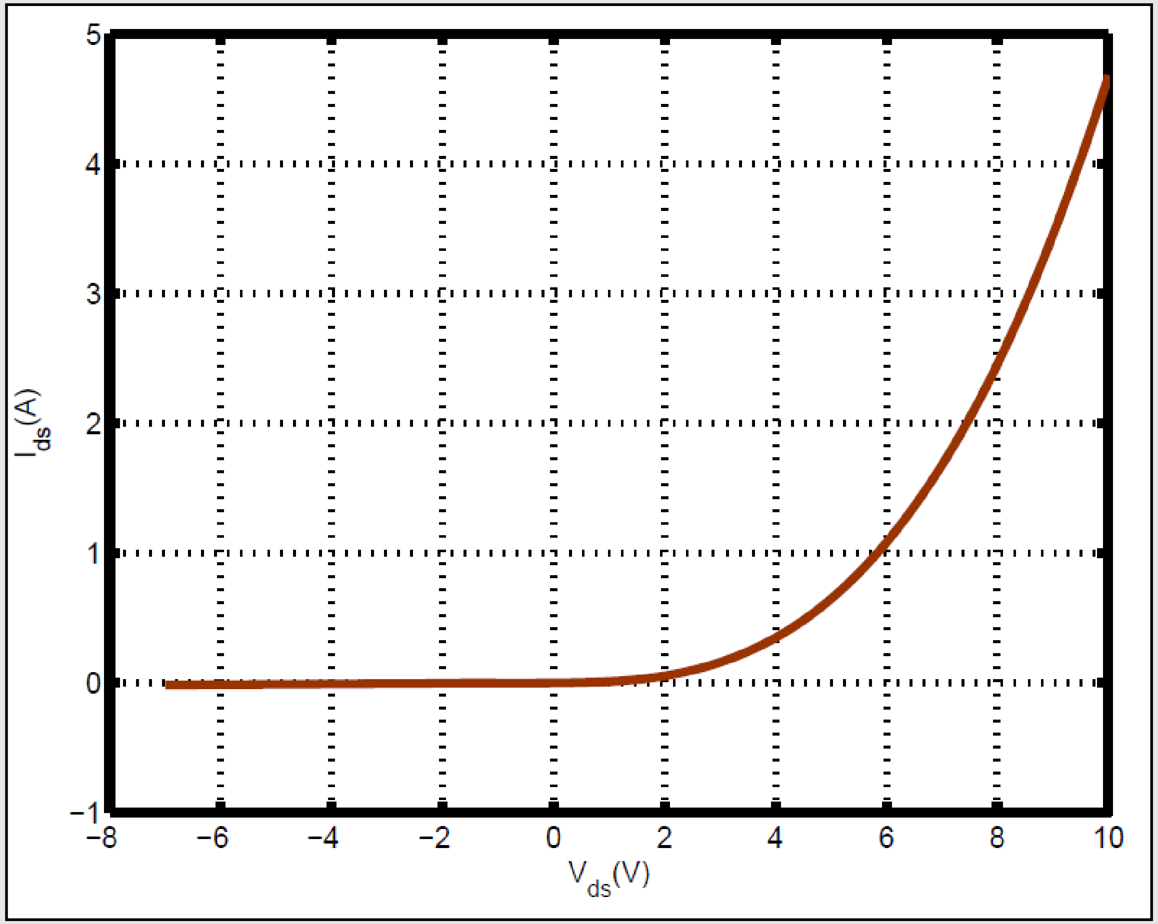


Fig. 1. GFET based LC-VCO with GFET-2D cross-section (left)

I-V Curves



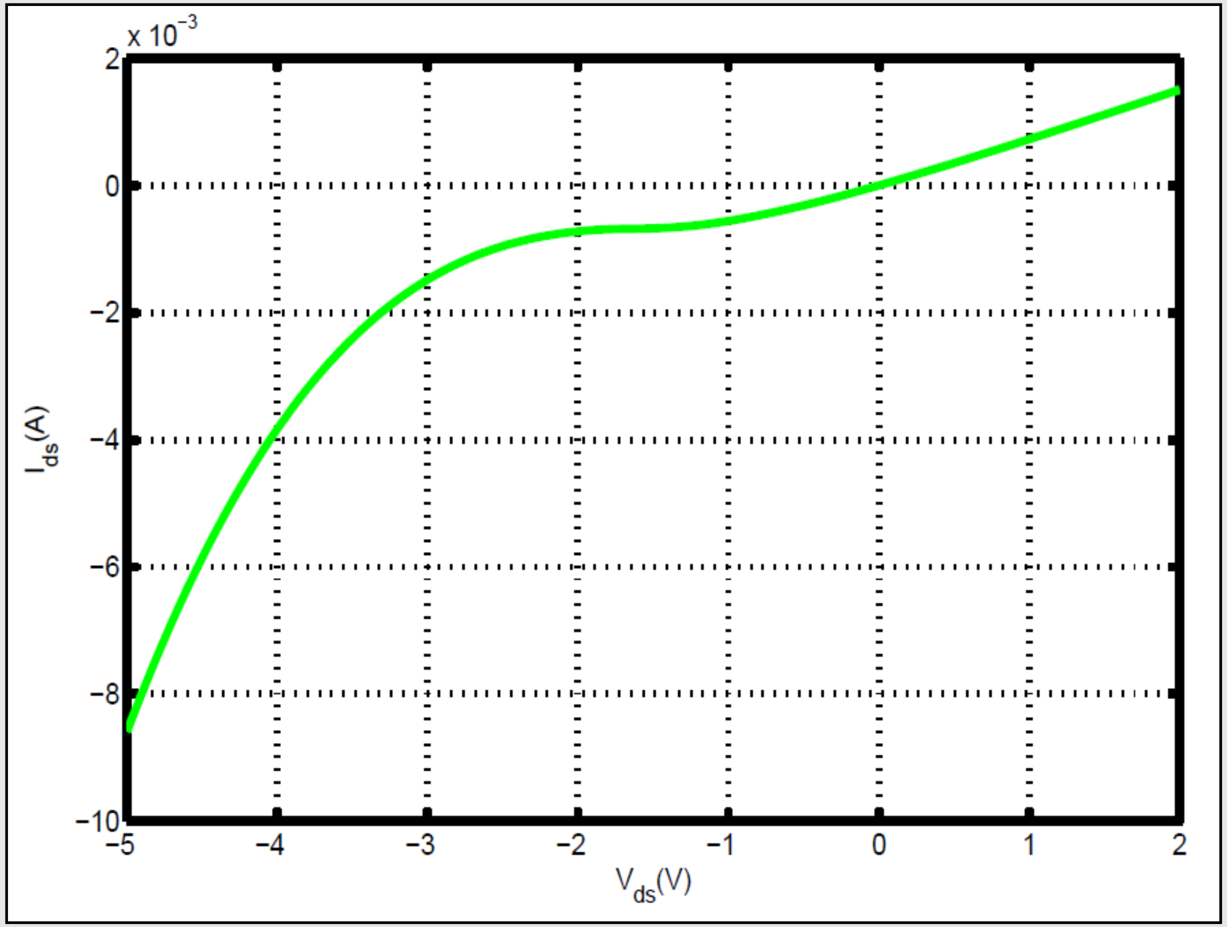
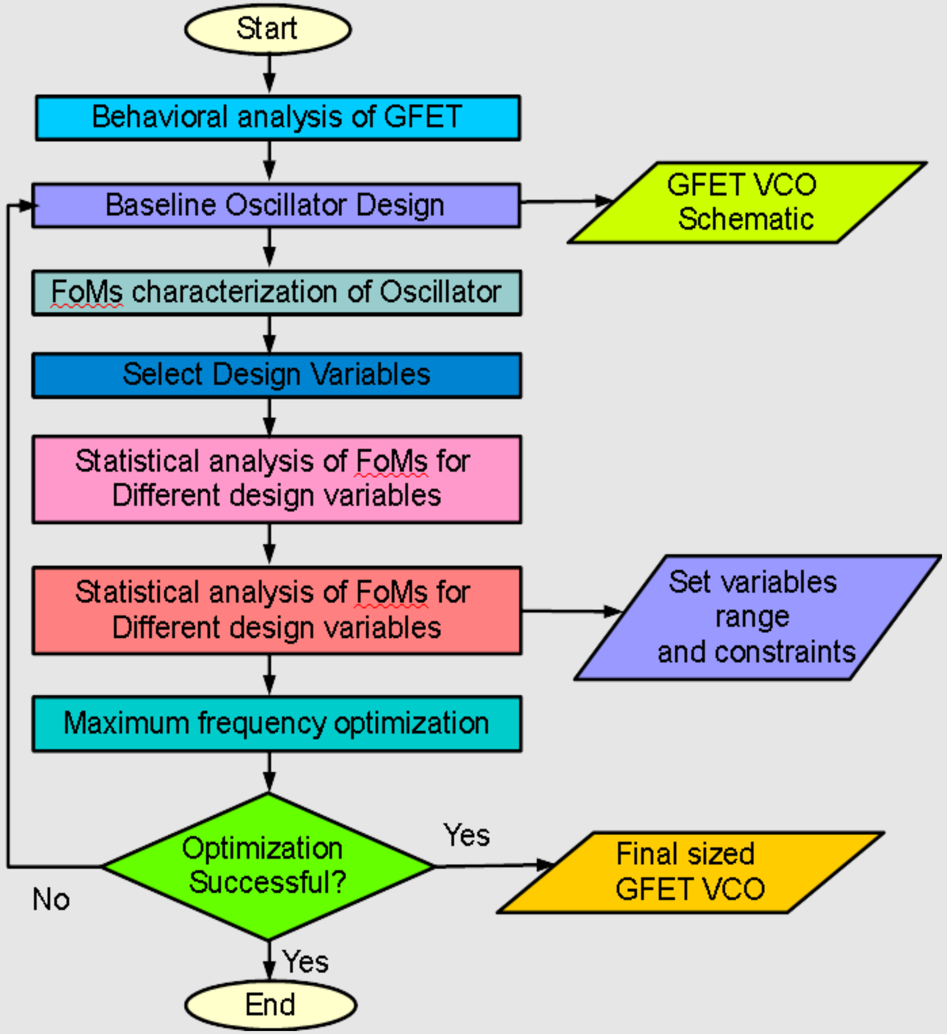


Fig. 2. I-V Curve of N-type and P-type GFET around operating region

Proposed Design Optimization flow for GFET Based LC-VCO

LC-VCO Characteristics	Estimated Values
f_{center}	2.56 GHz
$V_{tank,p\text{-}p}$	0.8 V
I_{bias}	0.77 mA
Tuning Range	4.88%
Phase Noise (1 MHz offset)	-88.25 dBc/Hz

Table 2. Baseline GFET based LC-VCO



Tuning Range and Phase Noise

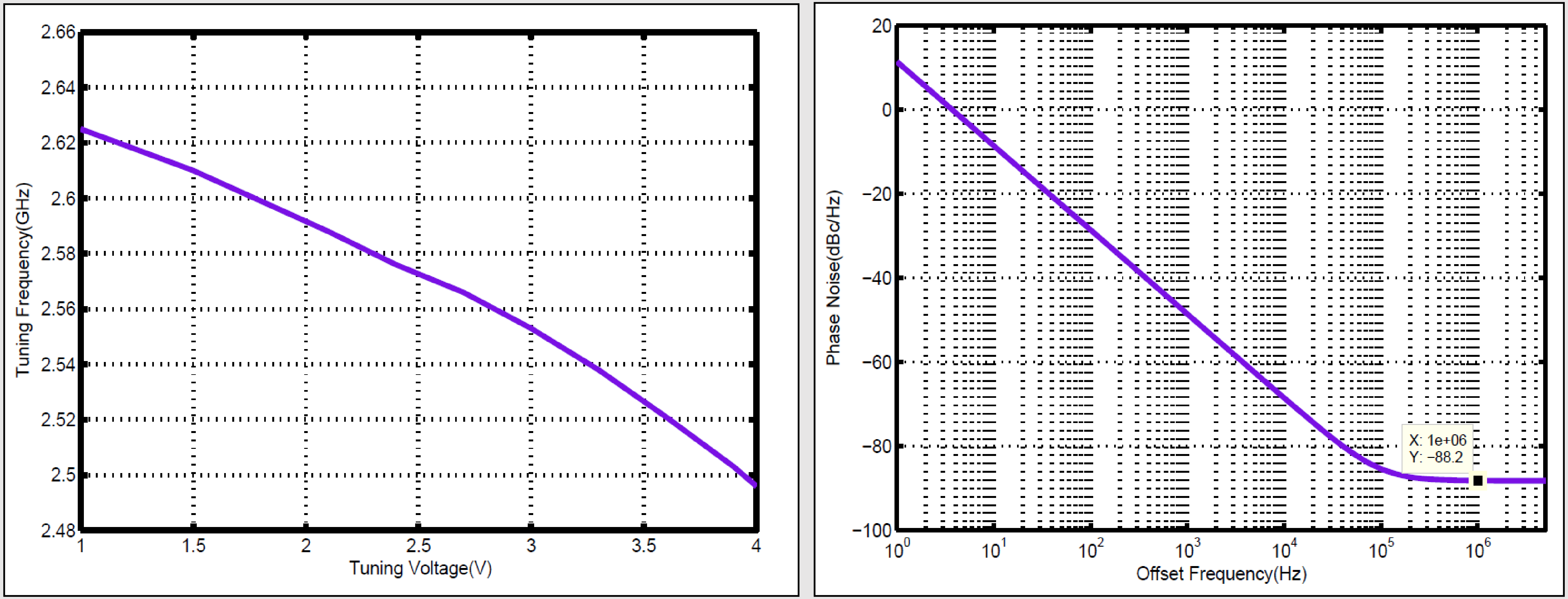
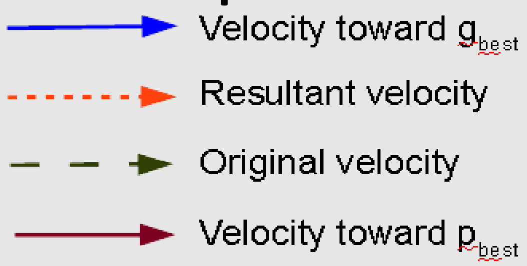


Fig. 3. Tuning range and Phase noise Characteristics of the baseline GFET based LC-VCO

Multi Swarm Optimization (MSO) Technique

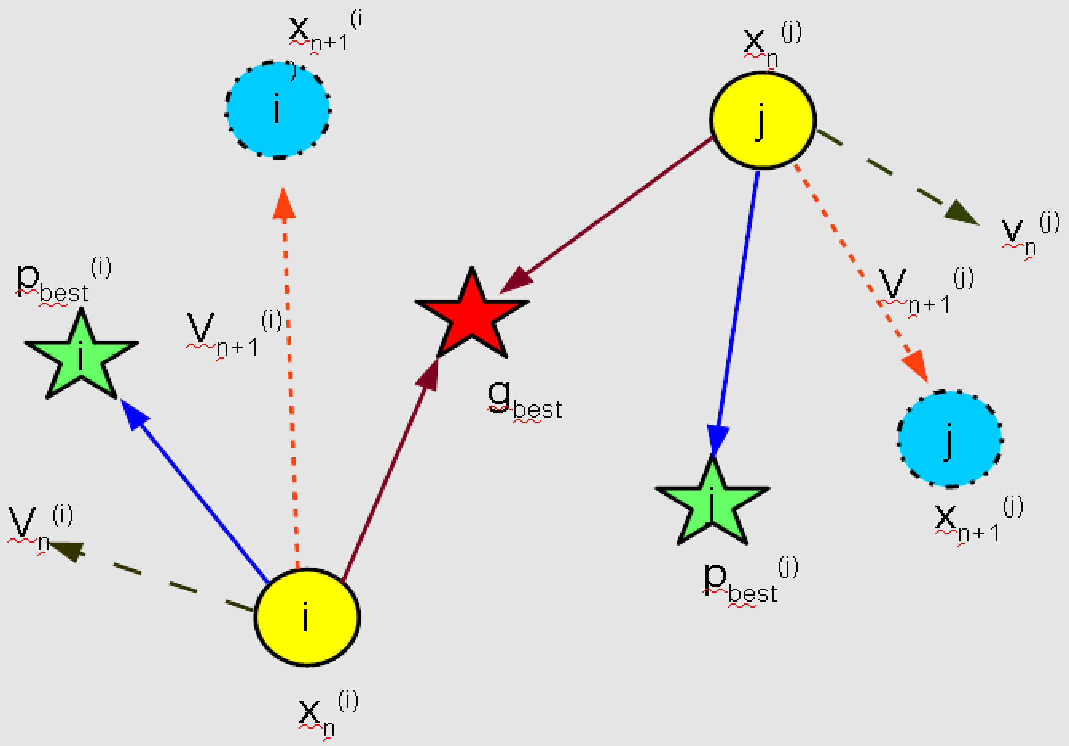


- Particle velocity update:

$$v_{t+1} = wv_t + c_1r_1(x_i - p_{best}) + c_2r_2(x_i - s_{best}) + c_3r_3(x_i - g_{best})$$

- Particle position update:

$$x_{t+1} = xi + vt_{+1}$$



Algorithm Parameters	Values
w	0.7 – 0.33
c_1, c_2, c_3	0.2

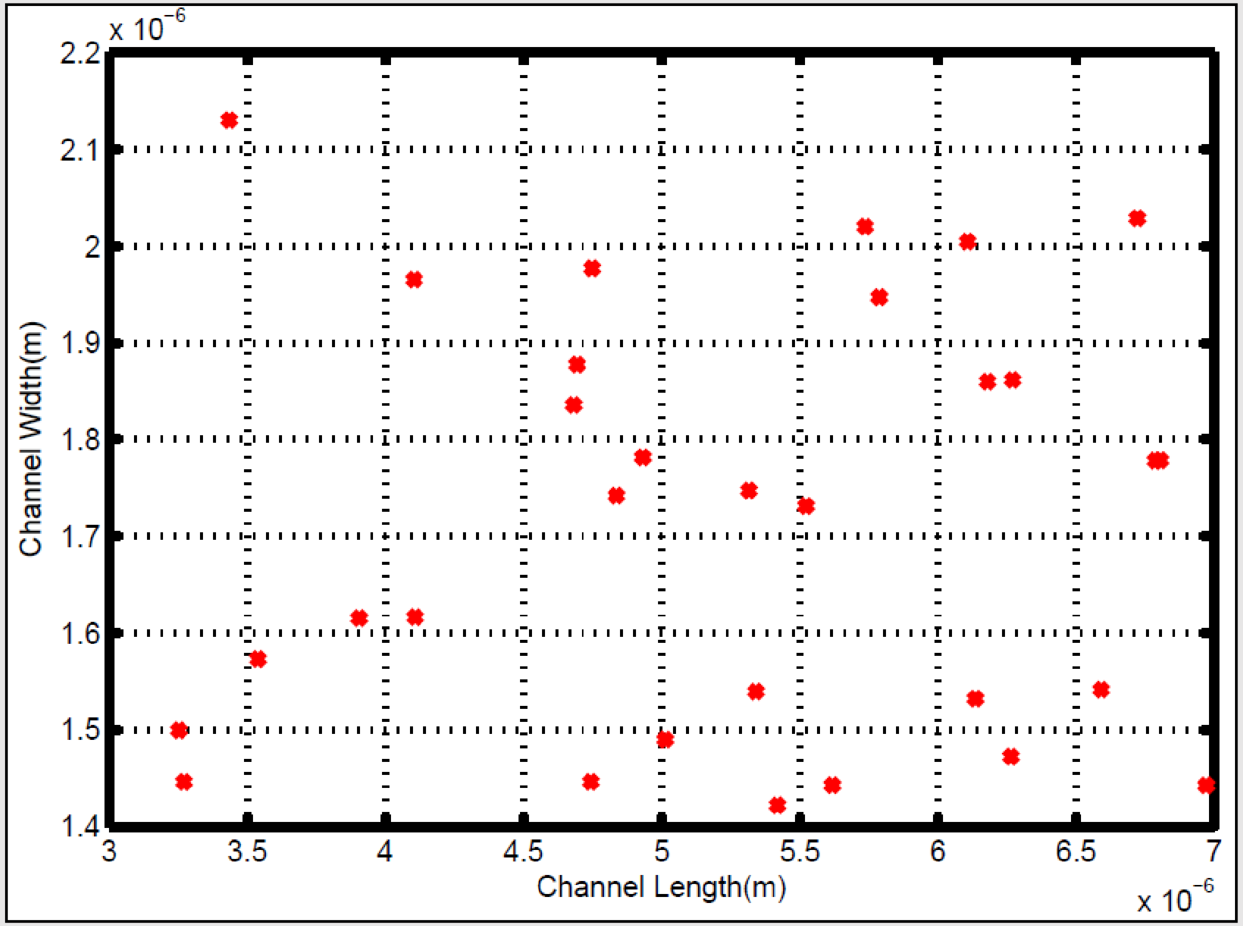
Table 3. MSO Algorithm Parameters

Continued…

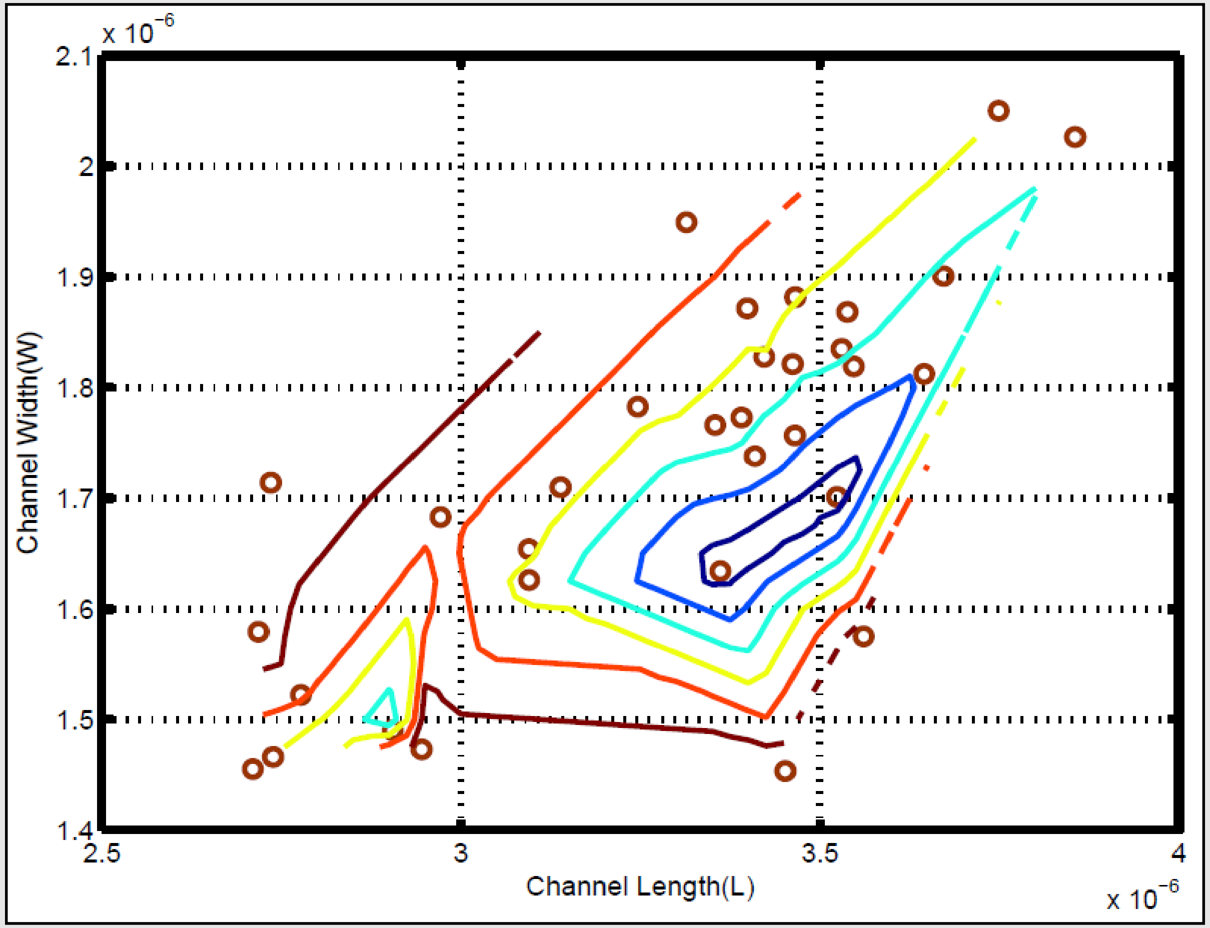
LC-VCO Parameters	Parameter Type	Minimum Value	Maximum Value
L	Design Variable	3 µm	7 µm
W	Design Variable	1.4 µm	2.2 µm
Power Dissipation	Design Constraint	Minimize	16 mW
Phase Noise	Design Constraint	Minimize	-80 dBc/Hz

Table 4. GFET based LC-VCO Design Variable and Constraints

Continued…



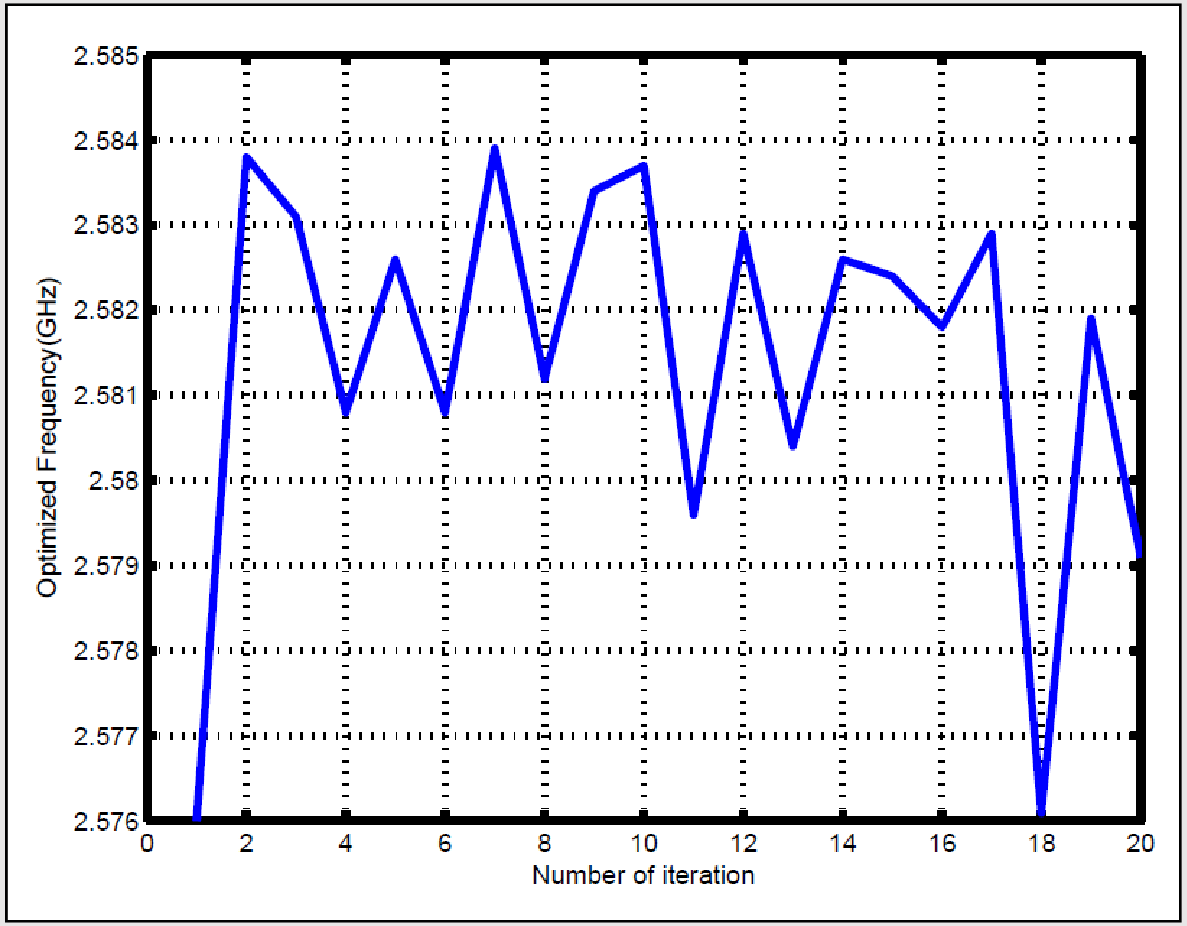
(a) Initial Particles, x



(b) Particles after 20th iteration

Fig. 4. GFET based LC-VCO Optimization

Optimized Frequency



(c) Optimized Frequency

Fig. 4. GFET based LC-VCO Optimization (Continued…)

Experimental Results – Quality Factor

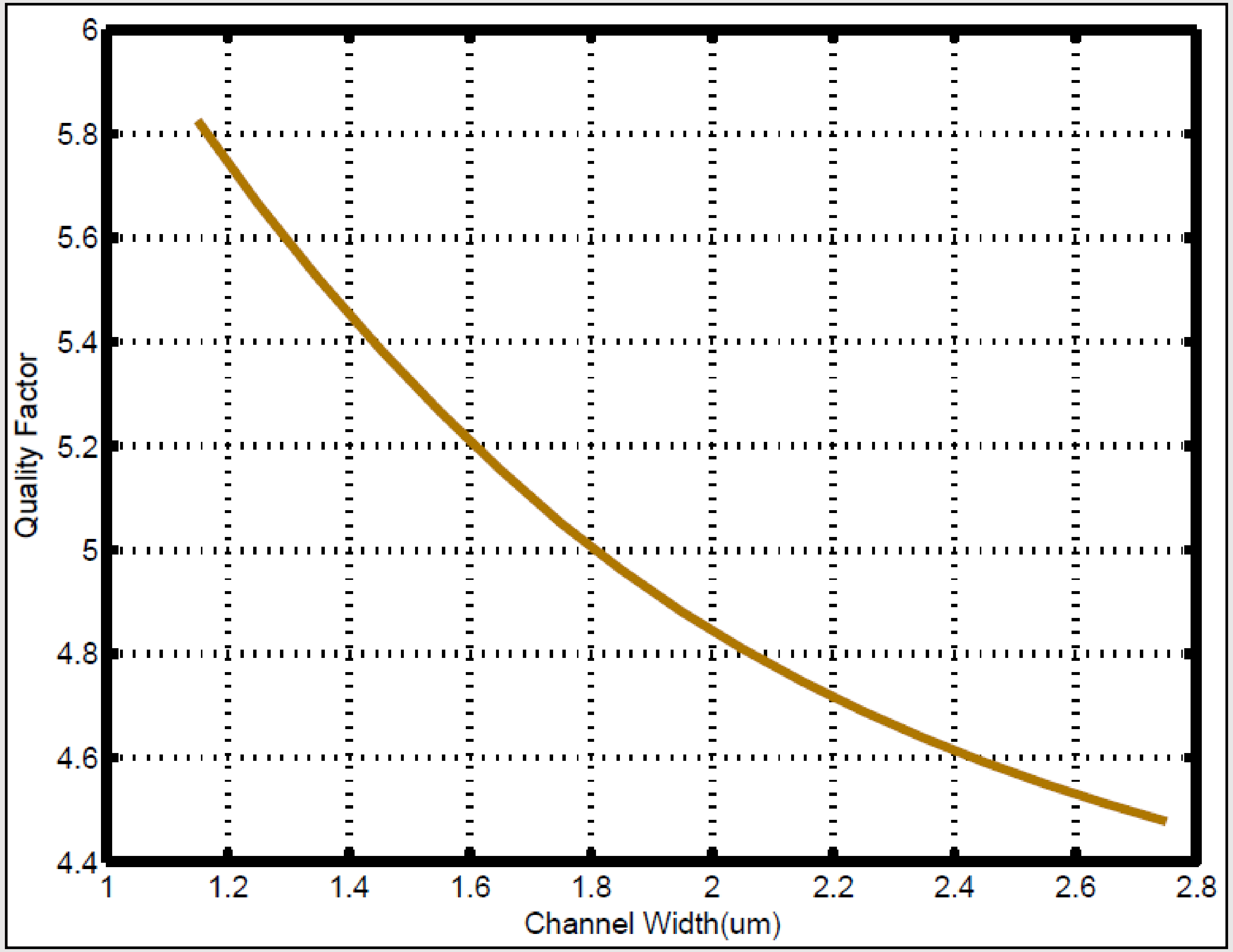


Fig. 5. Quality Factor of the GFET based LC-VCO

Frequency vs. length and width

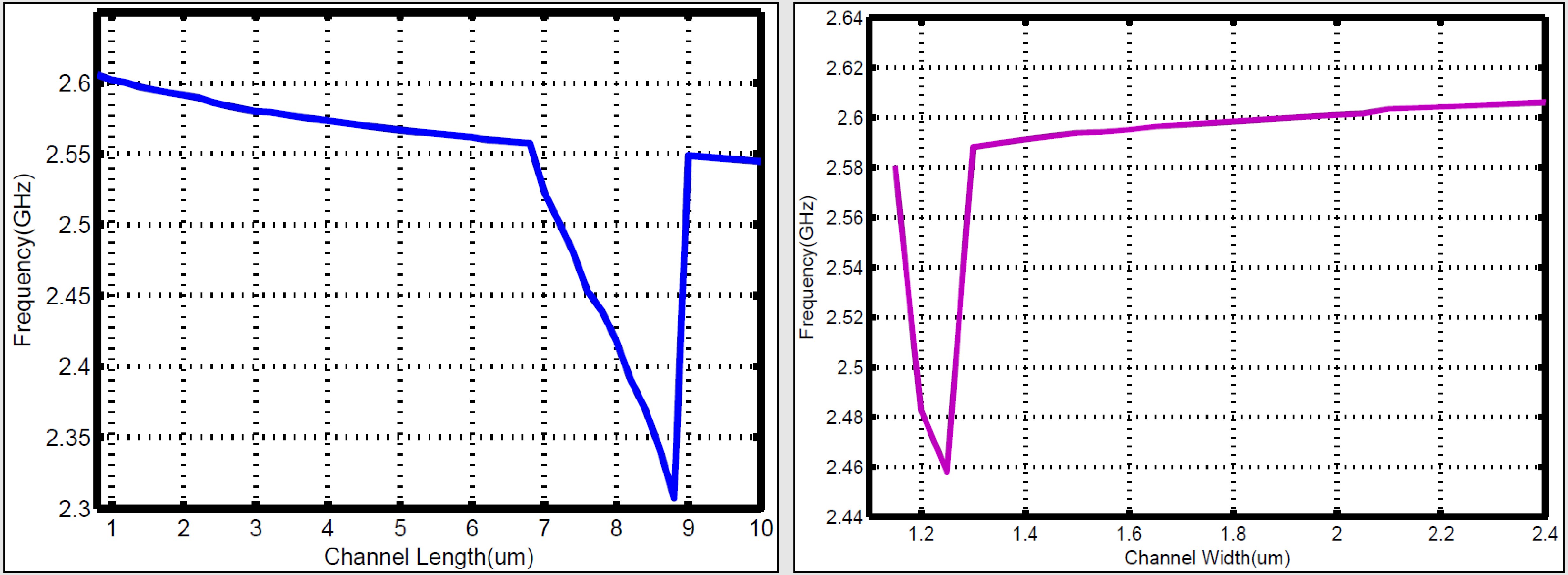


Fig. 6. Frequency of the GFET based LC-VCO vs Channel length and Channel width

Power dissipation vs. length and width

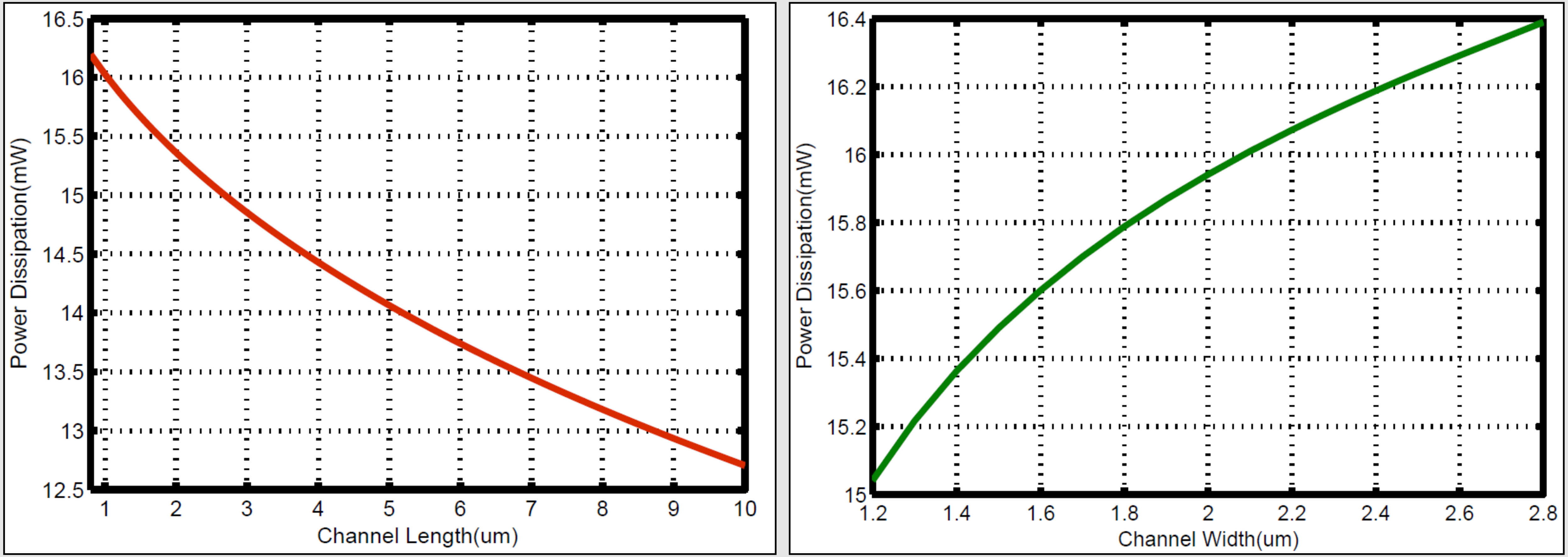


Fig. 7. Power Dissipation of the GFET based LC-VCO vs Channel length and Channel width

Phase Noise vs. length and width

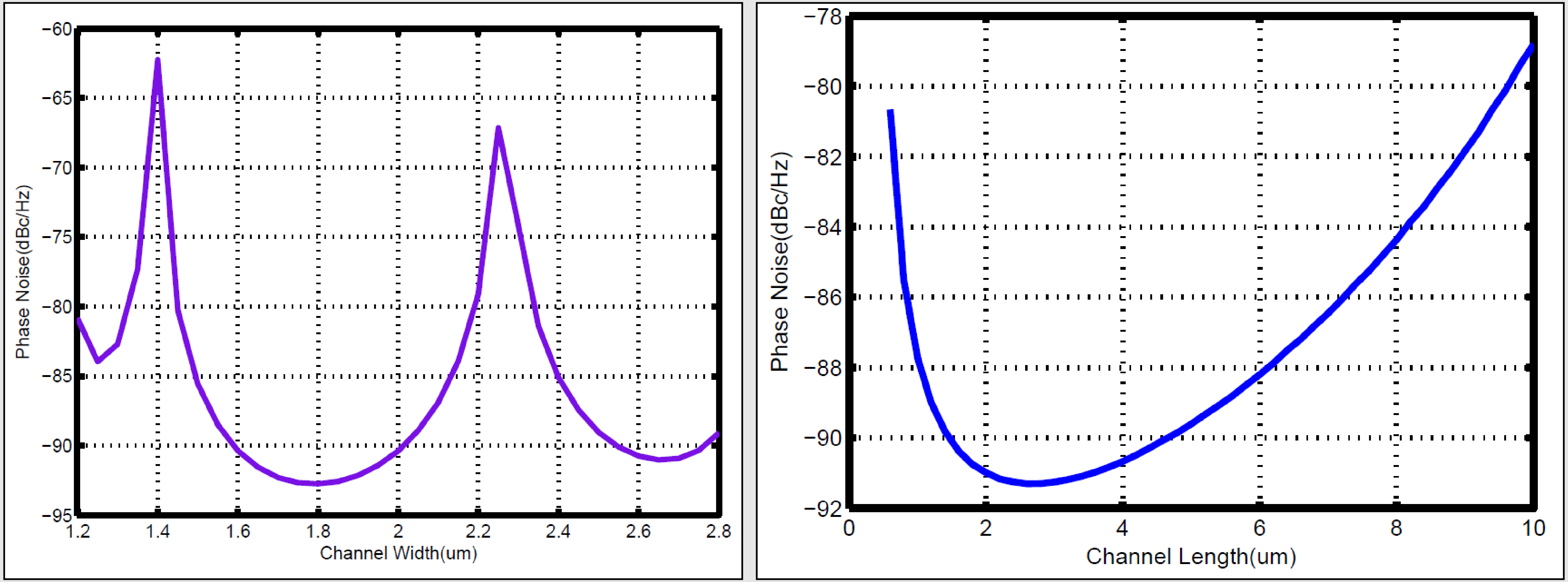
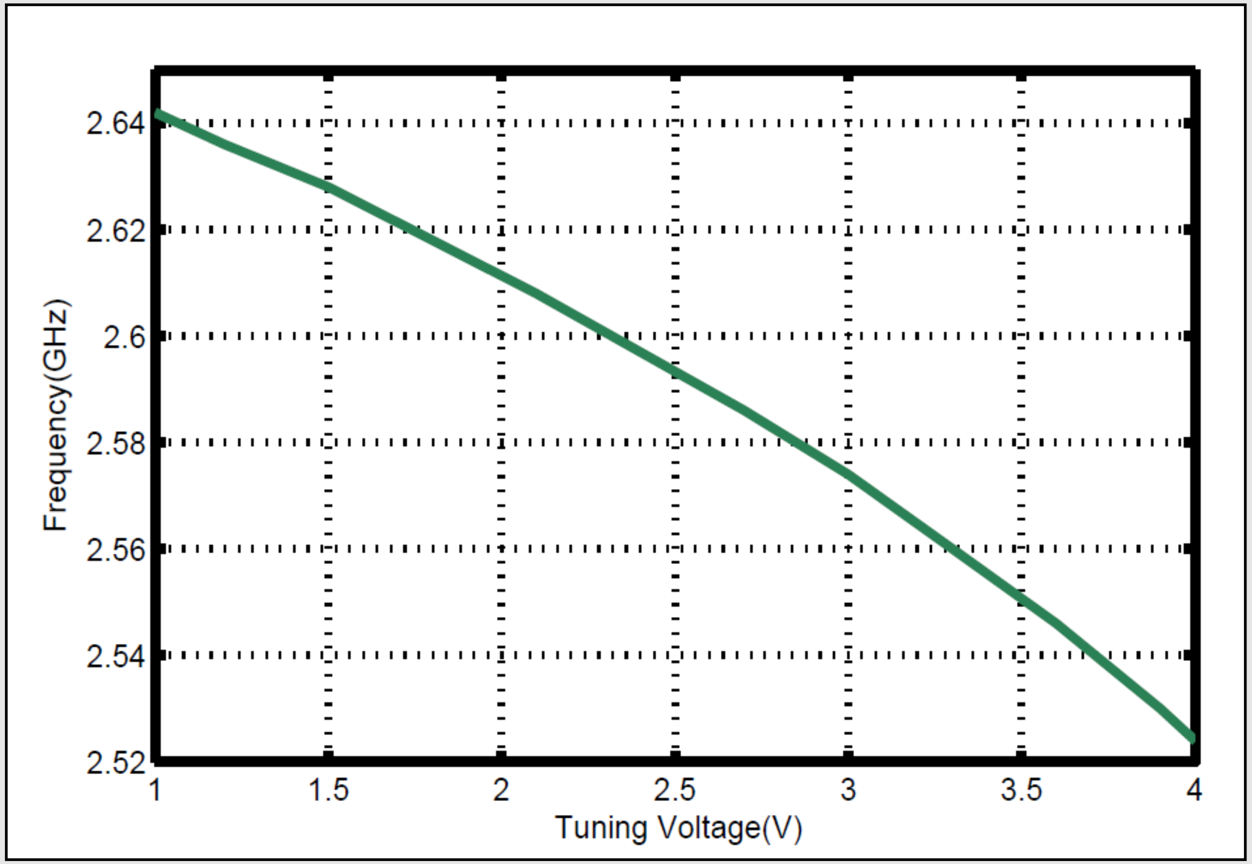


Fig. 8. Phase Noise of the GFET based LC-VCO vs Channel length and Channel width

Optimized response



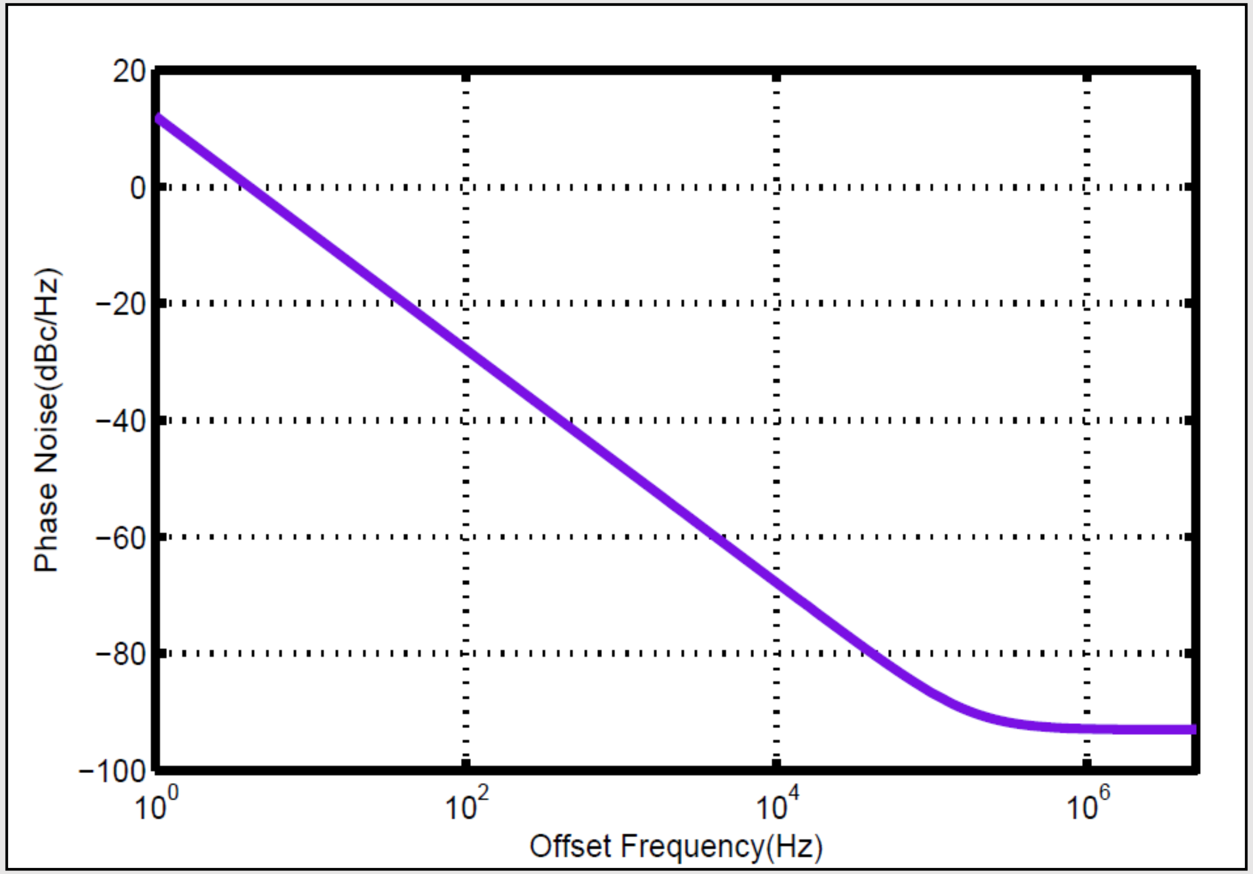


Fig. 9. Tuning Range and Phase Noise of Optimized GFET based LC-VCO

Optimal GFET based LC-VCO

LC-VCO Parameters	Obtained Values	Remarks
Channel Length	3.35 µm	3 – 7 µm
Channel Width	1.82 µm	1.4 - 2.2 µm
Power Dissipation	11.74 mW	Max. 16 mW
Phase Noise (1 MHz offset)	-92.92 dBc/Hz	Max. -80 dBc/Hz
Frequency	2.58 GHz	2.56 GHz
Tuning Range	4.62%	
$V_{tank,p-p}$	0.75 V	
I_{bias}	0.83 mA	

Optimization Variables (Channel Length, Channel Width)

Optimization Constraints (Power Dissipation, Phase Noise)

Initially Designed (Frequency)

Table 5. Characteristics of the Optimal LC-VCO

Conclusions and Directions for Future Research

- Design constraints of phase noise and power dissipation are well met.
- The power dissipation and phase noise are 26.6% and 16.2% below their maximum values.
- As a future work, a surrogate model of the circuit will be created which will then be used to perform optimization instead of using a netlist.
- Parasitic aware design and multi-objective optimization will be performed to obtain the final layout.

References

1. I. J. Umoh and T. J. Kazmierski, "VHDL-AMS model of a dual gate graphene FET," in Forum on Specification and Design Languages (FDL), 2011, pp. 1–5.
2. F. Schwierz, "Graphene transistors," Nature Nanotechnology, vol. 5, pp. 487–496, May 2010.
3. K. S. Novoselov, A. K. Geim, S. V. Morozov, D. Jiang, Y. Zhang, S. V. Dubonos, I. V. Grigorieva, and A. A. Firsov, "Electric Field Effect in Atomically Thin Carbon Films," Science, vol. 306, no. 5696, pp. 666–669, 2004.
4. S. Das and J. Appenzeller, "An All-Graphene Radio Frequency Low Noise Amplifier," in Proceedings of IEEE Radio Frequency Integrated Circuits Symposium (RFIC), 2011, pp. 1–4.

Continued…

5. H. Wang, A. Hsu, J. Wu, J. Kong, and T. Palacios, "Graphene-Based Ambipolar RF Mixers," IEEE Electron Device Letters, vol. 31, no. 9, pp. 906–908, 2010.
6. S. J. Han, K. A. Jenkins, A. Valdes Garcia, A. D. Franklin, A. A. Bol, and W. Haensch, "High-Frequency Graphene Voltage Amplifier," NanoLetters, vol. 11, no. 9, pp. 3690–3693, 2011.
7. M. E. Ramon, K. N. Parrish, S. F. Chowdhury, C. W. Magnuson, H. C. P. Movva, R. S. Ruoff, S. K. Banerjee, and D. Akinwande, "Three- Gigahertz Graphene Frequency Doubler on Quartz Operating Beyond the Transit Frequency," IEEE Transactions on Nanotechnology, vol. 11,no. 5, pp. 877–883, sept. 2012.
8. M. A. Khan, S. P. Mohanty, and E. Kougianos, "Statistical Process Variation Analysis of a Graphene FET based LC-VCO for WLAN Applications," in Proceedings of the 15th International Symposium on Quality Electronic Design, 2014, pp. 569–574.

Continued…

9. M. fakhfakh, Y. Cooren, A. Sallem, M. Loulou and P. Siarry, "Analog Circuit Design Optimization Through The Particle Swarm Optimization technique", Analog Integrated Circuits and Signal Processing, vol. 63, no. 1, pp. 71-82, April 2010.
10. O. Garitselov, S. P. Mohanty and E. Kougianos, "Accurate polynomial metamodeling-based ultra-fast bee colony optimization of a nano-cmos phase-locked loop", Journal of Low Power Electronics, vol. 8, pp. 317-328, 2012.
11. G. G. E. Gielen, H. C. C. Walsch and W. M. C. Sansen, "Analog Circuit Design Optimization Based on Symbolic Simulation and Simulated Annealing", IEEE Journal of Solid-State Circuits, vol. 25, pp. 707-713, 1990.

Thank you !!!