An Algorithm Used in a Power Monitor to Mitigate Dark Silicon on VLSI Chip

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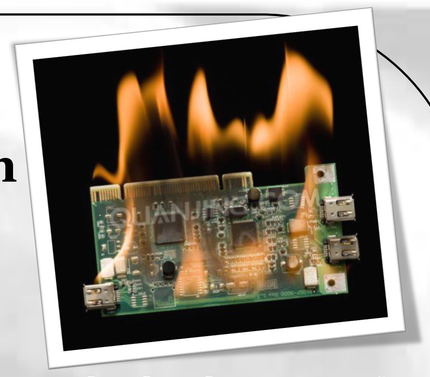
Introduction



❖ Background

- Down scaling of transistors promotes high density of transistors in a microprocessor design.
- Meanwhile, clock frequency and required bandwidth LAN have significantly increased due to the development of advanced communication technology.
- Dark silicon, which refers to a part of transistors in a chip with lower work frequency due to the limitations of cooling technique, has increased in a chip. Especially, in advanced multiple-core microprocessors, dark silicon largely occupies the entire chip and seriously influences work performance of processors.
- It can be anticipated that dark silicon will become larger in chip if there is no novel processor topology to implement as well as state-of-art circuit invented.
- Even worse, dark silicon might result in failure of MOS scaling technology.

❖ Existing Works

- Use of a power switch to deliver more current for single core with the purpose of improving performance at the cost of increasing low power consumption.
- Setting power wire with additional switches to work in two modes including traditional power mode and data mode.
- A "greendroid" concept to solve dark silicon issue for Android smartphones.

Major Contributions of Our Paper

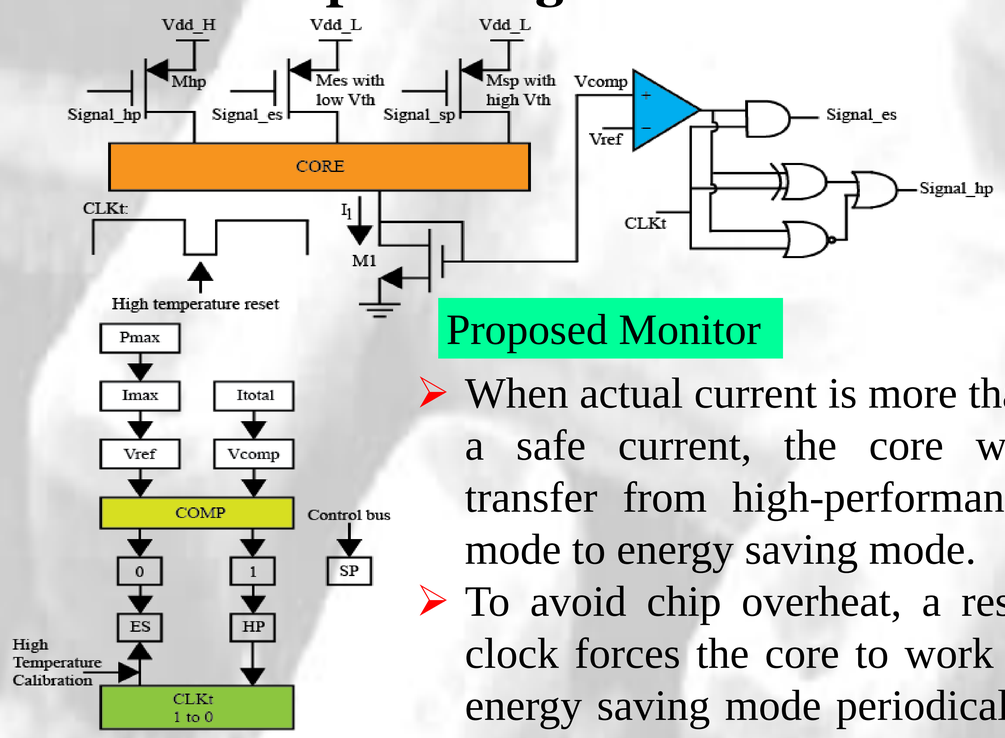
- We quantitatively analyzed power dissipation of VLSI chip and discuss the potential ways to reduce power dissipation without large frequency drop.
- A low cost power monitor and its algorithm are proposed to efficiently regulator chip power based on a voltage feedback system and a reset clock avoiding overheat for VLSI chips.
- A RC model is used to verify the effectiveness of the proposed power monitor.

Proposed Methodology

$$P_{total} = \frac{N_{work}}{N_{work} + N_{sleep}} C_{total} V_{dd}^2 f + \sum I_{leak} * V_{dd} + \sum R_{wire} I_{wire}^2$$

- Using above equation to find tradeoff between chip performance and power dissipation.
- Using feedback system to achieve real-time power monitoring and regulating.

Proposed Algorithm



Proposed Monitor

- When actual current is more than a safe current, the core will transfer from high-performance mode to energy saving mode.
- To avoid chip overheat, a reset clock forces the core to work in energy saving mode periodically ignoring the value of current.

Proposed Algorithm

- For the potential multiple-core working asynchronously, a sleep mode is added to reduce the power dissipation of those cores momentarily out of work.

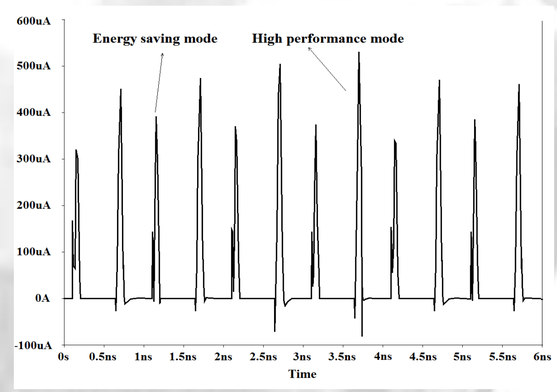
Experimental Results

Modeling Setup:

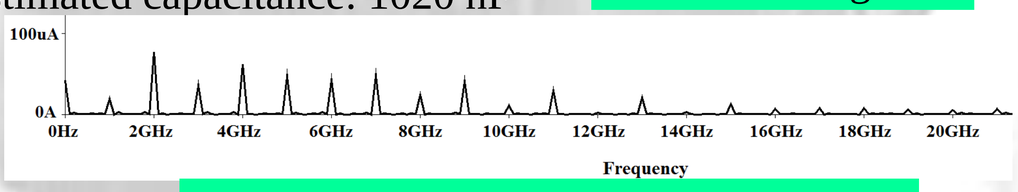
A virtual processor is created using a 16nm predictive transistor model trend in processors' performance. An RC model of a microprocessor with 4 cores is made.

Modeling Parameters:

Number of cores: 4
Supply voltage: 0.9V
Maximum current: 0.6mA
Clock frequency: 3GHz
Transistor Count: 90 million
Estimated resistance: 1500 Ω
Estimated capacitance: 1020 nF



Simulation of Mode Switching



Frequency response of switching process

In 1ns, high performance mode, energy saving mode and sleep mode last around 0.2ns, 0.2ns, and 0.5ns, respectively. The maximum frequency of switching work mode is 13GHz which is more than working clock.

Conclusions and Future Research

- Discussed power dissipation and tradeoff between power dissipation and performance.
- A low cost power monitor and its algorithm are proposed and a RC model is used to verify our idea.

Future work:

- Our group is working on designing a high performance microprocessor in submicron process with the proposed monitor and some other circuits in an attempt to mitigate dark silicon in VLSI chip.
- Designing some state-of-art gate-level circuits should be another way to light future VLSI chip.