Exploring Kriging for Fast and Accurate Design Optimization of Nanoscale Analog Circuits

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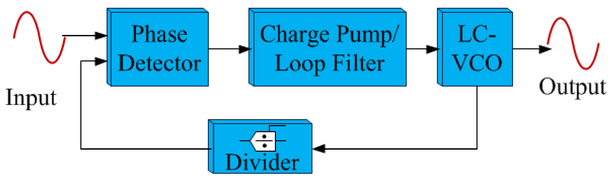
Abstract

Aggressive scaling of technology allows for the possibility of more system components to be integrated on a single chip. The design of such systems however constitutes a significant challenge, with increasing numbers of parameters making efficient exploration of the design space a burden. A prominent issue in designs deep in the nanometer range is including the effects of process variation. Conventional synthesis methods use computationally expensive SPICE simulations. Metamodeling techniques abstract the expensive simulation times by providing fast access to the design space with an approximation of the transistor-level response of the circuit. Current metamodeling techniques are however unable to model the effects of process correlations. Kriging based techniques use effective weighting that utilizes the correlation between parameters and can be modeled to capture process variation. This work explores Kriging for the fast and accurate design optimization of nanoscale AMSSoCs. An illustration with a 180nm PLL designs shows a reduction in power dissipation by 79% while reducing simulation time by about 25x.

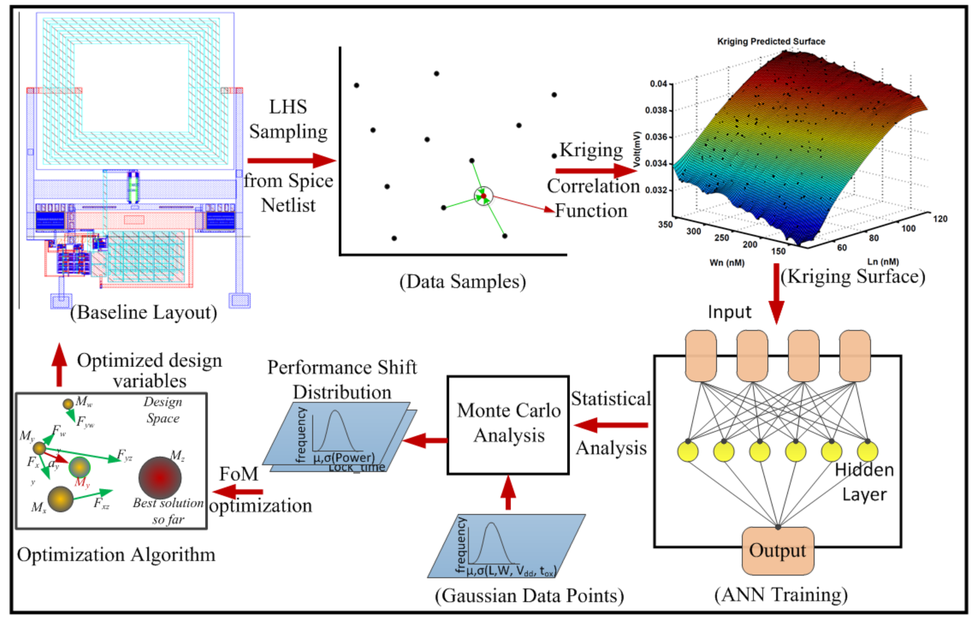
Case Study Circuit: PLL

- The design process of a Phase Locked Loop (PLL) is used to illustrate the efficiency of the proposed technique.
- The design objective was to minimize power dissipation using locking time as a constraint.
- The physical design of the PLL was implemented using 180nm technology.
- The parasitic netlist is extracted and parameterized for 21 design variables.



System Level Diagram of a PLL

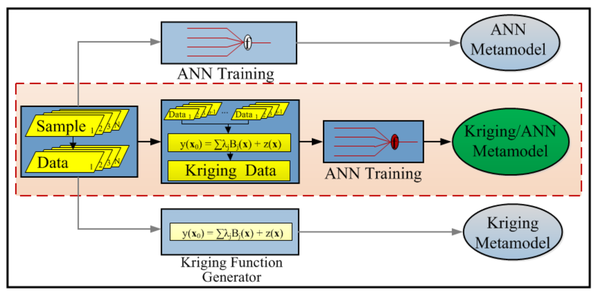
The Proposed Kriging-ANN Metamodel based Fast Analysis Method



High Level Design Flow

Kriging Bootstrapped ANN Concept

- Kriging techniques take into account the correlation effects between design parameters and can thus better capture the effects of process variation during the design process.
- Kriging weighting calculations are potentially time consuming for high dimensional designs.



Kriging Based ANN Metamodel Generation Flow

- ANN techniques produce accurate models but do not model process variation effects.
- The proposed technique combines Kriging and ANN by using intermediate sample (bootstrapped) data points to train the ANN model.

Metamodel Accuracy and Comparison

Statistical Analysis for Accuracy of Generated Metamodels for PLL

		Circuit	Kriging-ANN		Kriging		ANN	
		Value	Value	error (%)	Value	error (%)	Value	error (%)
P_{PLL}	Mean	2.48 mW	2.40 mW	3.22	2.50 mW	0.81	2.50 mW	0.81
	STD	0.42 mW	0.34 mW	19.05	0.51 mW	21.43	0.69 mW	64.28
F_{PLL}	Mean	2.66 GHz	2.51 GHz	5.64	2.66 GHz	0.11	2.74 GHz	5.38
	STD	10.95 MHz	41.93 MHz	282.92	3.72 MHz	66.03	51.9 MHz	373.97
Lck_{PLL}	Mean	5.51 μs	5.11μs	7.26	5.51 μs	0.07	5.20 μs	5.63
	STD	0.72 μs	0.44 μs	38.88	.58 ns	10.25	1.01 μs	40.27
J_{PLL}	Mean	16.80 ns	14.69ns	10.25	16.78ns	0.12	17.91 ns	6.61
	STD	1.32 ps	4.50 ps	240.91	0.68ps	48.48	19.17 ps	1352.22

Comparison with Related Metamodel Designs

Research	Metamodel	Test Circuit	Accuracy
Garitselov [28]	Polynomial	PLL	0.157
Yu [9]	Kriging	RO	0.5325 (MSE)
		LC-VCO	0.5325 (MSE)
Kuo [7]	Polynomial	PLL	2.0×10^{-4}
This Paper	Kriging-ANN	PLL	2.51×10^{-6}

Monte-Carlo Time Analysis

Model	Kriging-ANN	Kriging	ANN
Time	19 s	468 s	19 s
Speedup	24.63×	1	24.63×

Optimization Results

Final Optimization Results for PLL

Metric	Power (mW)	Locking Time (ns)	Area (μm^2)
Baseline Design	8.27	2.74	525 × 326
Optimal Optimal	1.67	2.63	525 × 326
Reduction	79 %	4 %	0 %

Conclusion

- A novel metamodeling design flow methodology combining Kriging and Artificial Neural Networks to create process aware metamodels is presented.
- The proposed technique shows improved process awareness over conventional ANN models and achieves power consumption improvement of 79% and Monte Carlo analysis time speed up of 25x over Kriging models.
- Future work will explore techniques for increasing nominal accuracy.