Architectural and Layout Level Optimization of Performance Centric 3D Nanosystem Design

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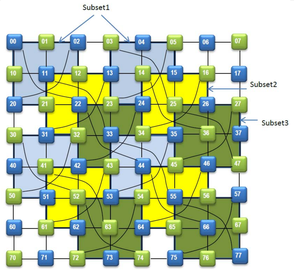
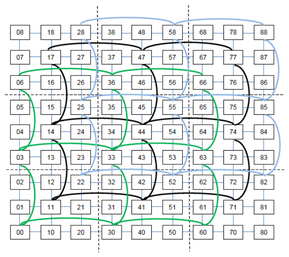
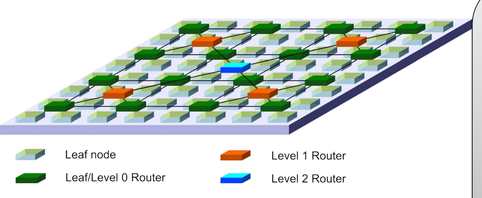
ABSTRACT

As classic CMOS based integrated circuits hit technology and performance walls, network-on-chip (NoC) and 3D integration have been evolved to provide sustainable solutions. Our current research is geared to contribute towards performance centric 3D nanosystem design with architecture and layout optimizations while reducing power dissipation. It has three key aspects. First, architectural optimization of performance centric NoC design. Different topologies like SD2D, L2STAR, FL2STAR, and Hybrid have been developed with underlying cost effient, deadlock free routing mechanisms. Second, performance centric layout design optimization algorithms for 3D ICs. Partitioning, placement, global routing of 3D ICs have been addressed and different multi-objective cost efficient design solutions have been developed. Solutions have been proposed for: (1) area, and through silicon via (TSV) aware 3D partitioning, (2) thermal, wirelength, and TSV aware 3D placement, and (3) thermal and congestion aware 3D global routing. Lastly, amalgamation of these 3D and NoC technologies to develop cost efficient 3D NoC architecture to combine benefits of previous two to offer an unprecedented performance gain. A new scalable 3D topological NoC is designed based on butterfly fat tree (BFT) topology with an efficient table based uniform routing. Designed global routing solution for 3D ICs, FuzzRoute, achieves balanced superiority in terms of routability, runtime, and wirelength over Labyrinth, BoxRouter 2.0, and FGR with 91.81%, 86.87%, and 32.16% improvement in routing time respectively and up to 17.35% in wirelength. In case of 3D NoC, BFT based topological solution has significant latency improvements of 43-89%, 83-88%, 46-96%, and 31-95% over mesh, torus, butterfly, and flattened butterfly, respectively.







SD2D [1]

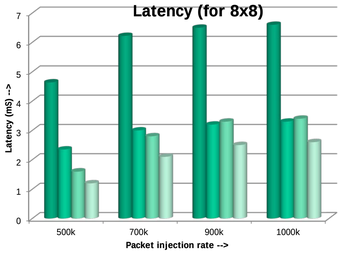
For MxN size (both multiple of 2)
Number of nodes = (M × N)
Diameter = Max (M, N)
Bisection width ≤ 2 × Min (M, N)
Node degree = Min 3, Max 7
Scalable, deadlock free
Static, irregular, case wise high latency

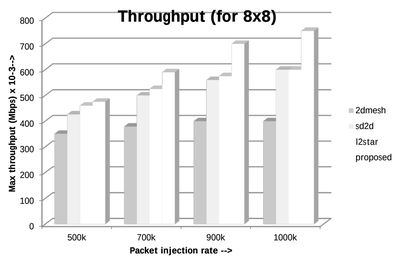
FL2STAR [3]

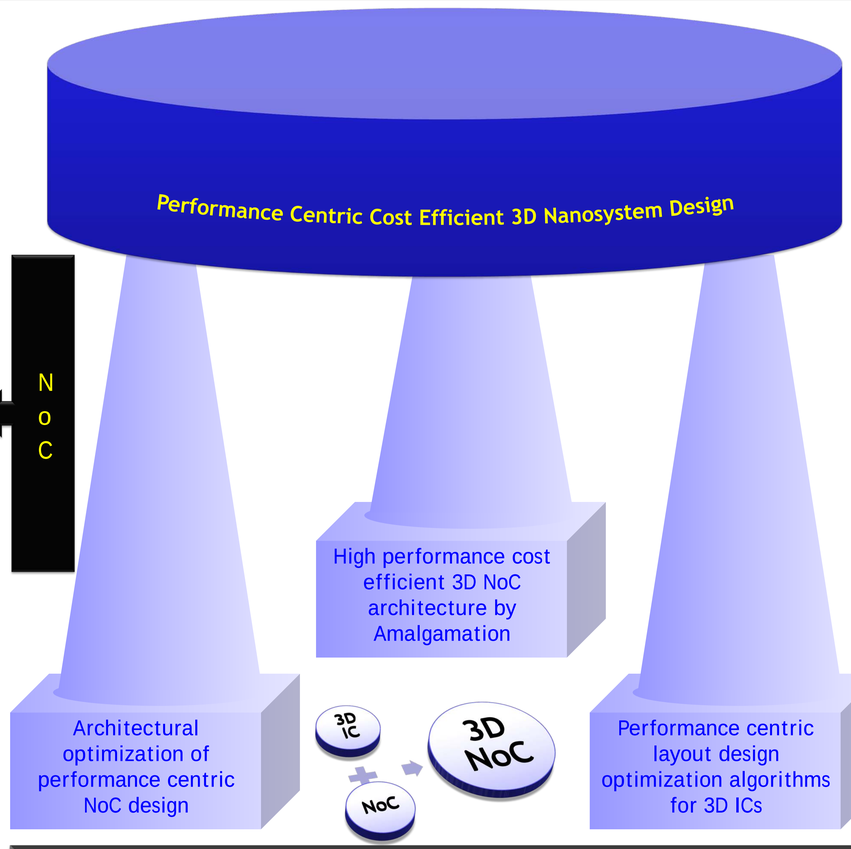
For MxN size (both multiple of 3)
Number of nodes = (M × N)
Diameter = ((Max (M,N) – 3)/3) + ((Min (M, N)/3 - 3) + 4
Bisection width = 2 × Min (M, N)
Node degree = Min 3, Max 9
Scalable, regular, deadlock free, fault tolerant
Less adaptive, selective faults

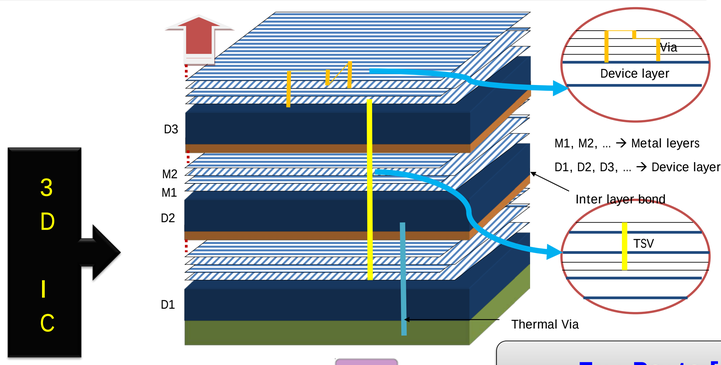
Hybrid [4]

For MxM size (M = 2^m)
Bisection width = M + 4
Max node degree of non-leaf router = 7
Of leaf router = 9, 6 for N = 4, 1
Max no IP cores connected to a network = M x M x N
Scalable, regular, deadlock free, low latency, high throughput

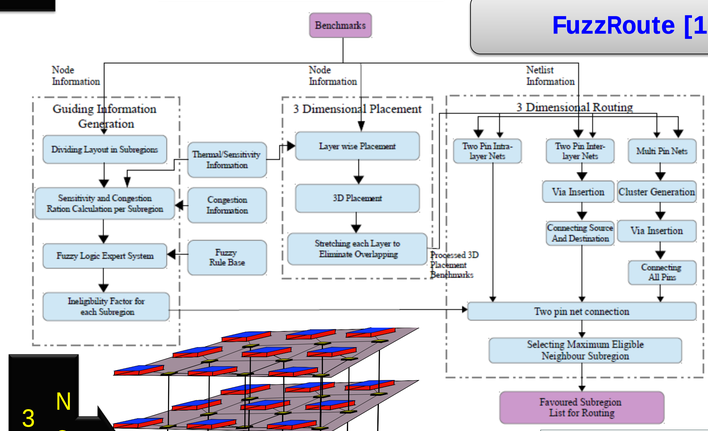


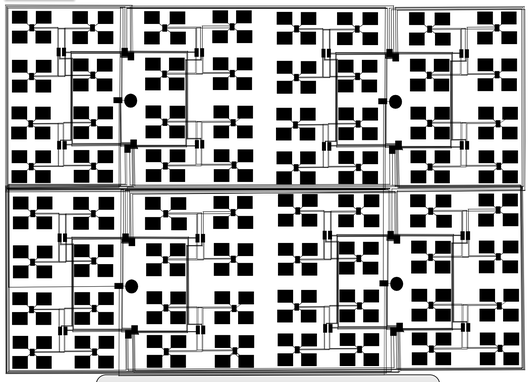




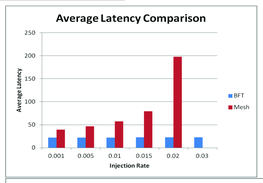


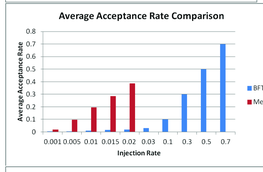
FuzzRoute [11]

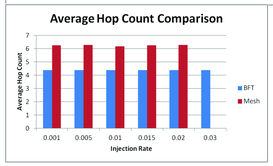




3D-NoC-BFT [12]







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