Statistical Process Variation Analysis of a Graphene FET based LC-VCO for WLAN Applications

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Outline of the talk

- Background and Motivation
- Novel Contributions
- Design of the Graphene based LC-VCO
- Sensitivity Analysis of the LC-VCO
- Process Variation Analysis
- Conclusion

Motivation

 Technology Miniaturization (aka Technology scaling)

Nano



 New Technologies (Alternative Devices)



Novel Contributions

- Verilog-A model of a graphene transistor (GFET) is implemented.
- An LC-VCO is designed using the Verilog-A model for WLAN applications and simulated in Cadence – Spectre circuit simulator.
- Process Variation analysis is done by performing Monte-Carlo analysis.



Related Prior Research

- GFET based RF circuits like ambipolar RF mixer, multiplier etc. are found in literature.
- Polarity controllable graphene inverter has been explored.
- Low on/off current ratio makes it inappropriate for digital design but very suitable for RF device design due to high carrier mobility.



GFET Model



Source:http://technophilicmag.com/2011/02/07/ graphene-field-effect-transistors/

GFET characteristic:

- Exhibits ambipolar characteristics.
- Second linear region after saturation.
 - Operating region can be determined by manipulating top and back gate voltage.



Design of GFET LC-VCO



Design Equations

$$f_0 = \frac{1}{2\pi\sqrt{LC}}\tag{1}$$

$$C = C_{GS} + C_{GD} + C_{varactor} \tag{2}$$

$$g_{active} > \frac{RC}{L}$$
 (3)

$$I_{bias} \ge I_{max} \tag{4}$$

$$v_{tank} = \frac{I_{bias}}{g_{tank}} \tag{5}$$

Cross Coupled LC-VCO using GFETs

Design of GFET LC-VCO





Design of GFET LC-VCO

VCO Characteristics

Parameter	Value		
	GFET	CMOS	
f_o	2.64 GHz	2.64 GHz	
$V_{tankp-p}$	0.55V	1.9V	
V_{supply}	9V	2.5V	
I _{bias}	0.88mA	1.1mA	
Tuning Range	4.2%	15.53%	
Phase noise(at 1MHz offset)	-92dBc/Hz	-161.1dBc/Hz	



Design of GFET LC-VCO GFET-VCO Characteristic



Fig: Tuning Characteristic(Right)



Sensitivity analysis of GFET VCO

- Sensitivity analysis is done on four major VCO characteristics:
 - Frequency
 - Phase Noise
 - Power Dissipation
 - Quality Factor

GFET Parameters selected for sensitivity analysis are:

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- Length
- Width
- Mobility



Sensitivity analysis of GFET VCO



^{2.62} 2.5 2.53 2.54 2.55 2



- VCO response is sensitive to GFET parameters.
- Dip in the curves caused by the resonance due to the variation of capacitances with length and width.



Frequency Vs Mobility

Sensitivity analysis of GFET VCO



Power Dissipation Vs Length



Power Dissipation Vs Width







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characteristic curves.

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Mobility(m²V⁻¹S⁻¹) Phase-noise Vs Mobility

04

0.25

0.3



Process Variation analysis of GFET VCO

- Monte Carlo simulation is performed on VCO circuit for 1000 samples.
- Design parameters Length(L), Width(W), Mobility, Drain to Source resistance of NFET, and top gate oxide thickness are varied within design specification ranges.

STATISTICAL CHARACTERIZATION OF GRAPHENE FET BASED *LC*-VCO.

Parameters	Mean (μ)	Mean (Fitted)	St. Dev. (σ)	St. Dev. (Fitted)
Frequency	2.56 GHz	2.57 GHz	60 MHz	28 MHz
Phase Noise (dBc/Hz)	-86.01	-87.34	7.78	4.87
Power Dissipation	12.15 mW	12.13 mW	758 μ W	$738\mu W$
Q Factor	5.49	5.49	0.84	0.71





Histograms: Frequency (top-left), Phase-noise (top-right), Power Dissipation (bottom-left), Power Dissipation (bottom-right)



PV analysis of GFET VCO

- Most frequencies fit within 2.5GHz to 2.62GHz range which is nominal frequency for the circuit.
- Phase noise varies from -80dBc/Hz to -93dBc/Hz.
- Extreme value distribution curve fits well the frequency and phase noise data.
- Lognormal distribution fits well the power dissipation and normal distribution fits well the quality factor distribution.



Conclusions

- A Verilog-A GFET implementation of a voltage controlled oscillator for WLAN applications is presented.
- A statistical analysis was performed to provide a comprehensive illustration of how GFET parameters affect circuit characteristics.
- A Monte-Carlo analysis was also presented to illustrate the effects of process variation on circuit performance.
- Further exploration of the physical design could be done to analyze circuit parasitics.



Thank you !!!