A Performance Enhancing Hybrid Locally Mesh Globally Star NoC Topology

Tuhin Subhra Das[†], Prasun Ghosal[†‡], Saraju P. Mohanty[‡], Elias Kougianos[‡]

[†] Indian Institute of Engineering Science and Technology, Shibpur (www.becs.ac.in), Howrah 711103, WB, India
[‡] NanoSystem Design Laboratory (http://nsdl.cse.unt.edu), University of North Texas, Denton, TX 76203, USA
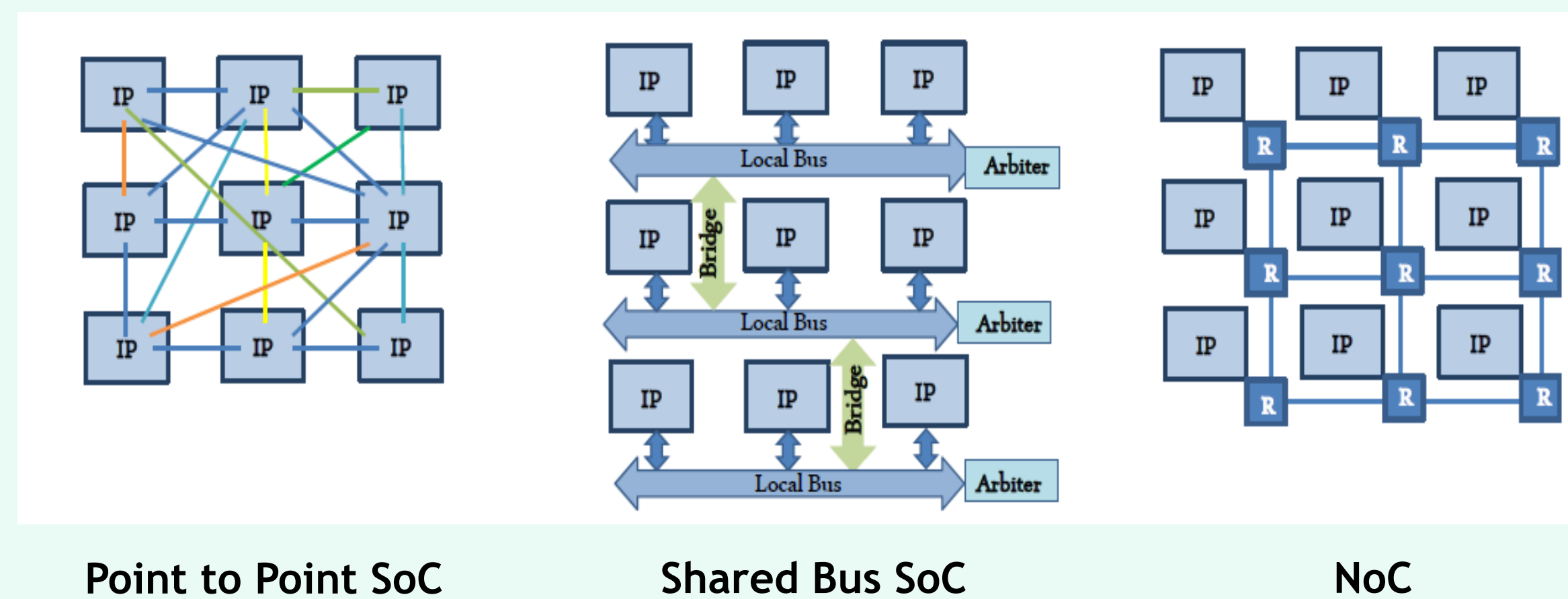Email: tuhinbcrec@gmail.com, prasun@ieee.org, saraju.mohanty@unt.edu, eliask@unt.edu

AT A GLANCE

- Rapid decrease in size in CMOS technology → severe challenges to classical design technology for convergence towards subatomic dimension
- Necessity of portable high end communication system by market continues
- Network-on-Chip (NoC) has come up as a sustainable solution for SoC, MPSoC, and, large scale CMP based designs.
- NoC provides a massively parallel communication intensive architecture for future large scale SoC design for high performance
- Underlying network interconnection architecture (topology), router architectural design, and routing policy play important roles towards the overall system performance enhancement
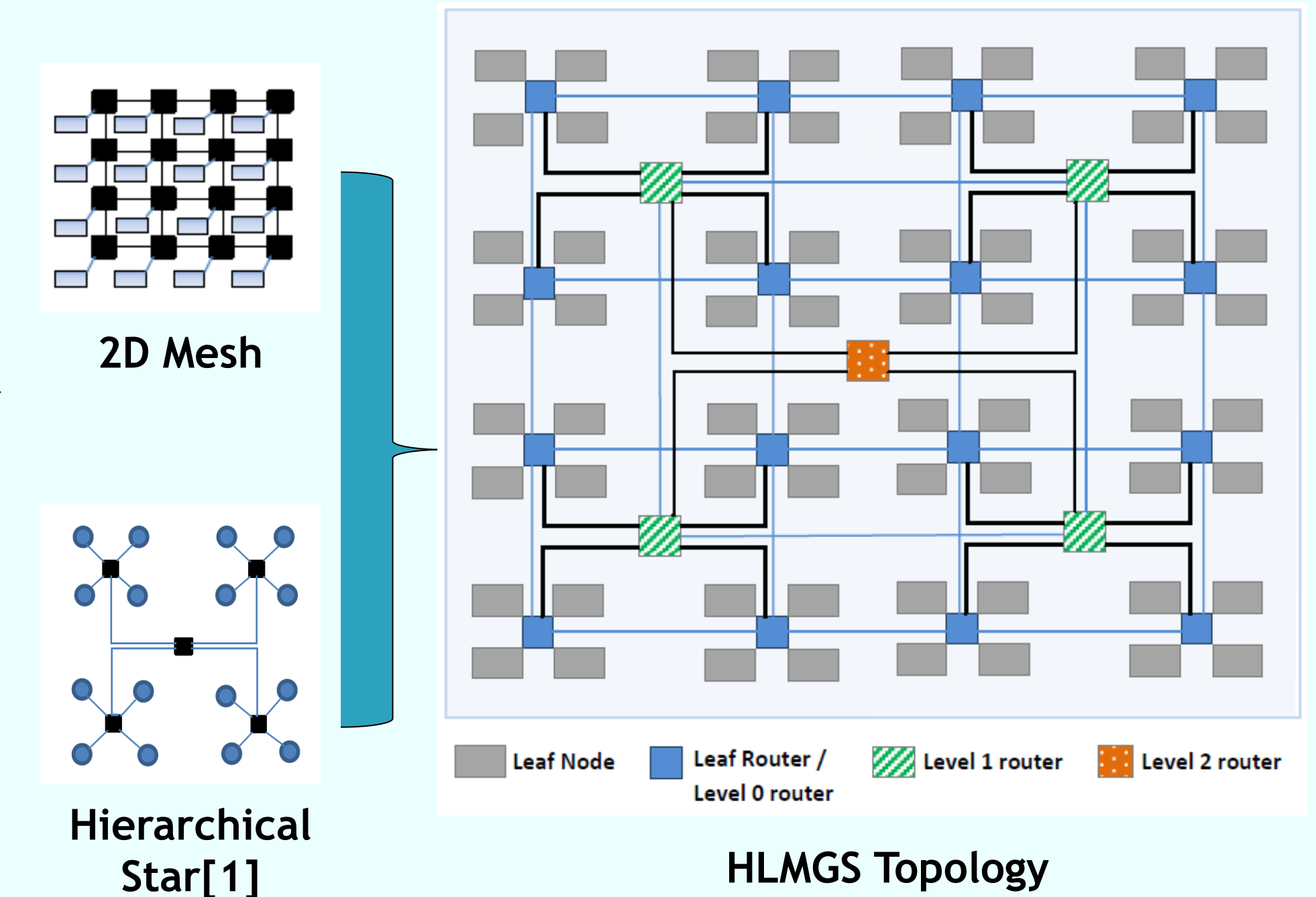
Problems in Bus Based SoC
- Challenge in integrating different silicon IPs on the same IC
- Concurrent communication is not possible in shared bus system
- More components increase → loading increases → further drop of speed, and increase in power consumption

Point to Point SoC   Shared Bus SoC   NoC

PROPOSED TOPOLOGY

Proposed Hybrid Locally Mesh Globally Star (HLMGS) NOC Topology

2D Mesh

Hierarchical Star[1]

HLMGS Topology

Leaf Node   Leaf Router / Level 0 router   Level 1 router   Level 2 router

TOPOLOGY METRICS

Proposed Hybrid NOC Topology

Important parameters of an M × M sized proposed architecture are as follows (where, M = 2^m for m = 2, 3, 4, . . . , n.)

Bisection width = M + 4
Maximum node degree of non-leaf router = 7
Maximum node degree of leaf router = 9, when N = 4
Maximum node degree of leaf router = 6, when N = 1
Maximum number of IP cores connected to a network = M×M×N
Where, N represents the numbers of IP core connected to each leaf level router.

Leaf Node   Leaf Router / Level 0 router   Level 1 router   Level 2 router
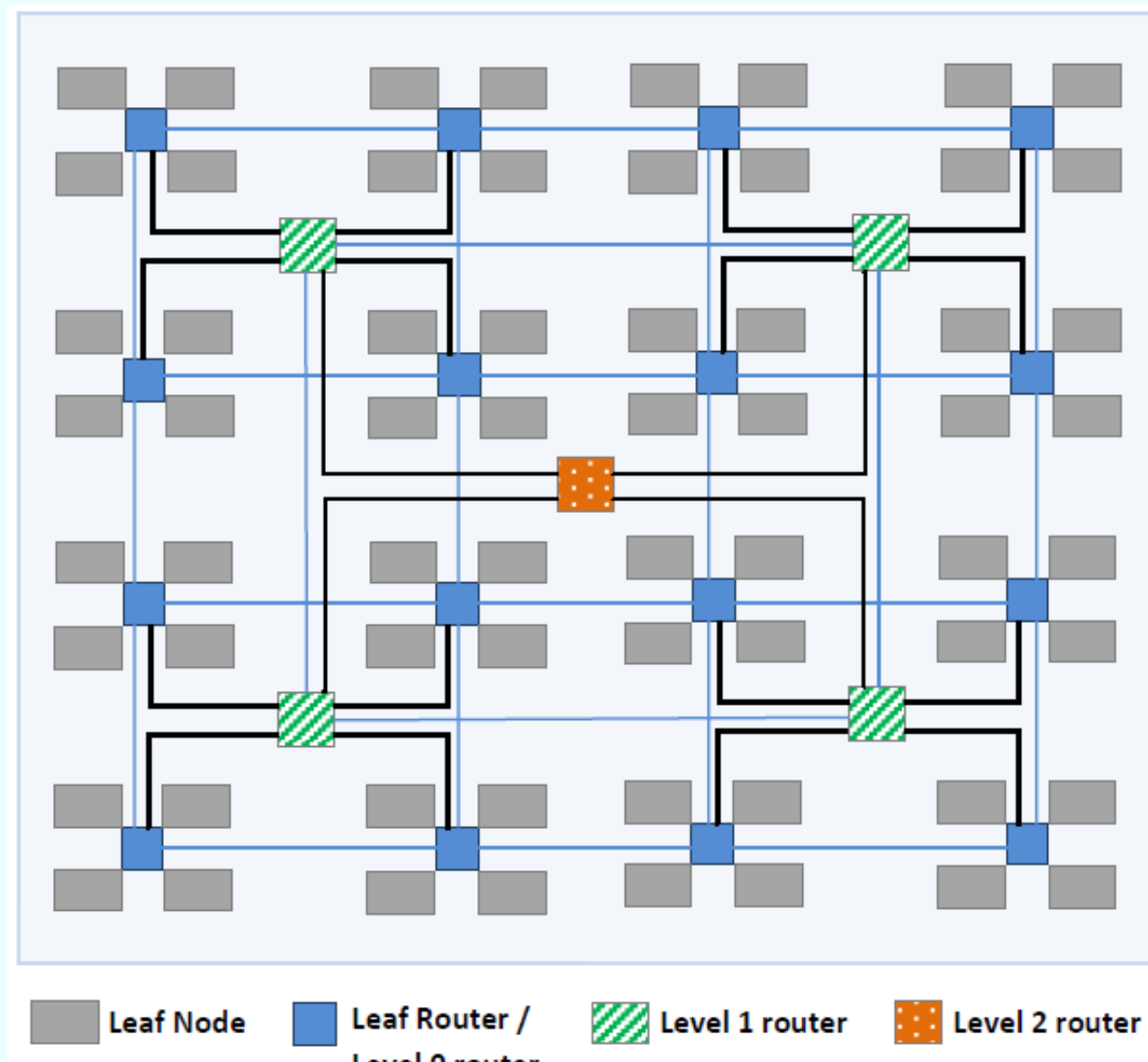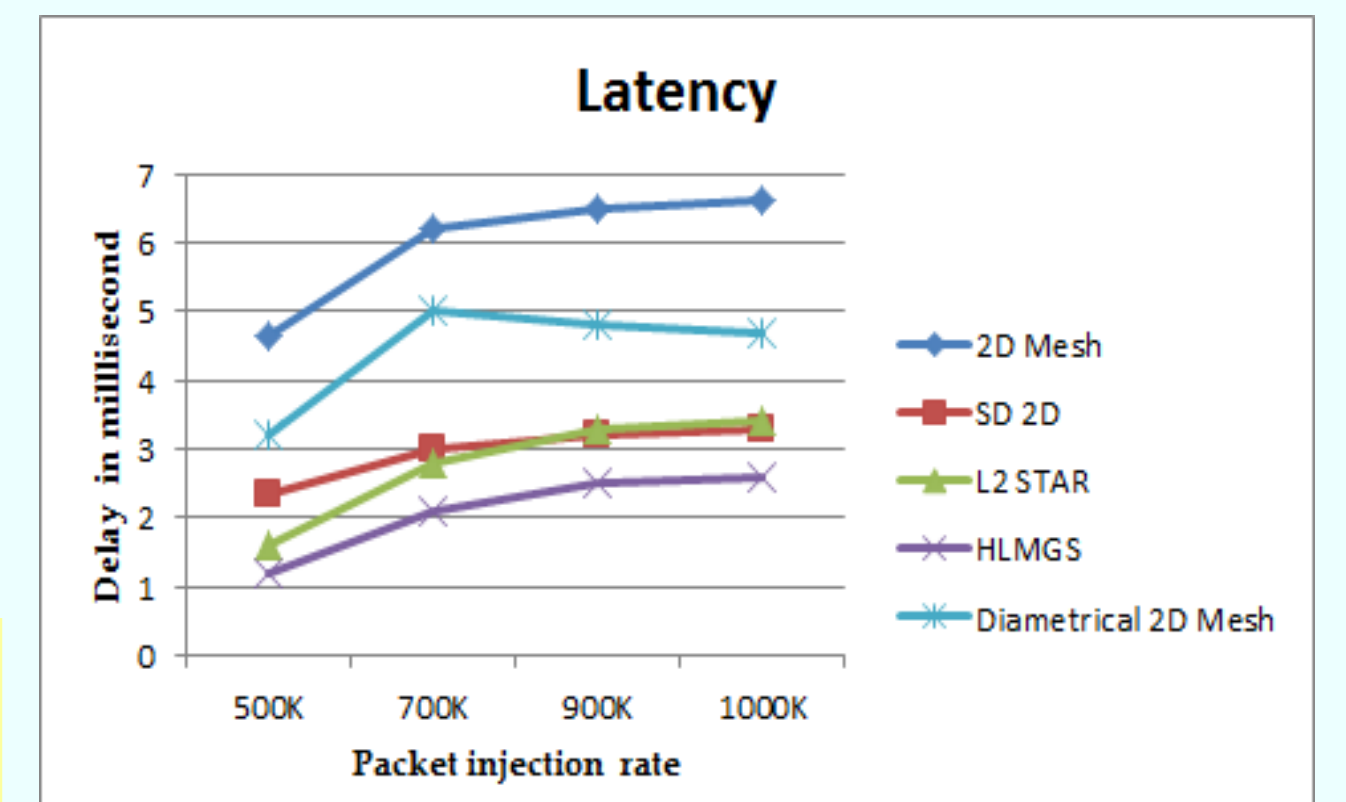
EXPERIMENTAL RESULTS

- Simulated result on important performance centric parameters like packet delay, throughput, packet drop ratio has been calculated and compared with Mesh topology, and with some other hybrid topology viz. SD2D[2], L2STAR [3], and Diametrical 2D Mesh[4] topology

$$Average\ link\ delay = \sum_{k=0}^{n} \frac{(Average\ delay\ of\ each\ commodity)}{n};$$
Where, n signifies total no. of commodity

$$Average\ commodity\ delay = \sum_{k=0}^{p}(Time\ stamp\ of\ data\ packet\ received\ at\ sink - Time\ stamp\ of\ data\ packet\ sent\ at\ source)/p;$$
Where, p signifies the total no. of packet received by sink
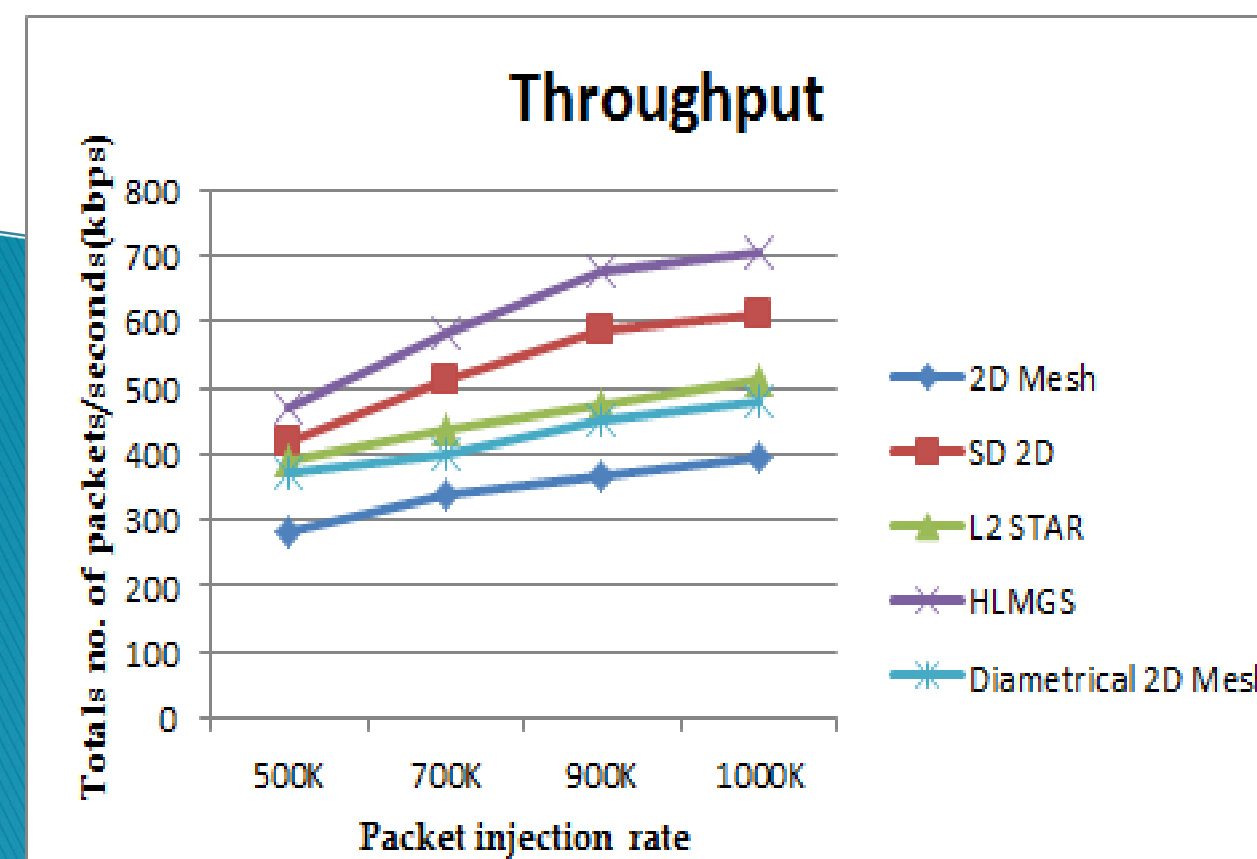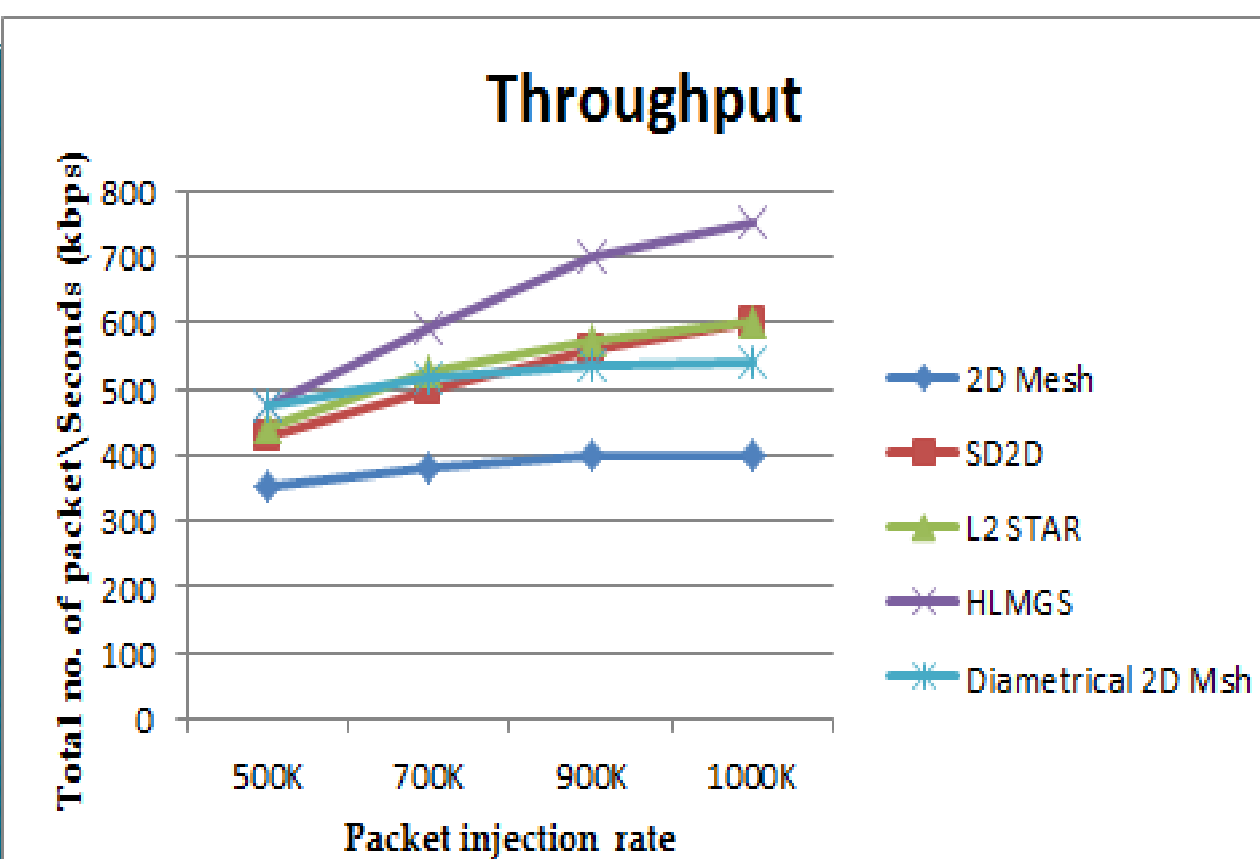

Latency

Observed latency of proposed 8x8 sized topology:

- Latency benefit of 62% over 2D Mesh
- 44% over Diametrical 2D Mesh
- 30% over SD2D and L2STAR

EXPERIMENTAL RESULTS

$$Throughput = \frac{Total\_packets/flits\_received\_in\_by\_\sin k}{Number\_of\_com\ mod\ ity}\bigg/Total\_time$$

Throughput

Throughput

Throughput of proposed 8x8 sized topology:

- 55% throughput gain over simple Mesh
- 28% over Diametrical 2D Mesh
- 20 % gain over SD2D and L2STAR

Throughput of proposed 12x12 sized topology:

- HLMGS has 42% gain over Mesh
- 32% over Diametrical 2D Mesh
- 27% over L2STAR and 14% over SD2D

$$Av = Ns(Rs + AsDgSfBs) + NcAc + AlNlLl$$

Area Overhead: (Using method proposed in [5])
- Compared to simple mesh, HLMGS topology has an area overhead of 31% to 13% for 8x8 sized topology with varying IP core connected to each router from 1 to 4

CONCLUSION & FUTURE WORK

- Proposed topology improves system performance in terms of latency and throughput
- Future works may be extended to minimize this area overhead as well as reduction of channel contention
- Observed result may be verified further by other NoC specific simulator to prove novelty of the proposed work
- System performance can be improved further by forwarding packets in some congestion aware dynamic way

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