Variability-Aware Design of Double Gate FinFET-based Current Mirrors

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Outline of the talk

- Introduction and Motivation
- Novel Contributions
- Related Research
- Double-Gate FinFET-based Current Mirror Design.
- Variability Analysis OF FinFET Current Mirrors
- Performance Analysis OF DG-FinFET based Current Mirrors
- Current Mirror Design Guidelines using DG-FinFET
- Conclusions and Future Research

Introduction and Motivation

- Major drawbacks of nano-CMOS current mirrors in analog design:
  - Short channel effects (SCE) and mismatch
  - Output resistance degradation
  - compliance voltage increase.
- Promising candidate is double gate FinFET (DG-FinFET) technology:
  - suppression of SCE
  - high transconductance and optimal subthreshold voltage.
  - reduced mismatch from random dopant fluctuations.
  - design flexibility at circuit level with two gates as the threshold voltage can be adjusted using bias applied on the back-gate.

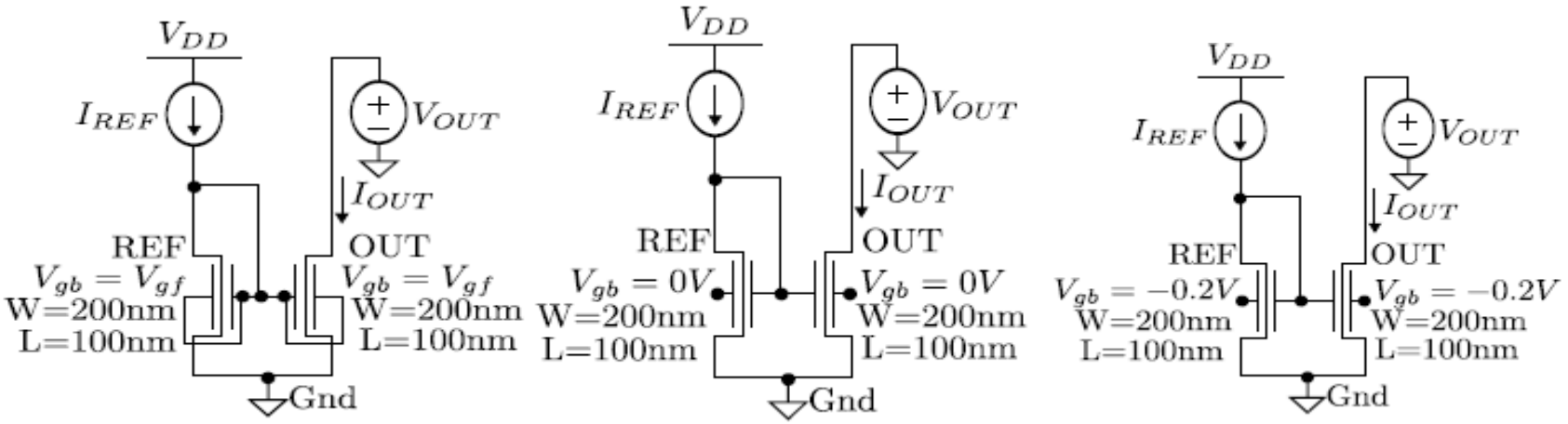
Novel Contributions

- Comparative study among SG, IG and LP configurations of the double gate FinFET current mirror is presented using 32 nm FinFET.
- Study of mismatch, variability, output resistance (r_0), compliance voltage (V_{CV}) for SG, IG and LP mode FinFET current mirrors is presented.
- A novel algorithm is presented for measuring and predicting mismatch in double gate FinFET current mirrors using Design of Experiments (DOE) and polynomial modeling. Mismatch models are developed for each configuration.
- A novel algorithm is presented for measuring variability in the various double gate FinFET configuration-based current mirrors. The coefficient of variation (c_v) is presented for each configuration.
- Guidelines are formed for current mirror design using double gate FinFET current mirrors.

Related Prior Research

- Feasibility of FinFET based digital and analog circuits is well established in literature.
- Various configurations of the FinFET device for analog applications have been presented in current literature with main focus on forward bias configurations
- Reverse bias configurations, which are becoming increasingly popular for digital applications and are covered in the current paper.
- The current paper deals with current mirror design focusing more on the relevant FoMs like compliance voltage and output resistance.
- Apart from variability, current mismatch is measured in this paper, which is crucial for current mirror design.

Double Gate FinFET based Current Mirrors



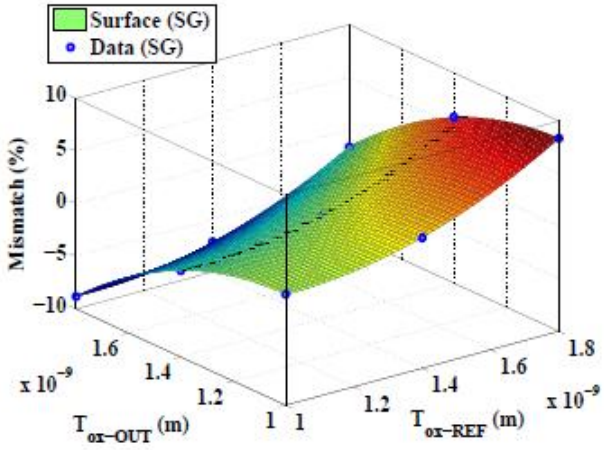
SG mode IG mode LP mode

- Figure shows shorted-gate (SG), independent-gate (IG), and Low-Power (LP) n-type FinFET current mirrors. Vgf= front gate voltage, Vgb= back gate voltage.
- In the SG mode, the front and back gates are tied together.
- In the independent-gate (IG) mode, the top part of the gate is etched out giving rise to two independent gates and the back-gate voltage (Vgb) is set to 0 V.
- The low-power (LP)-mode applies a reverse-bias voltage of -0.2V to the back-gate.

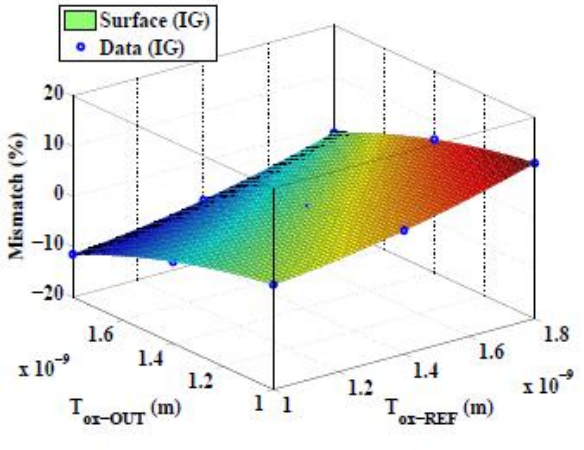
Mismatch in FinFET configuration current mirrors

1. **Objective:** Mismatch in SG, IG and LP configuration-based FinFET current mirrors.
2. **Input Factors:** $T_{ox\text{-}REF}$, $T_{ox\text{-}OUT}$.
3. **Output Responses:** Transfer ratio= I_{OUT}/I_{REF}, mismatch= $(I_{OUT}- I_{REF})/I_{REF}$ x 100%.
4. Setup experiment using 3 level-2 factors (32=9 states).
5. **for each** FinFET configuration **do**
6. **for each** 1:9 state of experiment **do**
7. Run simulation.
8. Record I_{OUT}/I_{REF}, mismatch.
9. **end for**
10. **end for**
11. Form regression-based mismatch models.

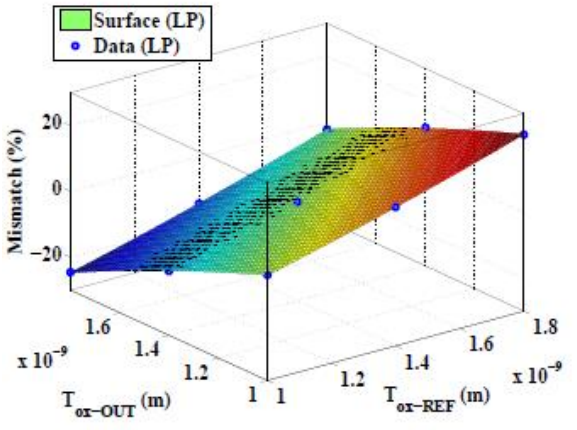
Mismatch in FinFET configuration current mirrors



SG mode



IG mode



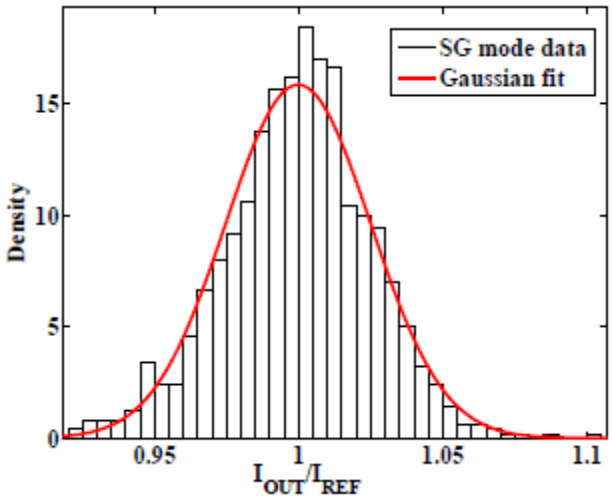
LP mode

REF	OUT	$\frac{I_{OUT}}{I_{REF}}$(SG)	Mismatch(SG)	$\frac{I_{OUT}}{I_{REF}}$(IG)	Mismatch(IG)	$\frac{I_{OUT}}{I_{REF}}$(LP)	Mismatch(LP)
T_{ox-R_L}	T_{ox-OUT_L}	1.00555	+0.555%	1.00845	+0.845%	1.0208	+2.080%
T_{ox-REF}	T_{ox-OUT_L}	1.02402	+2.402%	1.04573	+4.573%	1.12182	+12.182%
T_{ox-REF_H}	T_{ox-OUT_L}	1.08352	+8.352%	1.10897	+10.897%	1.23643	+23.643%
T_{ox-REF_L}	T_{ox-OUT}	0.982087	-1.791%	0.962083	-3.792%	0.89517	-10.483%
T_{ox-REF}	T_{ox-OUT}	1	0%	1	0%	1	0%
T_{ox-REF_H}	T_{ox-OUT}	1.05793	+5.793%	1.06459	+6.459%	1.12034	+12.034%
T_{ox-REF_L}	T_{ox-OUT_H}	0.911764	-8.824%	0.88536	-11.464%	0.75459	-24.541%
T_{ox-REF}	T_{ox-OUT_H}	0.928658	-7.134%	0.922524	-7.748%	0.857361	-14.264%
T_{ox-REF_H}	T_{ox-OUT_H}	0.983526	-1.647%	0.986101	-1.390%	0.977039	-2.296%

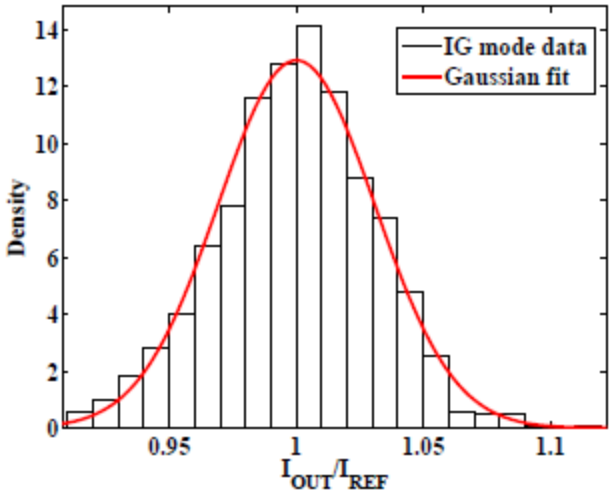
Process Variation in FinFET configuration current mirrors

1. **Objective:** Coefficient of variation (c_v) in SG, IG and LP configuration-based FinFET current mirrors.
2. **Input Factors:** $N(\mu_{Tox\text{-}REF}, \sigma_{Tox\text{-}REF})$, $N(\mu_{Tox\text{-}OUT}, \sigma_{Tox\text{-}OUT})$.
3. **Output Responses:** $N(\mu I_{OUT}/I_{REF}, \sigma I_{OUT}/I_{REF})$.
4. Setup Monte-Carlo experiment.
5. **for each** FinFET configuration do
6. **for each** 1:1000 Monte-Carlo run do
7. Run simulation.
8. Record IOUT/IREF
9. **end for**
10. **end for**
11. Report $\mu I_{OUT}/I_{REF}$, $\sigma I_{OUT}/I_{REF}$ and $c_v I_{OUT}/I_{REF}$

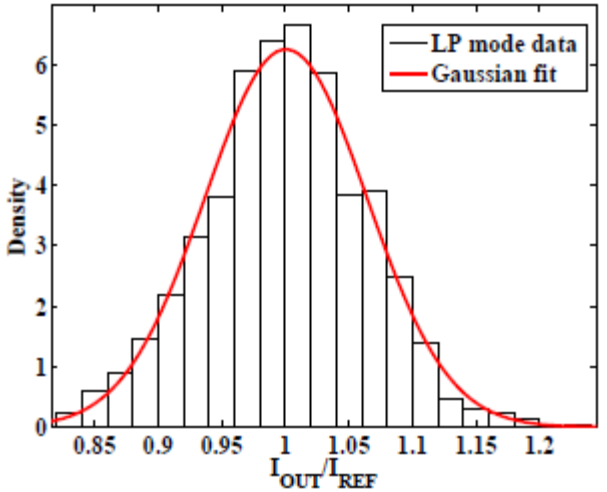
Process Variation in FinFET configuration current mirrors



SG mode



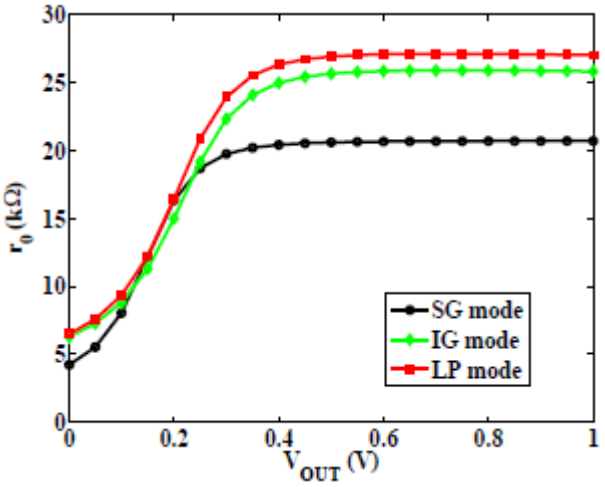
IG mode



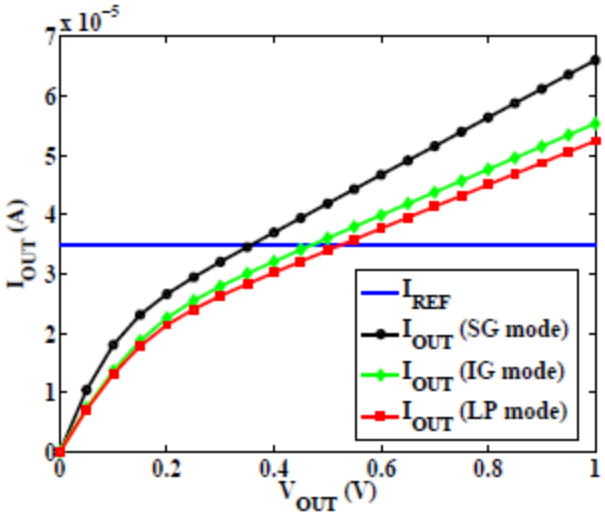
LP mode

Mode	μ	σ	c_V(in %)
SG	1	0.0252	2.52
IG	1	0.0309	3.09
LP	1	0.0637	6.37

Performance Analysis OF DG-FinFET based Current Mirrors



r_0 comparison



V_{CV} comparison

Configuration	r_0
SG mode	20.43 kΩ
IG mode	24.58 kΩ
LP mode	26.33 kΩ

Configuration	V_{CV} (V)
SG mode	0.359
IG mode	0.473
LP mode	0.528

Current Mirror Design Guidelines using DG-FinFET

Variability	r_0	V_{CV}	Configuration
High	High	High	LP
Medium	Medium	Medium	IG
Low	Low	Low	SG

- LP mode current mirror offers high gain (high r_0) making it suitable for application in a common source amplifier. However, it has high variability and high V_{CV}.
- SG mode current mirror offers low gain (r_0) making it suitable for use in a common drain amplifier for a voltage buffer. SG mode current mirror also offers the lowest variability and V_{CV}.
- IG mode offers a compromise between the LP and SG mode with medium variability, r_0 and V_{CV} .

Conclusions and Future Work

- Current mirror design based on 3 configurations double gate FinFET device for analog circuit design has been studied.
- 2 novel algorithms are presented for measuring mismatch (using DOE and polynomial modeling) and variability in the double gate FinFET current mirrors are presented.
- Future work will involve exploring advanced current mirror architectures such as cascode current mirror, regulated drain current mirror, supply independent biasing circuits using the various configurations of DG-FinFET.
- Mixed mode current mirrors may be proposed where certain devices are operated in the LP mode for high output resistance, and other devices in the SG mode for lower mismatch and higher compliance range.


Thank you !!!