DFX for Nanoelectronic Systems

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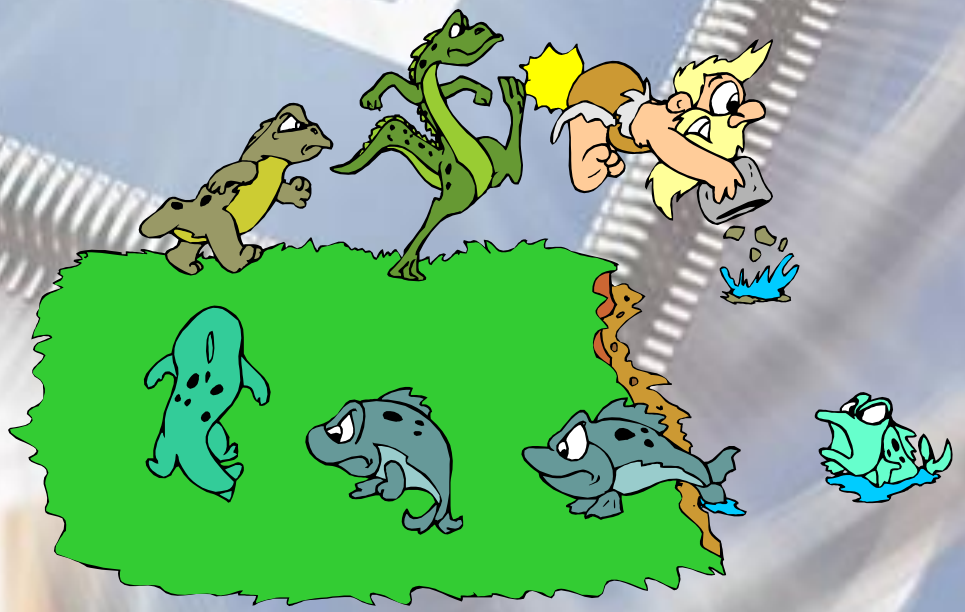
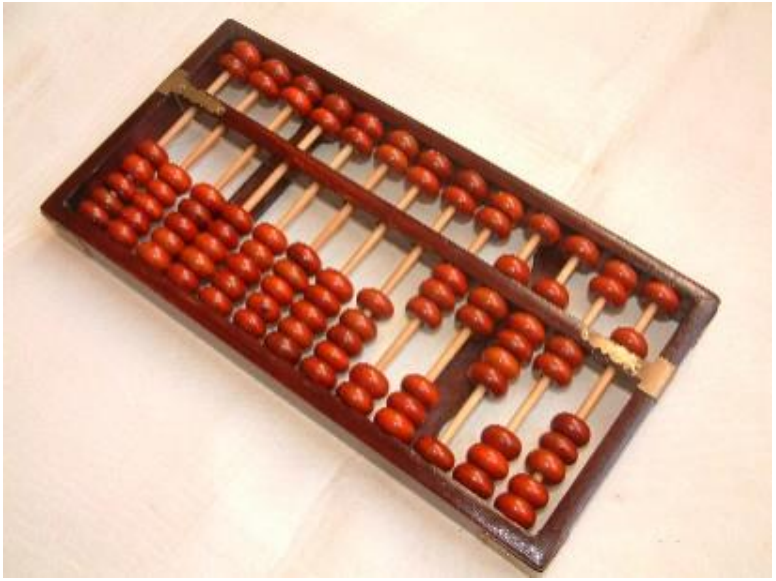
Computing Evolution

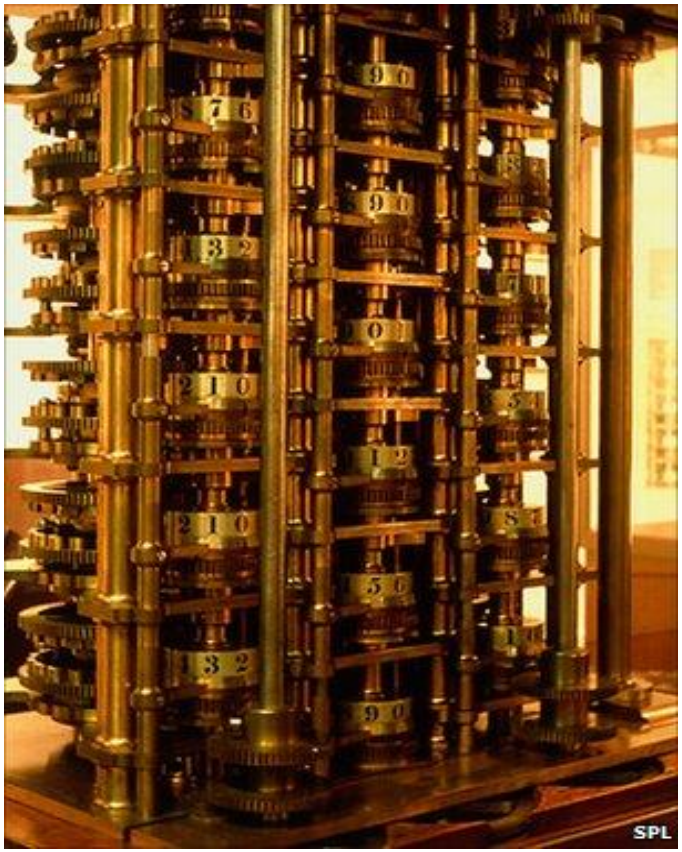


Ancient Computing Machines -- Mechanical



2400 BC

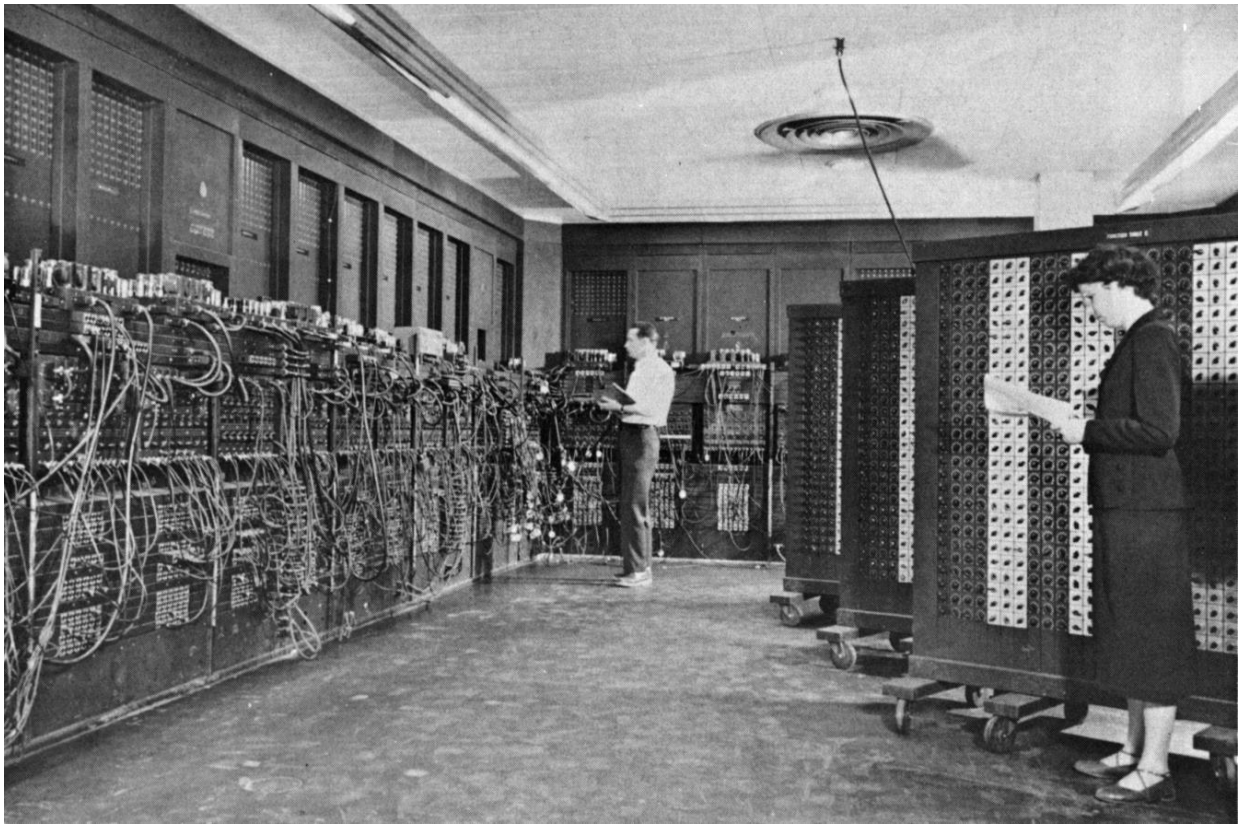
-- The abacus
-- The first known calculator
-- Invented in Babylonia



1832 AD

-- The Babbage Difference Machine
-- Tabulated polynomial functions
-- Invented in Britain

The First Electronic Computer



1946

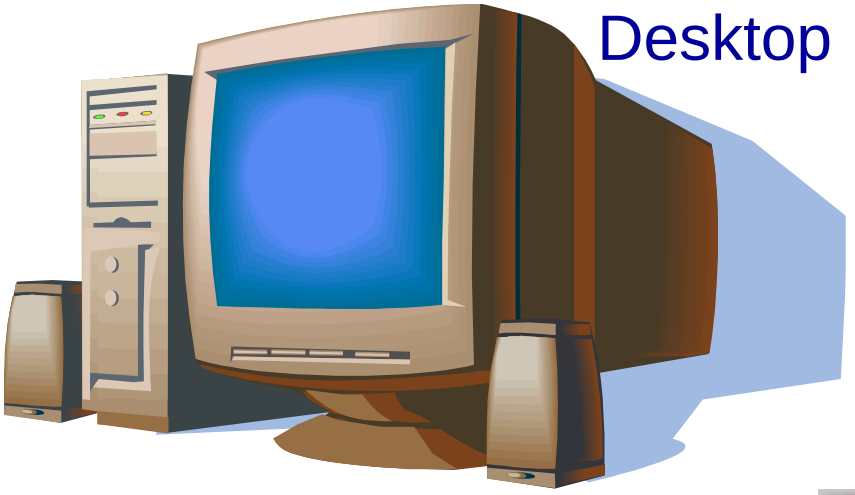
-- ENIAC -- The first electronic general-purpose computer.

-- Turing-complete, digital, and programmable.

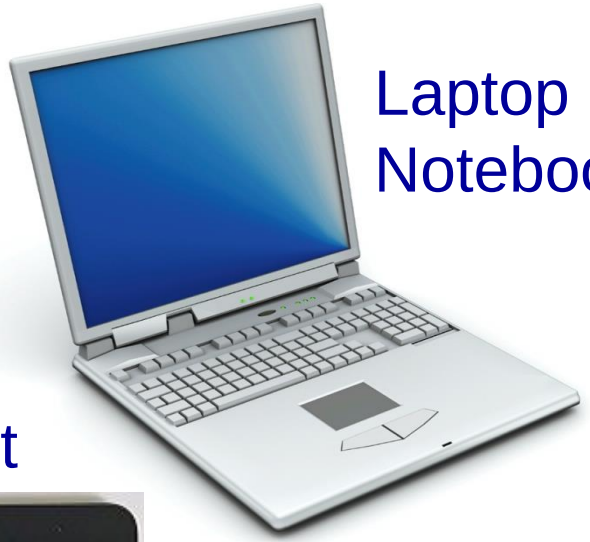
-- Invented in USA.

Current Computing Systems

Desktop PC



Laptop or Notebook PC



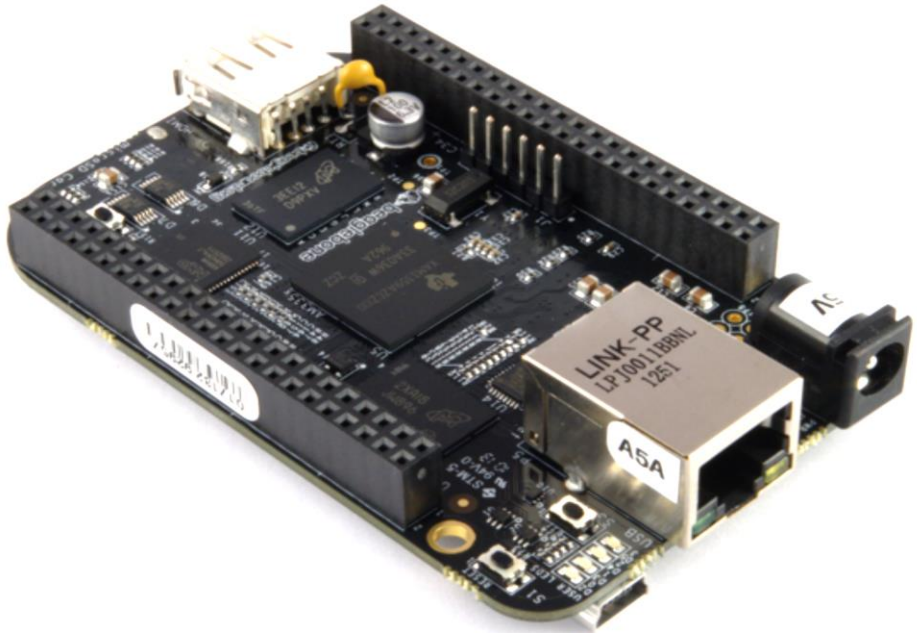
Tablet

Smart Phone

Slate PC

Smallest Single-Board Computers

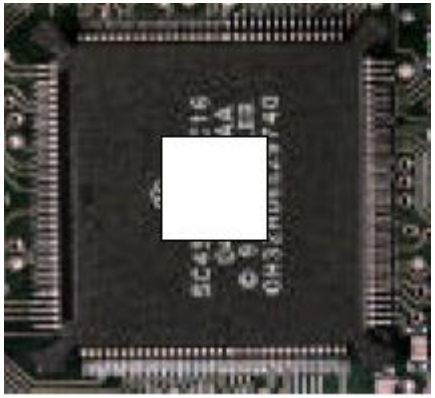
Raspberry Pi



BeagleBone

The Workhorses

Variety of Integrated Circuits or Chips?



Low-Cost ASIC

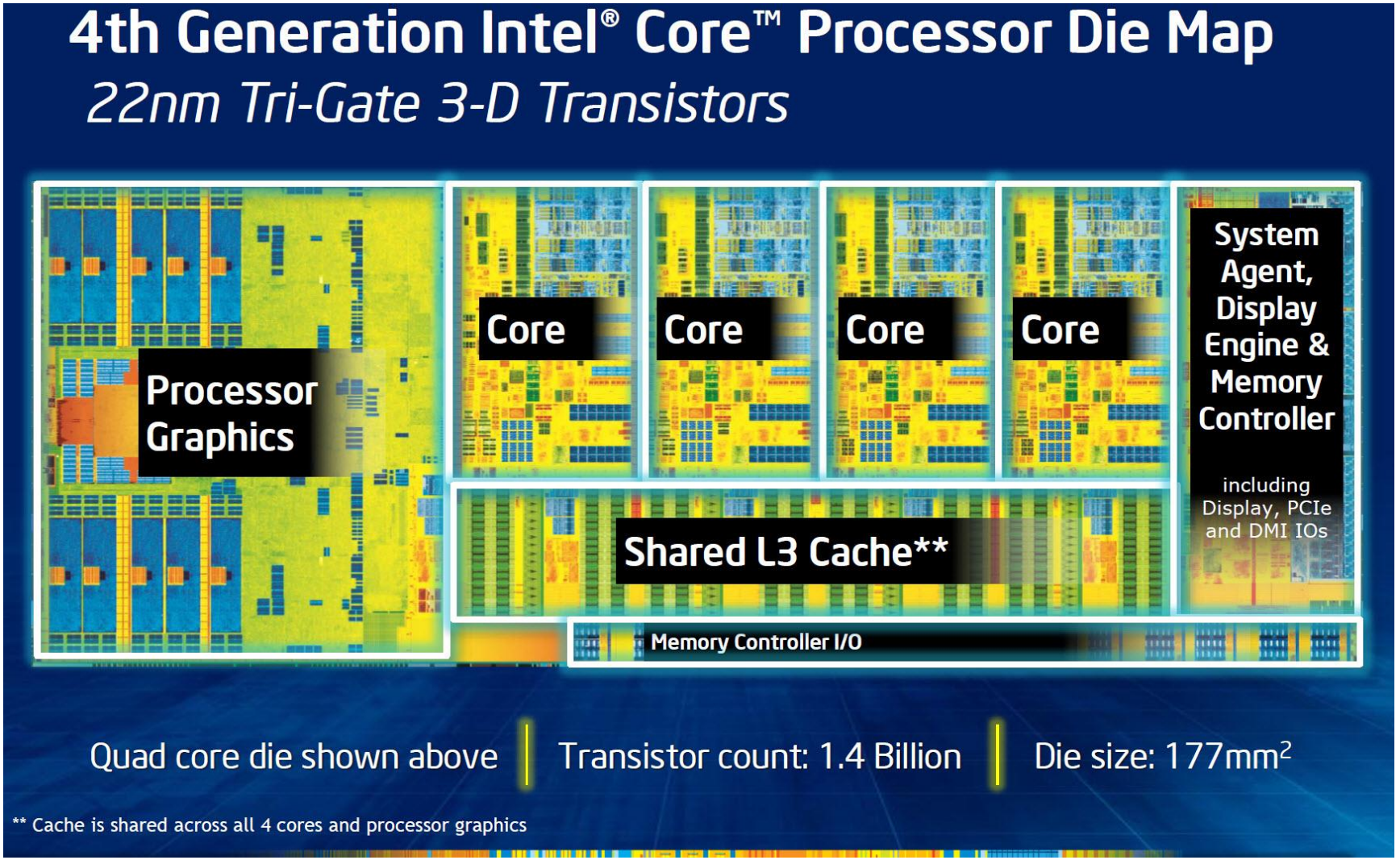
Communication Chip

Secure Media Processor

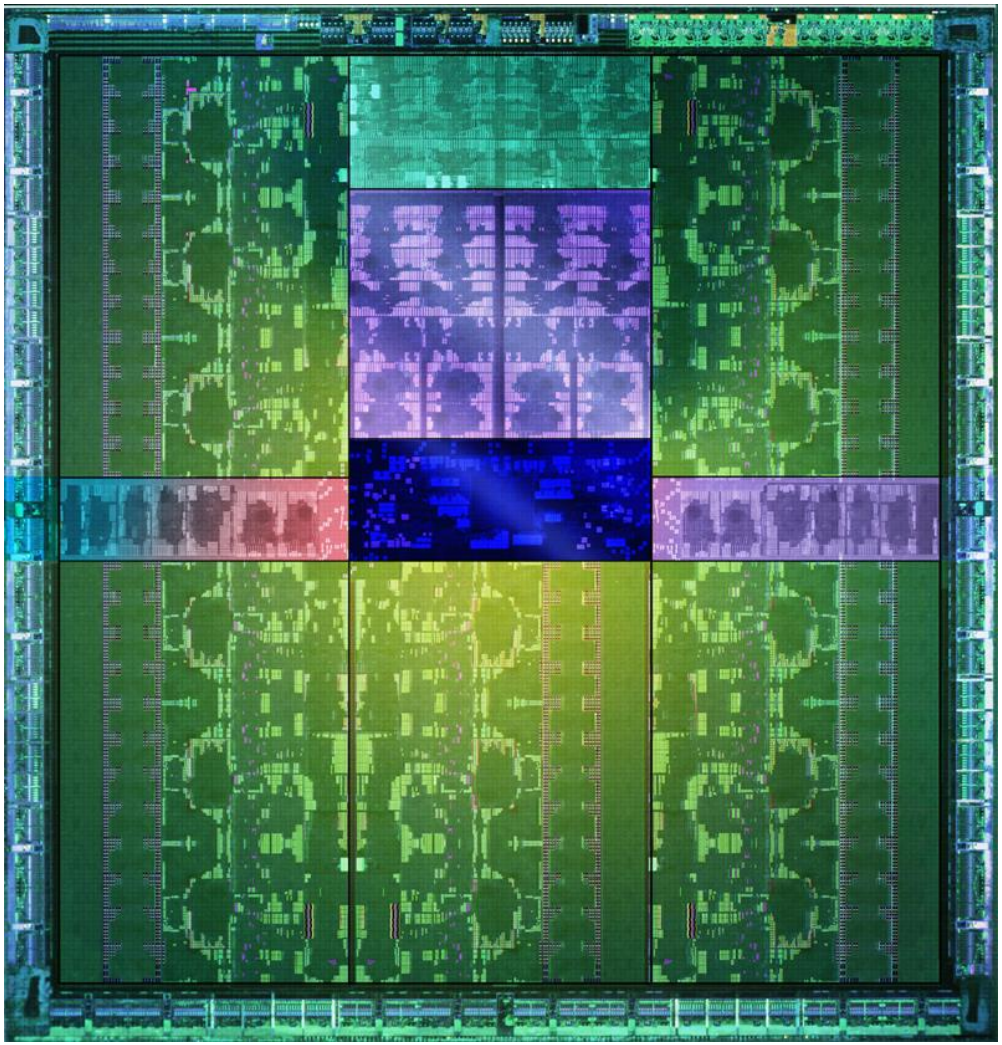
Intel Core i7 LGA1366 processor has 1366 pins.

ADC Chip

Intel Haswell Chip -- 2013



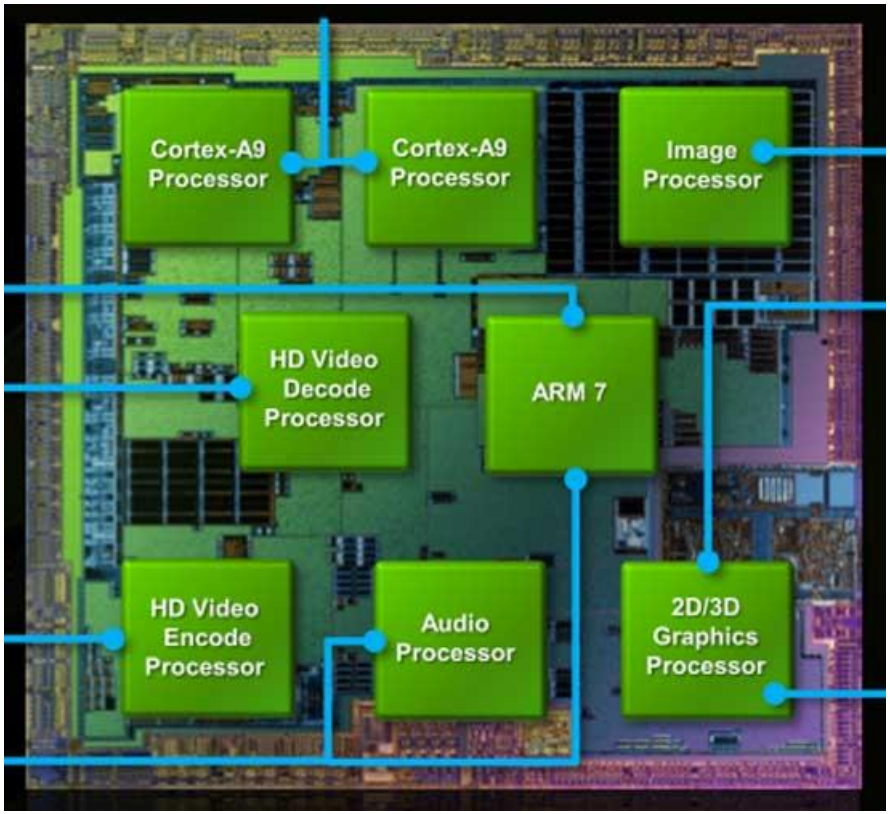
GPU with Highest Transistor Count



Nvidia GK110 has 7.1 billion transistors of a 28nm technology.

Source: http://www.tomshardware.com/news/nvidia-tesla-k20-gk110-gpu,15683.html

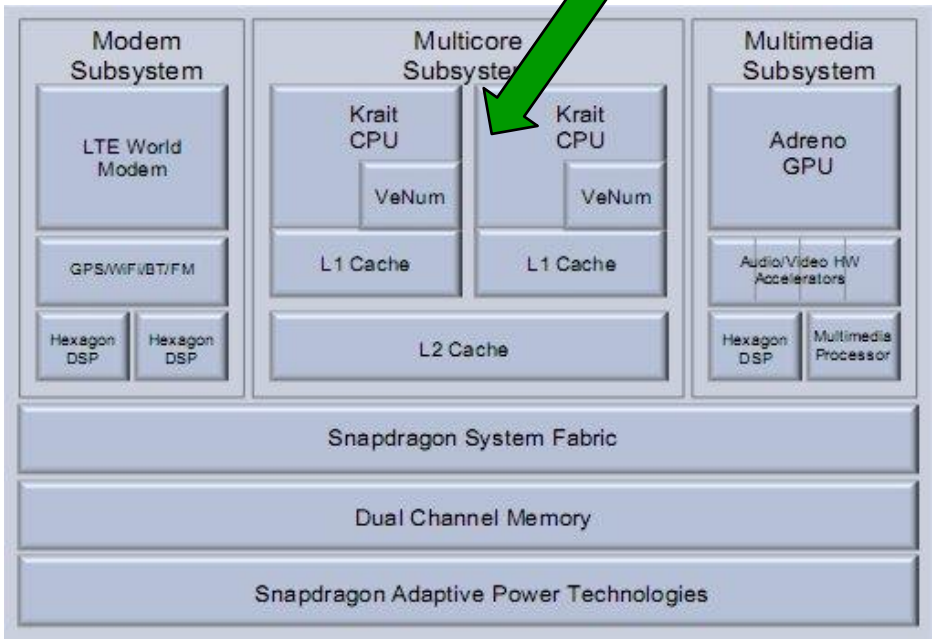
Processor for Mobile Systems: Essentially AMS-SoCs



NVIDIA's Tegra 2 die

Source: http://www.anandtech.com

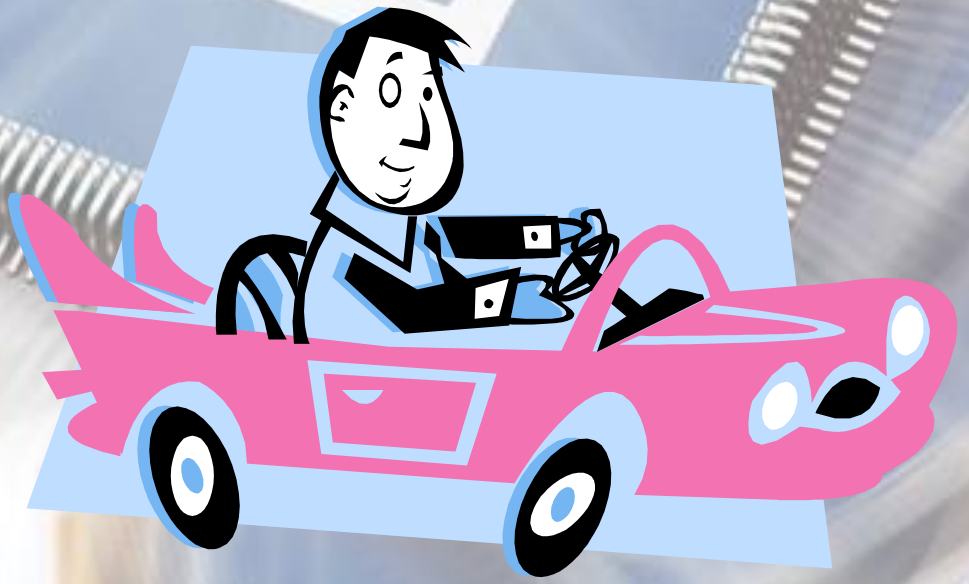
ARM-based from Qualcomm



Snapdragon S4 Block Diagram

Source: http://www.cnx-software.com

The Drivers

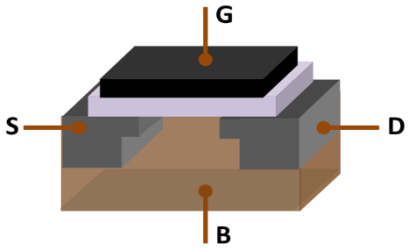


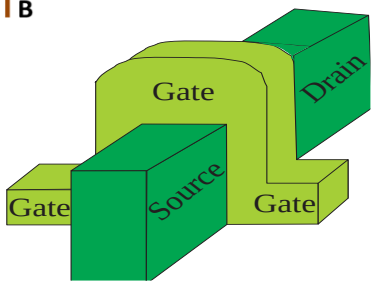
Two Main Drivers

- Technology Miniaturization (aka Technology Scaling)

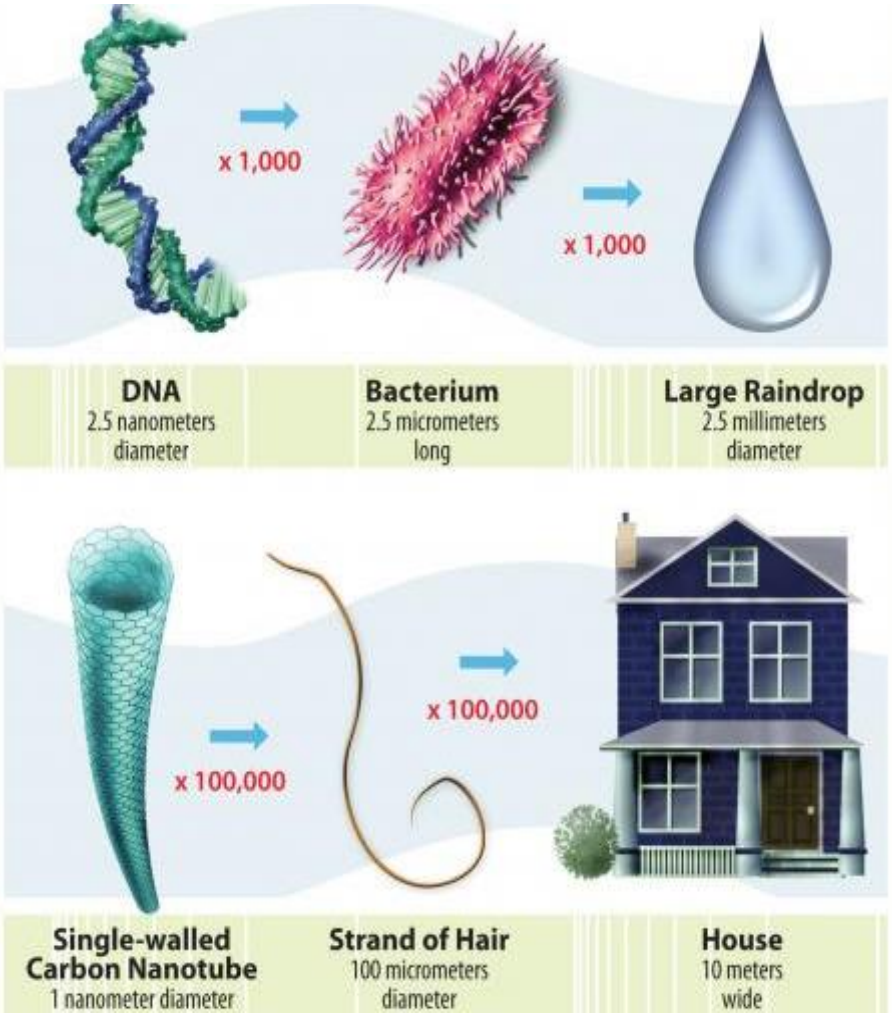
Nano

- New Technology (Alternative Devices)





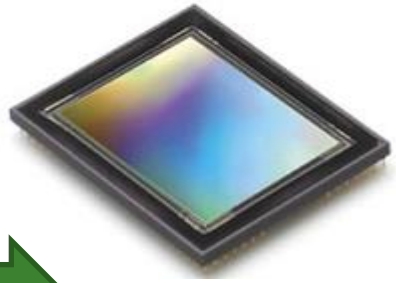
How Small in Nano??

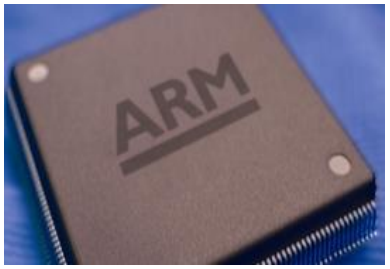


- "nano" means one-billionth, or 10^{-9}
- A sheet of paper is about 100,000 nanometers thick
- A human hair is approx. 100,000 nanometers wide

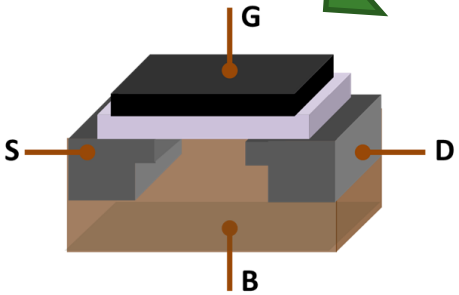
Source: http://www.nano.gov/nanotech-101/what/nano-size

A Typical Nanoelectronic System

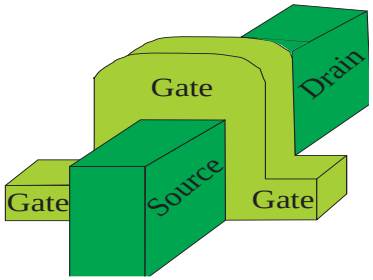




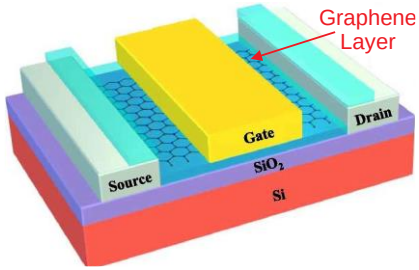
Heterogenours components with millions of nanoscale devices.



High-K nano-CMOS



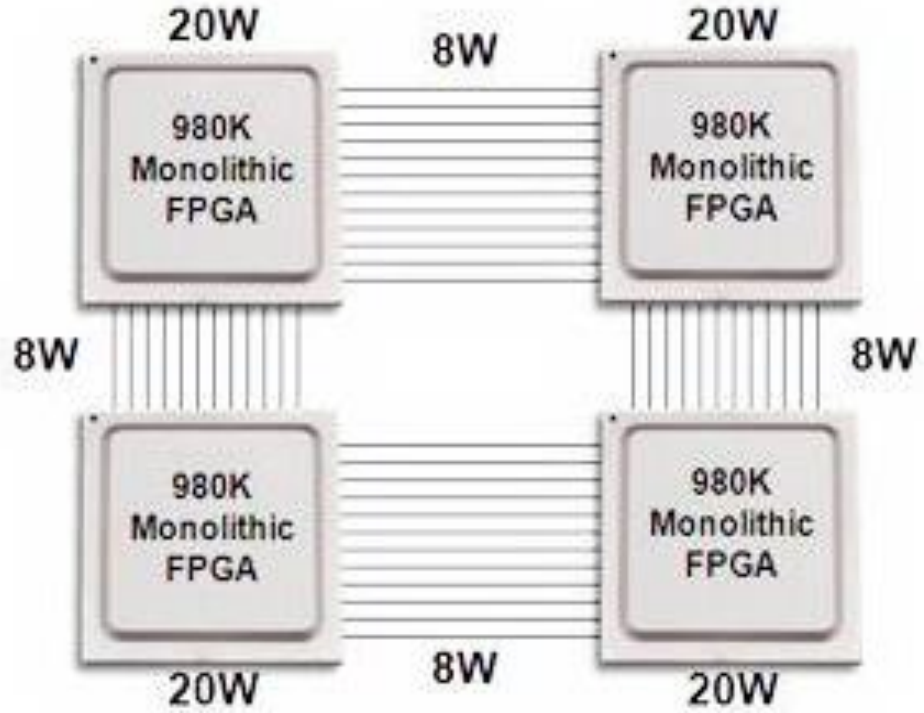
Triple Gate



Graphene Nanoribbon

Good and Bad, and DFX

Scaling Reduces Power Dissipation



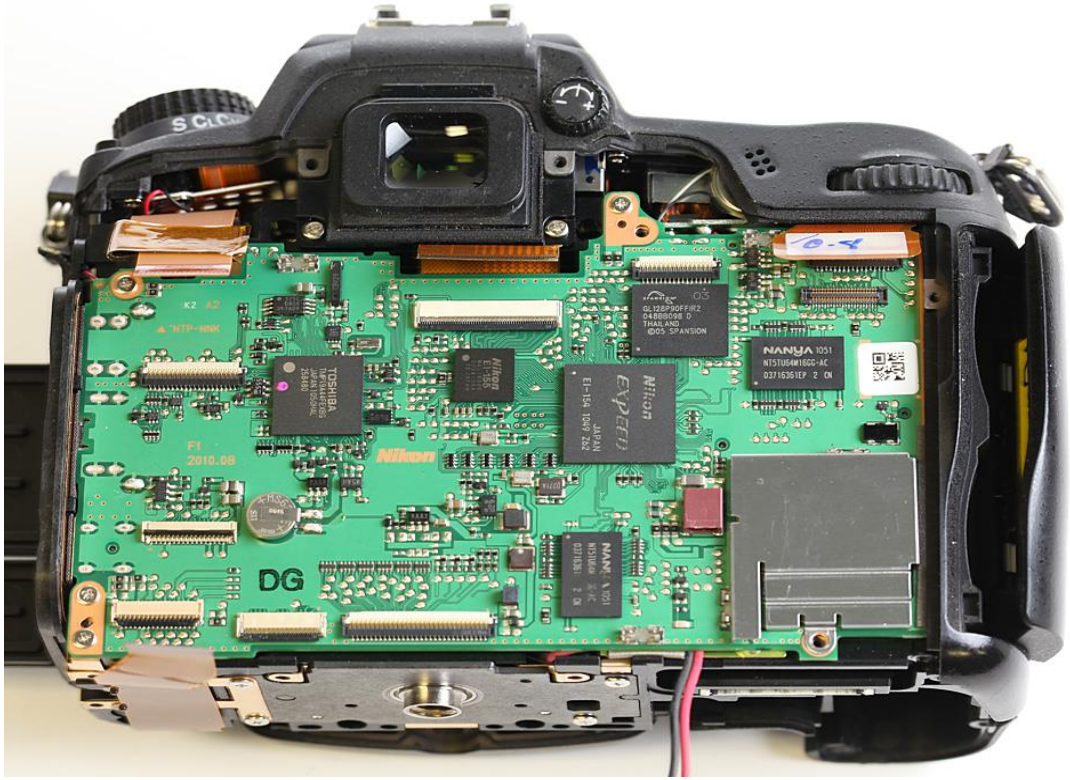
1 Virtex-7 2000T = 4 Largest Monolithic FPGAs

19 Watts 112 Watts

Source: http://low-powerdesign.com/sleibson

Scaling Reduces Cost of Electronics

In 1986: 1.3 megapixels CCD sensor Kodak camera was $13,000. You can buy now for few dollars.

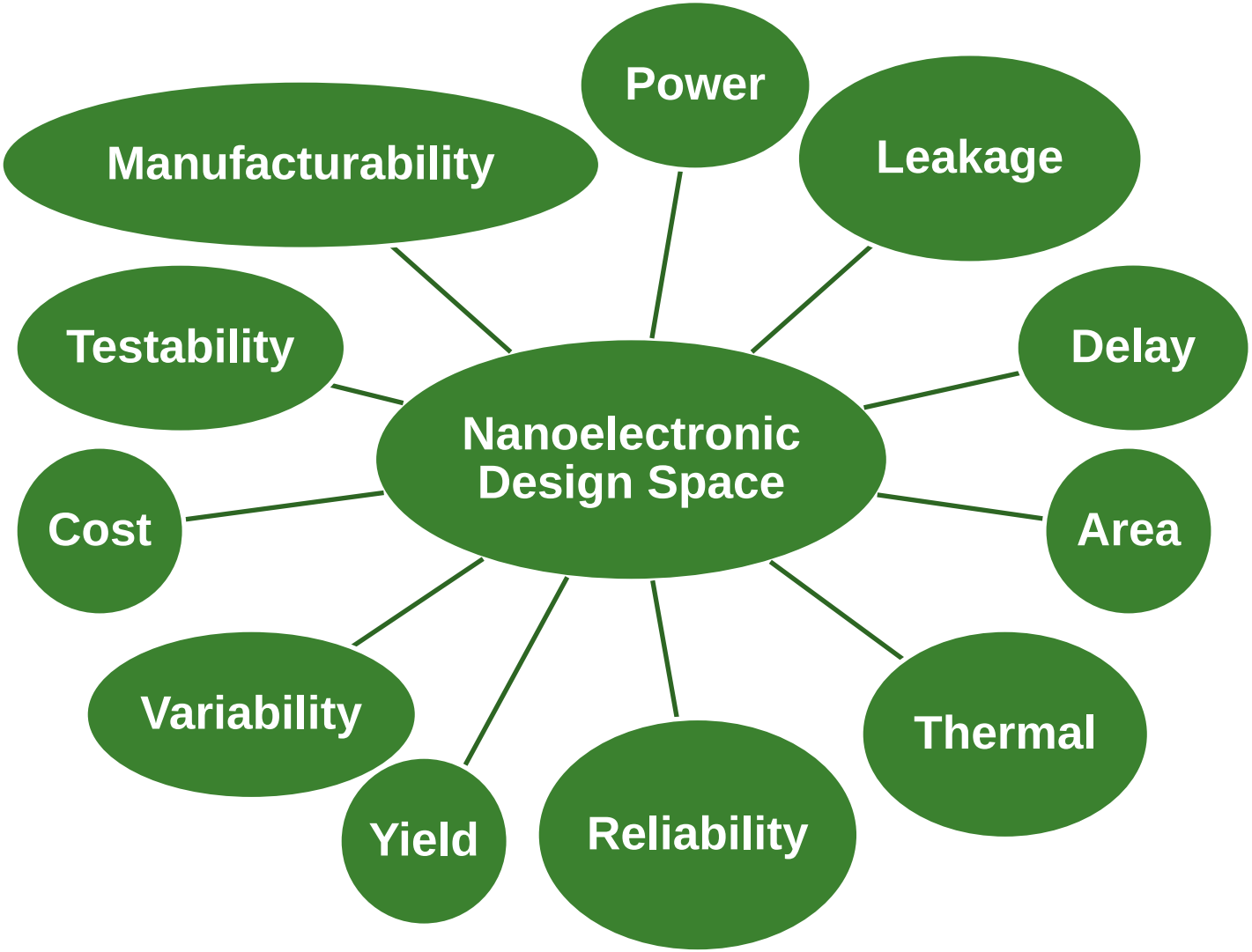


Nikon D7000
DSLR camera.

16 MP → $700

Source: http://www.lensrentals.com/blog/2012/04/d7000-dissection

Nanoelectronics : Challenges

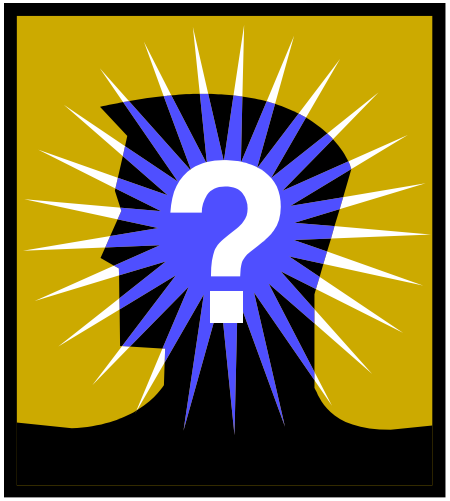


DFX -- Design for X (aka Design for Excellence)

X = set of IC design challenges

- **M**anufacturability
- **P**ower
- **V**ariability
- **C**ost
- **Y**ield
- **R**eliability
- **T**est
- **D**ebug

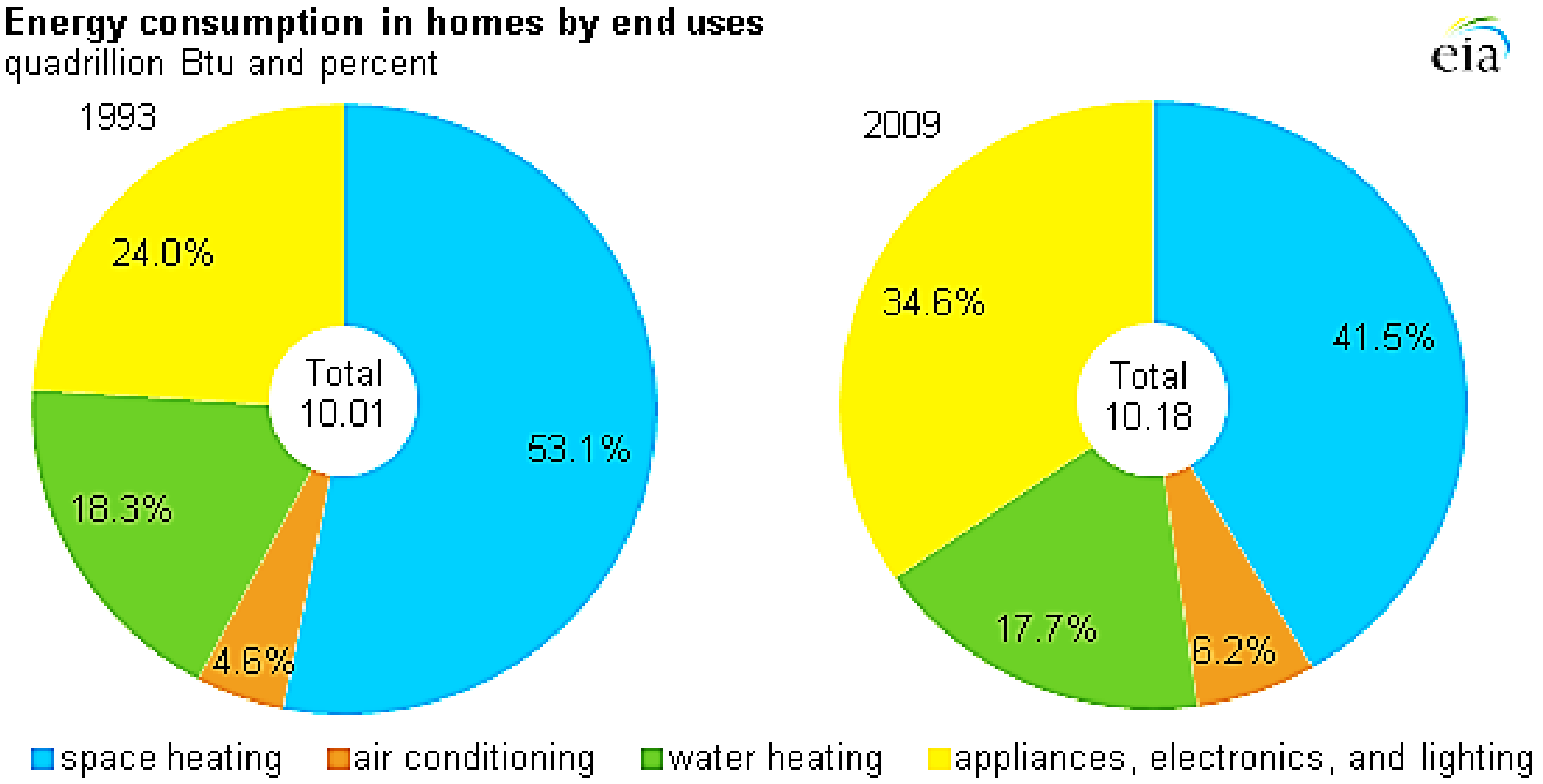
Designers



Source: ISVLSI 2012 Andrew Kahng Keynote

Design for Power

Consumer Electronics Demand More and More Energy



Quadrillion BTU (or quad): 1 quad = 10^{15} BTU = 1.055 Exa Joule (EJ).

Source: U.S. Energy Information Administration.

Different Electronic Systems: Common Story

- Smarter … Faster … High Throughput …

→ Power Hungry !! Battery Hungry !!

Battery Dependency: Not Overstated

One 787 Battery:
12 Cells / 32 V DC

- Boeing 787's across the globe were grounded in early 2013.

Source: http://www.newairplane.com

Battery Dependency: Can't Overemphasized

- Battery-powered phase was planned for about 64 hours.
- Solar cells used for recharging battry provided only half of power what is needed for recharging due to rough landing.

Surface of the Churyumov-Gerasimenko comet is seen from the Philae lander of European Space Agency

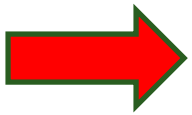
Source: http://www.businessweek.com/news/2014-11-14/scientists-may-try-to-move-comet-lander-as-battery-wanes

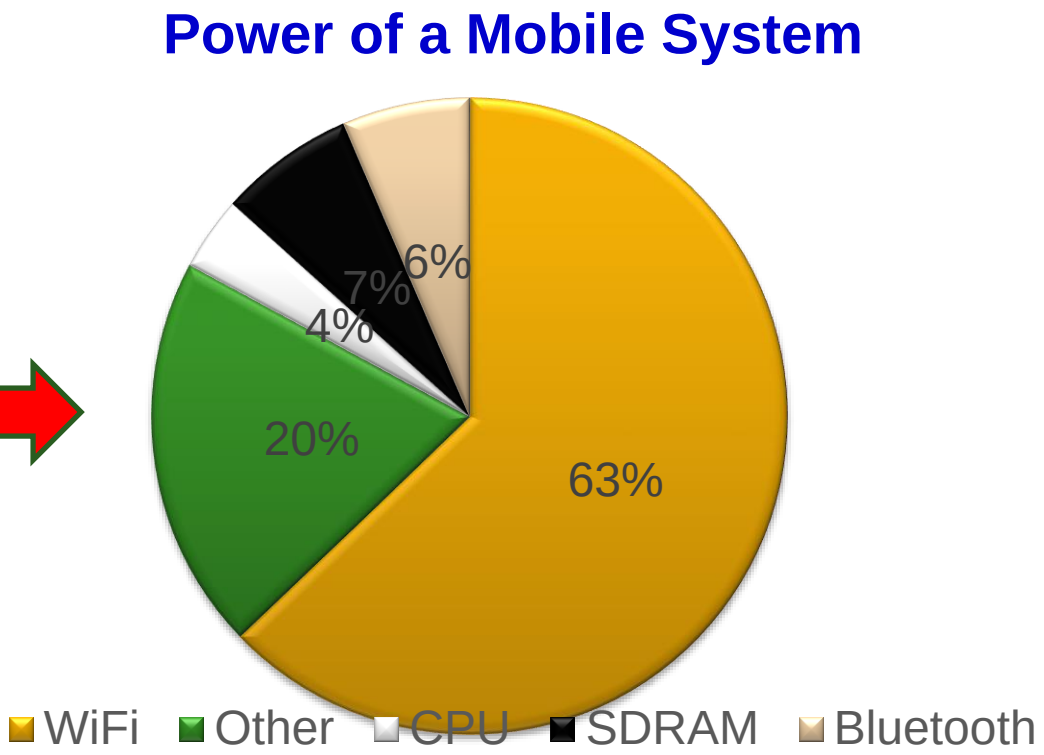
Battery Dependency: Not Overstated

- Great idea: Smartwatch with functioning like smartphone.
- Big Problem: Battery life of one time charging is only 1 day.

Source: http://www.businessinsider.com

A Typical Electronic System: Where Energy Consumed??

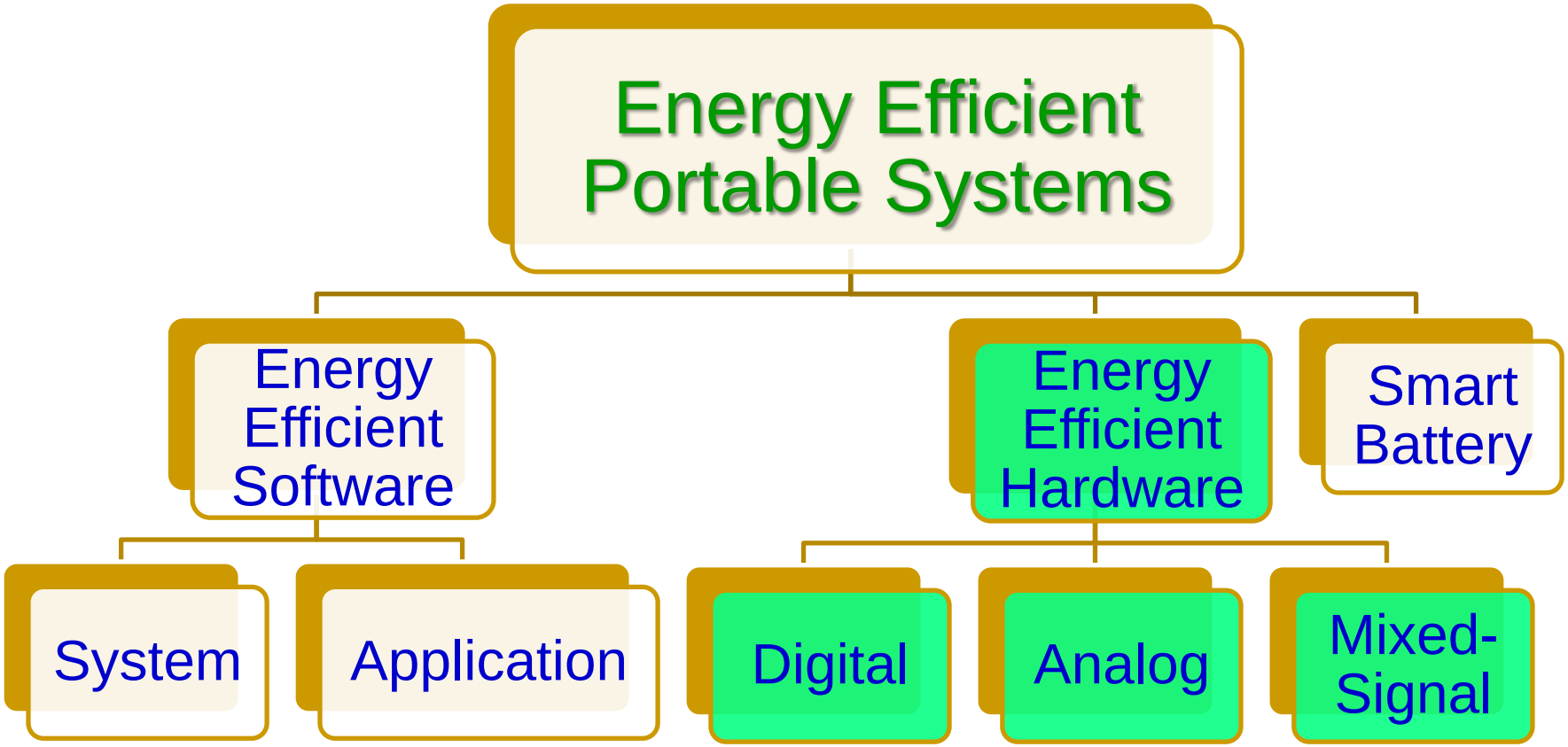




Power dissipation breakdown in idle mode of a connected mobile device

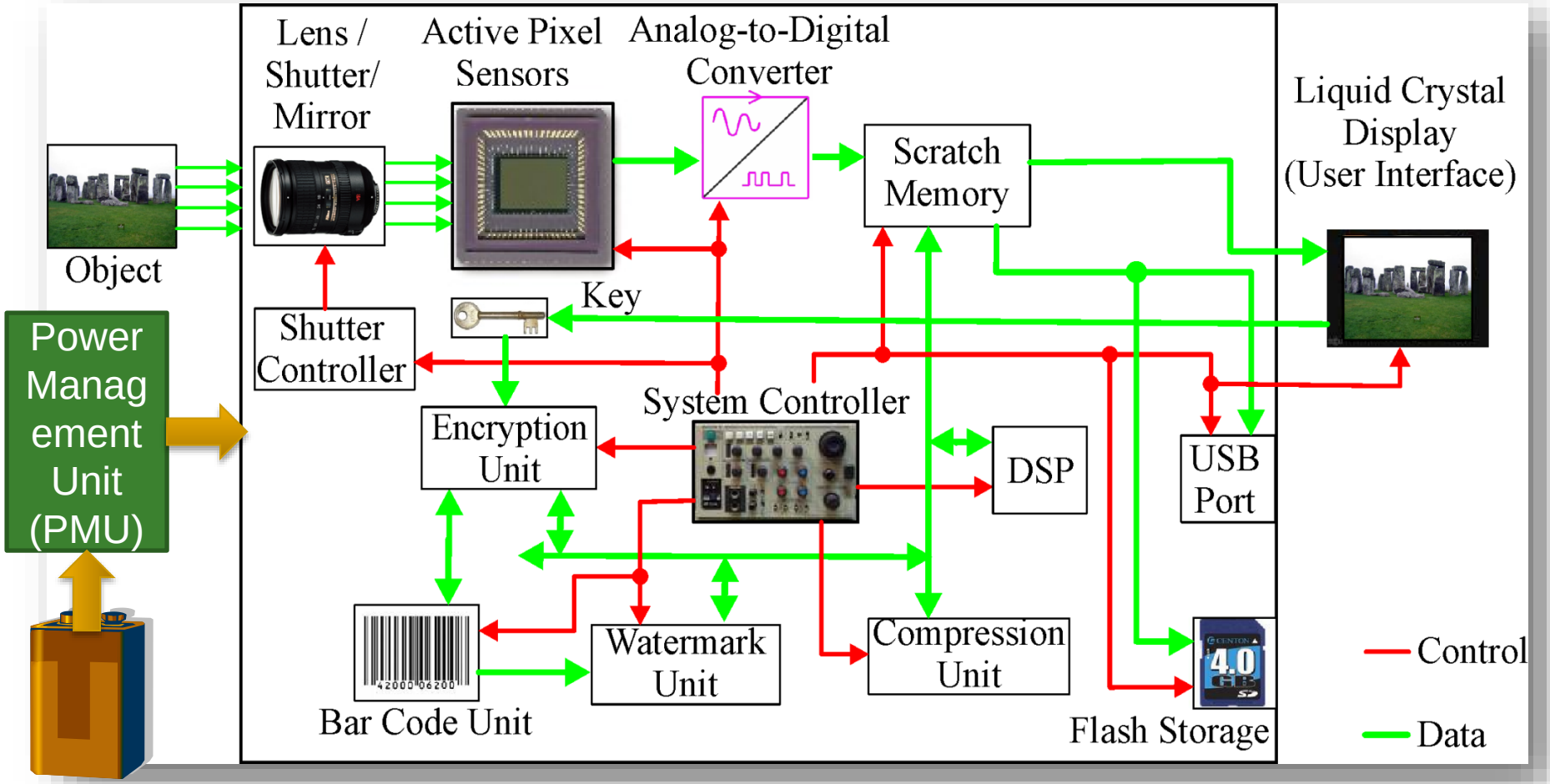
Source: Pering MobiSys 2006

DfP: Possible Solution Fronts

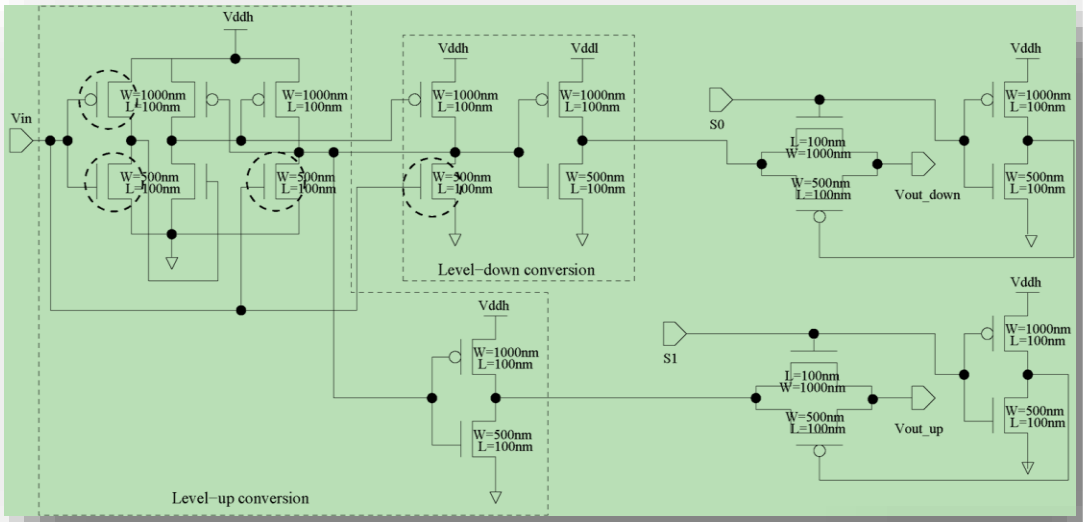


DFP: Design of an Universal Level Converter for Dynamic Power Management

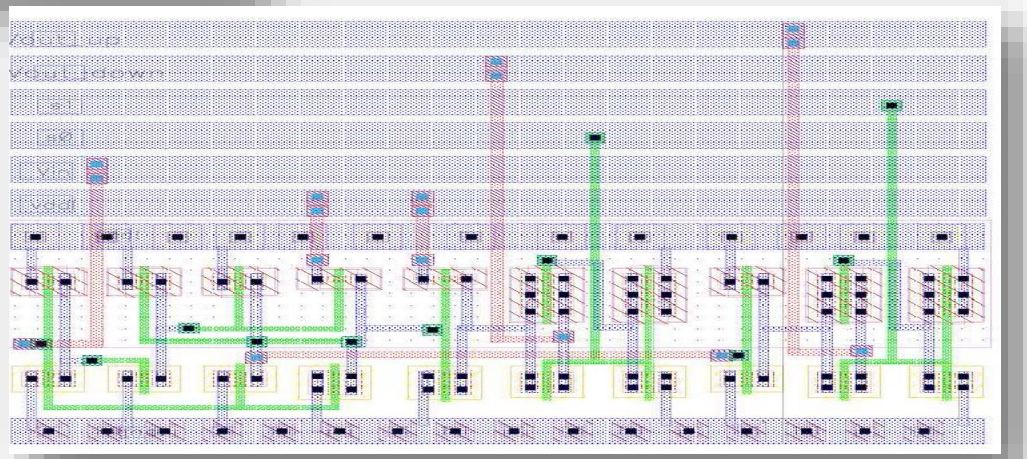
One Example Electronic System: Secure Digital Camera



Universal Voltage-Level Converter: One Topology



- 20 transistor area efficient design.
- Energy hungry transistors are circled.



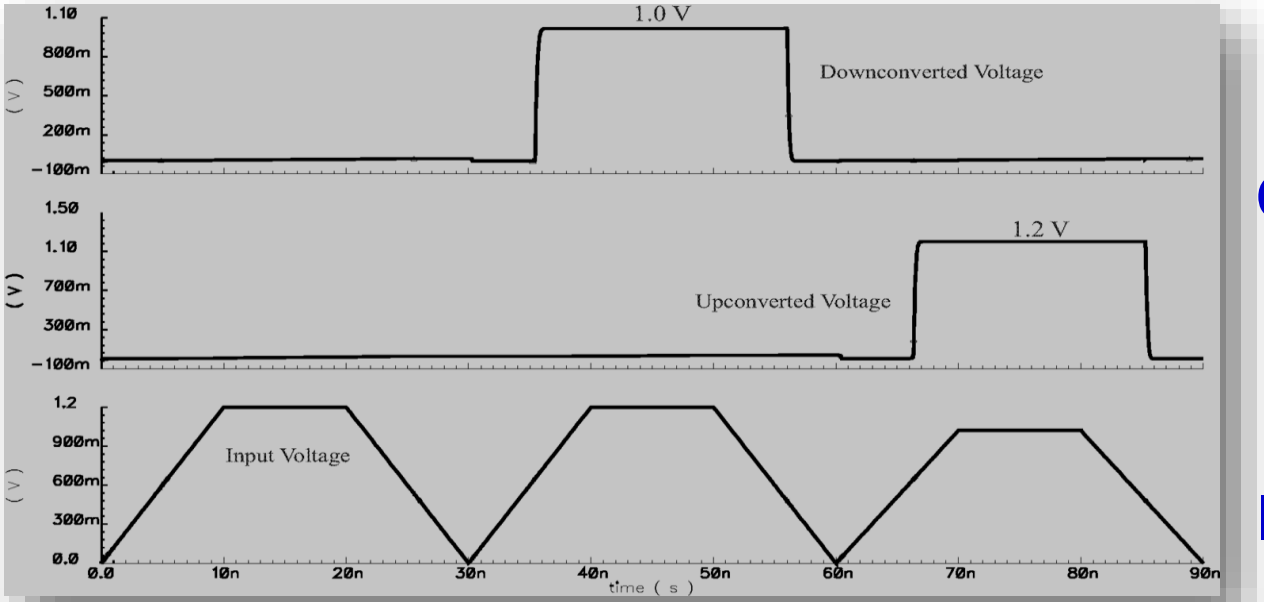
- Energy hungry transistors have thicker oxide.
- 90nm CMOS dual-oxide physical design of ULC.

Universal Voltage-Level Converter: Operations

Operations of the ULC:

- Level-up conversion
- Level-down conversion
- Blocking of input signal

Select Signal		Type of Operation
0	0	Block Signal
0	1	Up Conversion
1	0	Down Conversion



Output

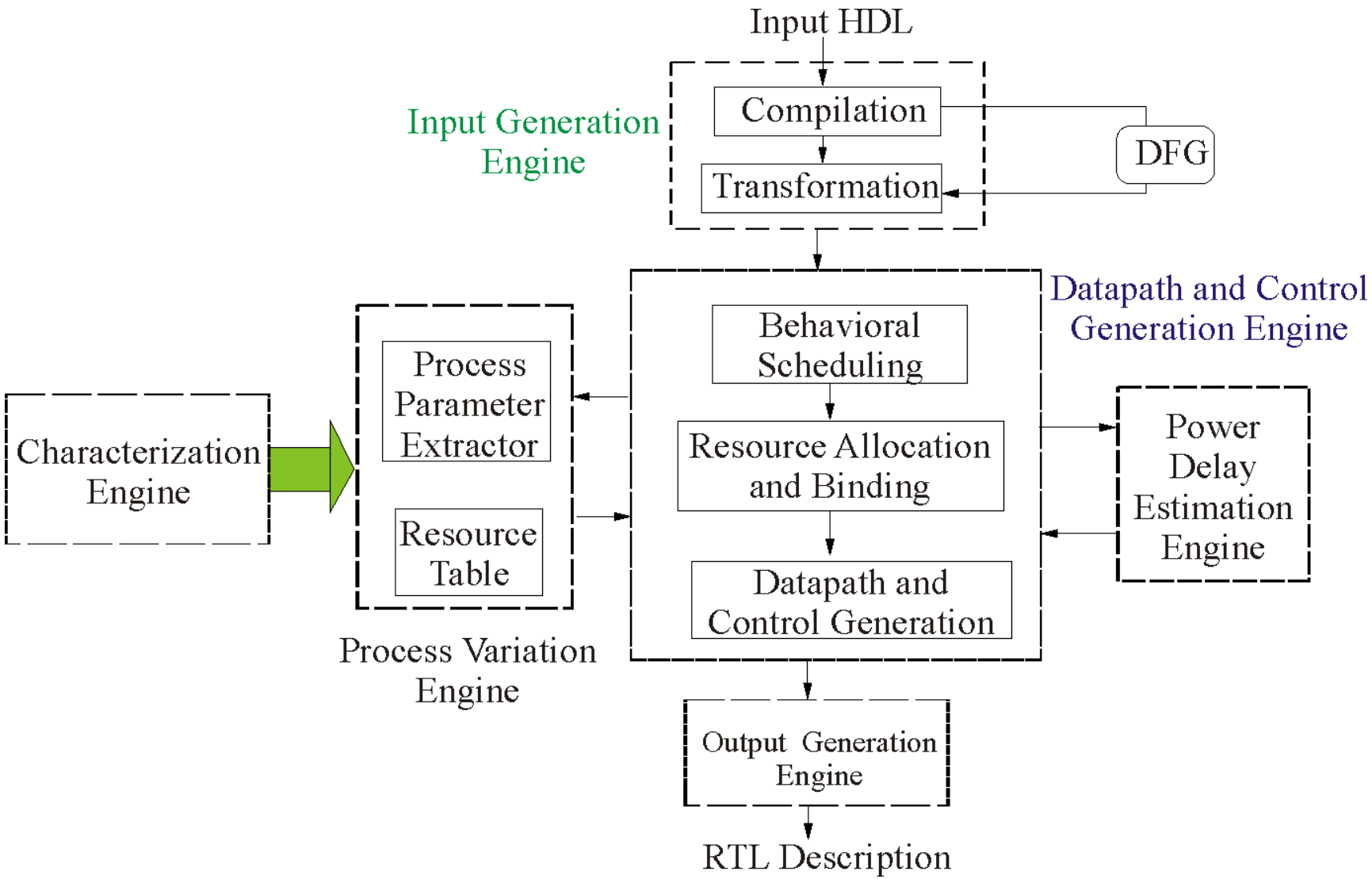
Input

Universal Voltage-Level Converter: Has Minimal Overhead

Designs	Technology (nm)	Power	Delay	Conversion	Design Approach
Ishihara 2004	130nm	---	127 ps	Level-up and down	Level converting flip flops
Yu 2001	350nm	220.57 µW	---	Level-up	SDCVS
Sadeghi 2006	100nm	10 µW	1 ns	Level-up	Pass transistor and Keeper transistor
ULC	90 nm	12.26 µW	113.8 ps	Level-up/down and block	All conversion types and Programmable

DFC/DFV: Statistical Nano-CMOS RTL Optimization for Power

Nano-CMOS RTL Statistical Optimization



Statistical RTL Optimization: Formulation

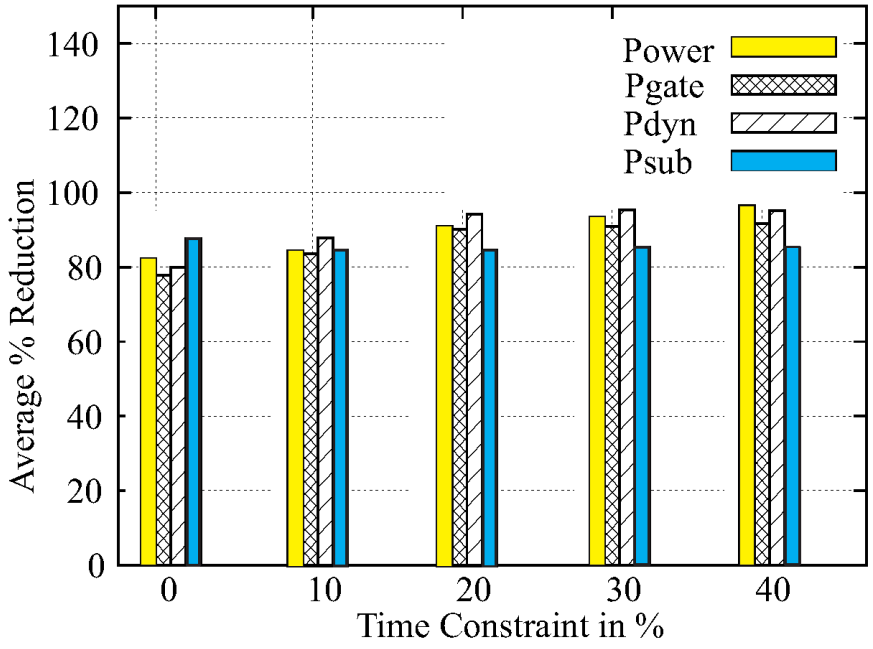
Minimize: $FoM_{Total}^{DFG}\left(\mu_I^{DFG}, \sigma_I^{DFG}\right)$

Subjected to (Resource/Time Constraints):

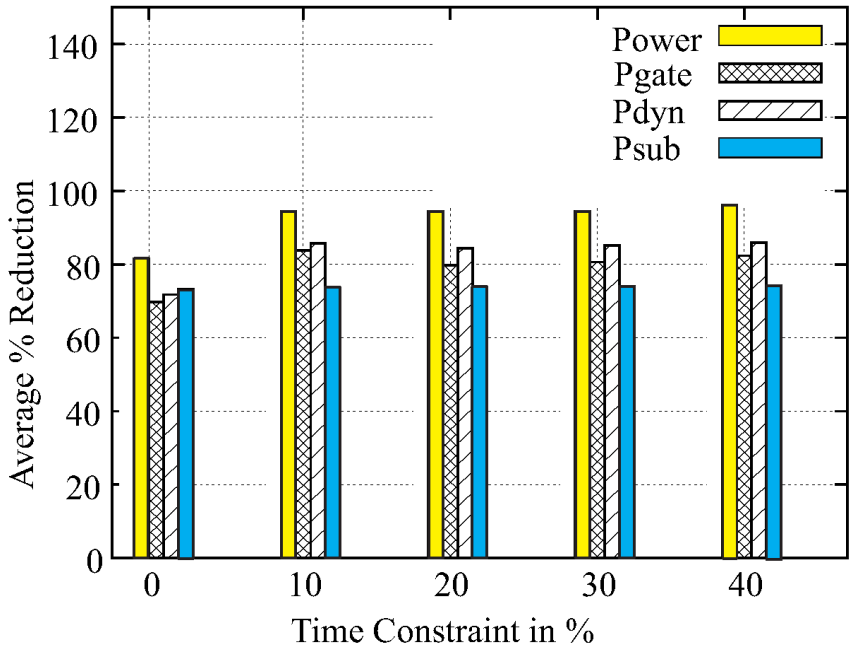
$$\text{Allocated}\left(FU_{k,i}\right) \le \text{Available}\left(FU_{k,i}\right), \forall \text{cycle} c$$

$$D_{CP}^{DFG}\left(\mu_D^{DFG}, \sigma_D^{DFG}\right) \le D_{Con}\left(\mu_D^{Con}, \sigma_D^{Con}\right)$$

Statistical RTL Optimization: Results on DSP Benchmarks



(For ARF Benchmark)

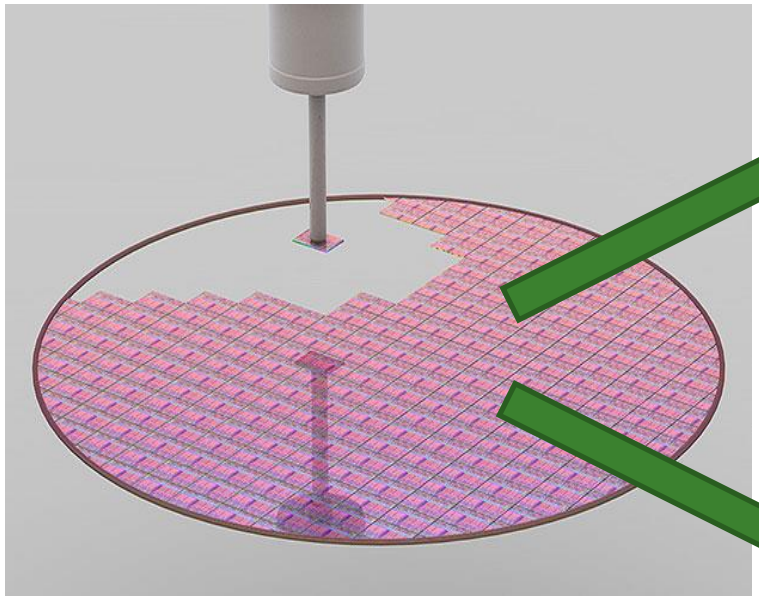


(For BPF Benchmark)

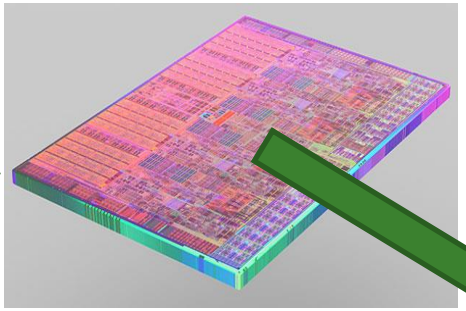
Design for Variability (DFV)

Nanoelectronics Variability ?

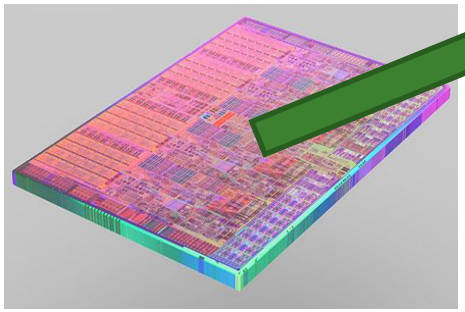
- Discrepancy between the chip parameters --
  Design Time versus Actual Post Fabrication

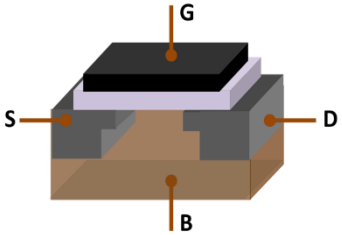


Same Design Fabricated

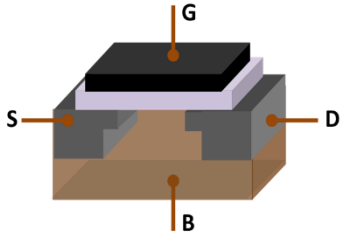


Each Chip has
Different Performance



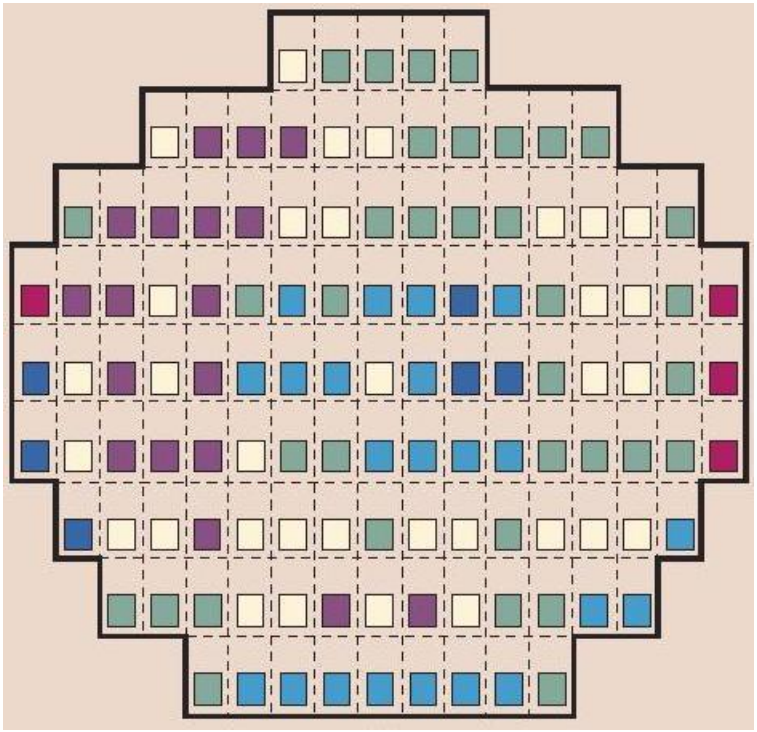


Each Transistor
is Different

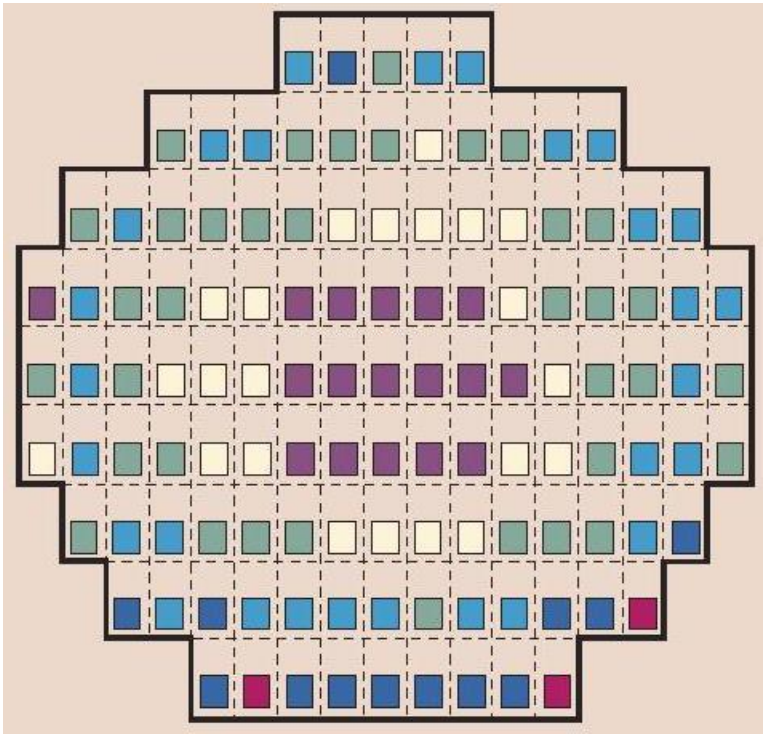


Source: http://apcmag.com/picture-gallery-how-a-chip-is-made.htm

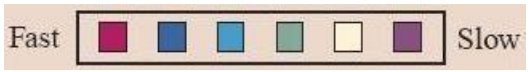
Process Variation: Parameters



Source–drain resistance is different for different chips in a same die.



Gate-to-source and gate-to-drain overlap capacitance is different for different chips in a same die.

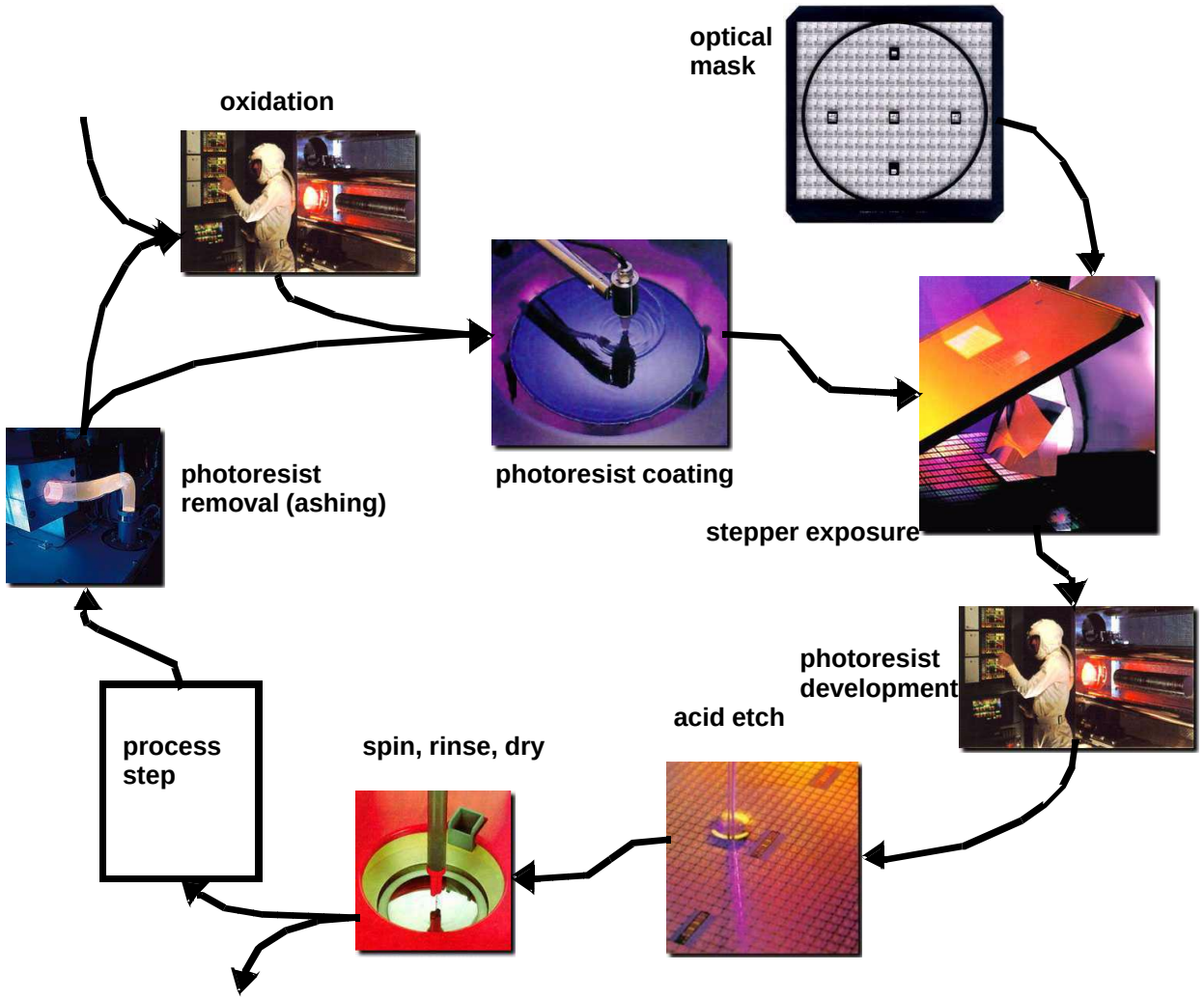


Source: Bernstein et al., IBM J. Res. & Dev., July/Sep 2006.

Process Variation: The Impact

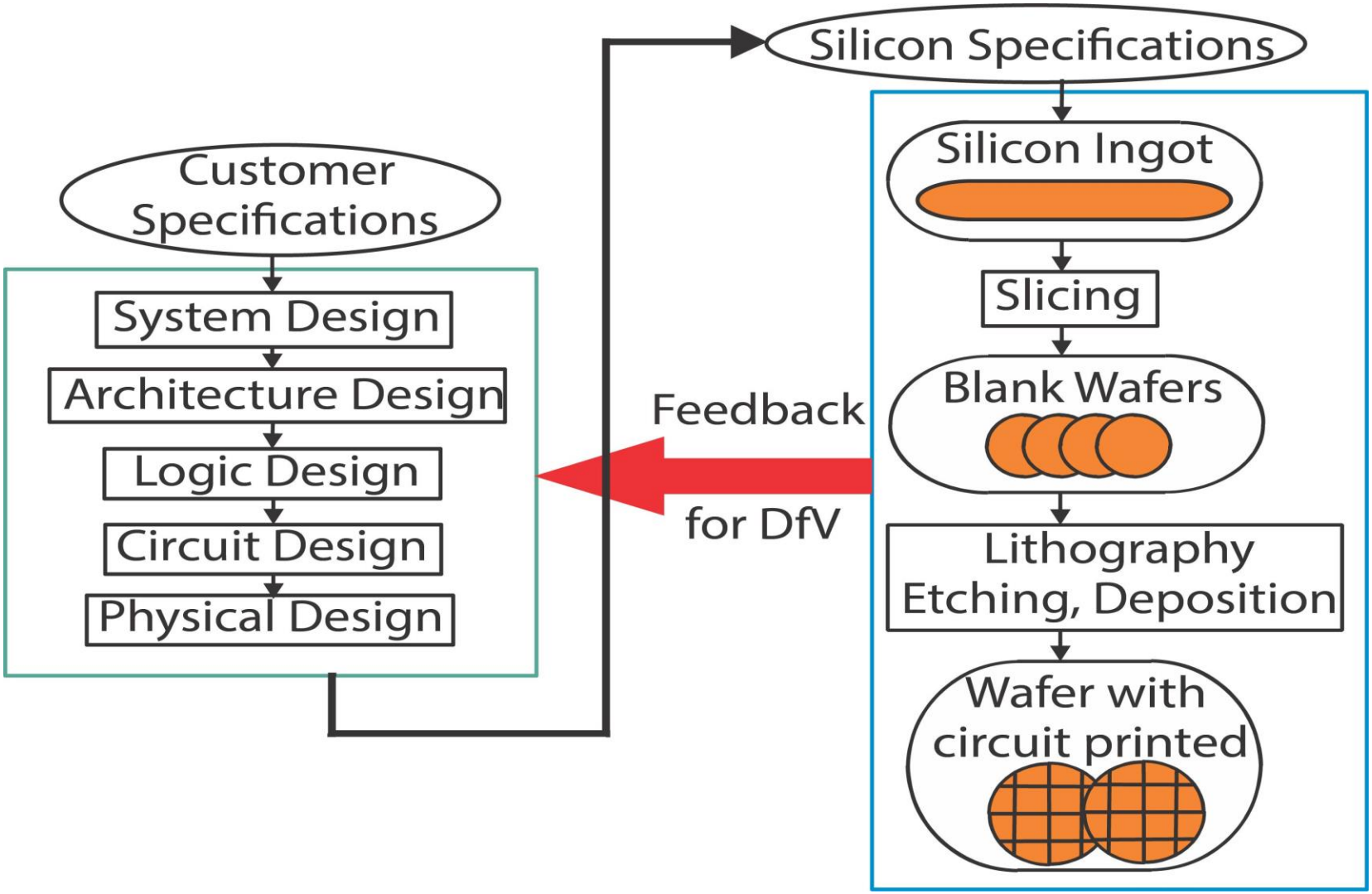
- Yield Loss
- Reliability Issue
- Higher Cost

Process Variation: Sources

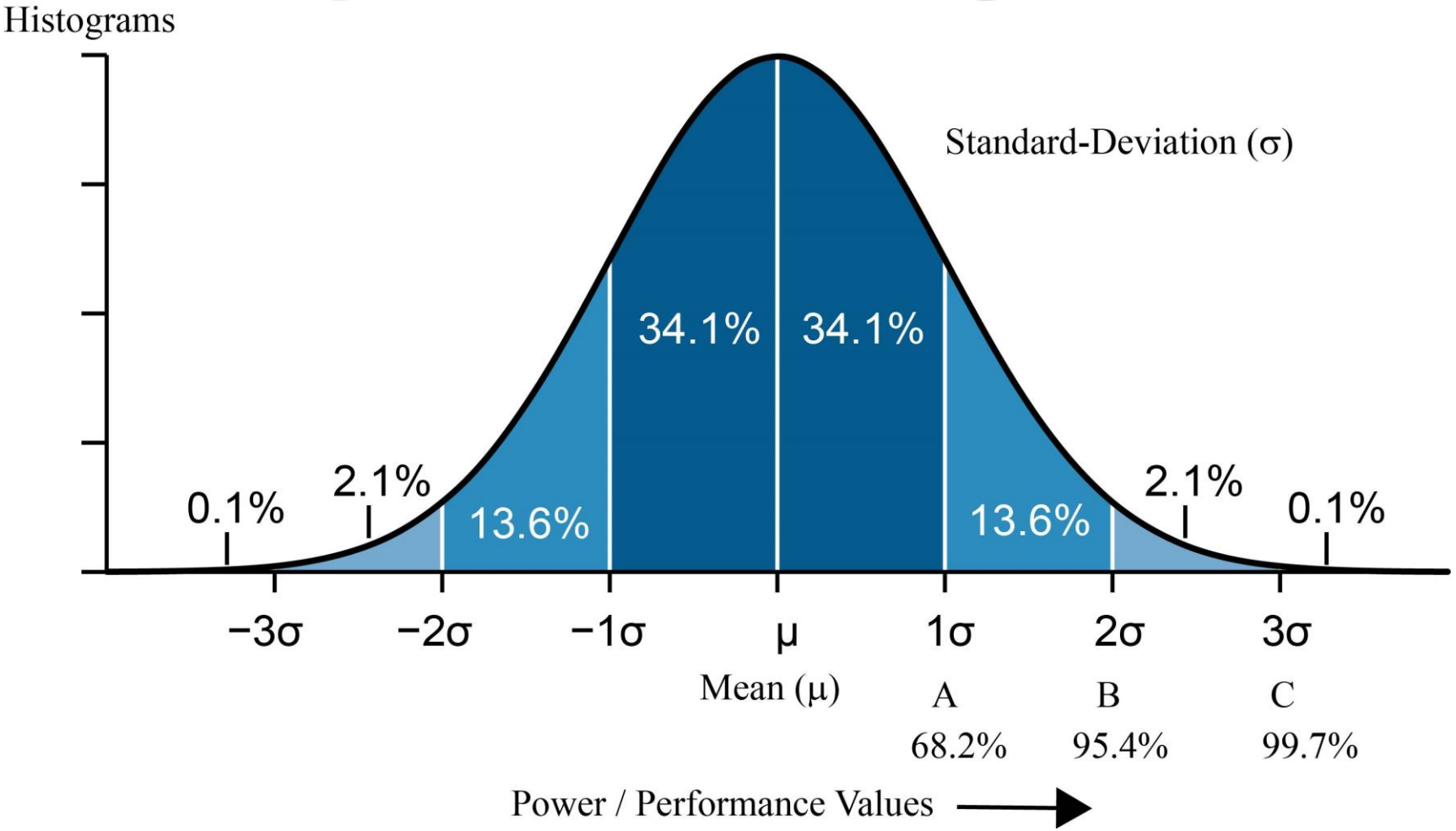


Sophisticated Lithography

Process Variations : Solution

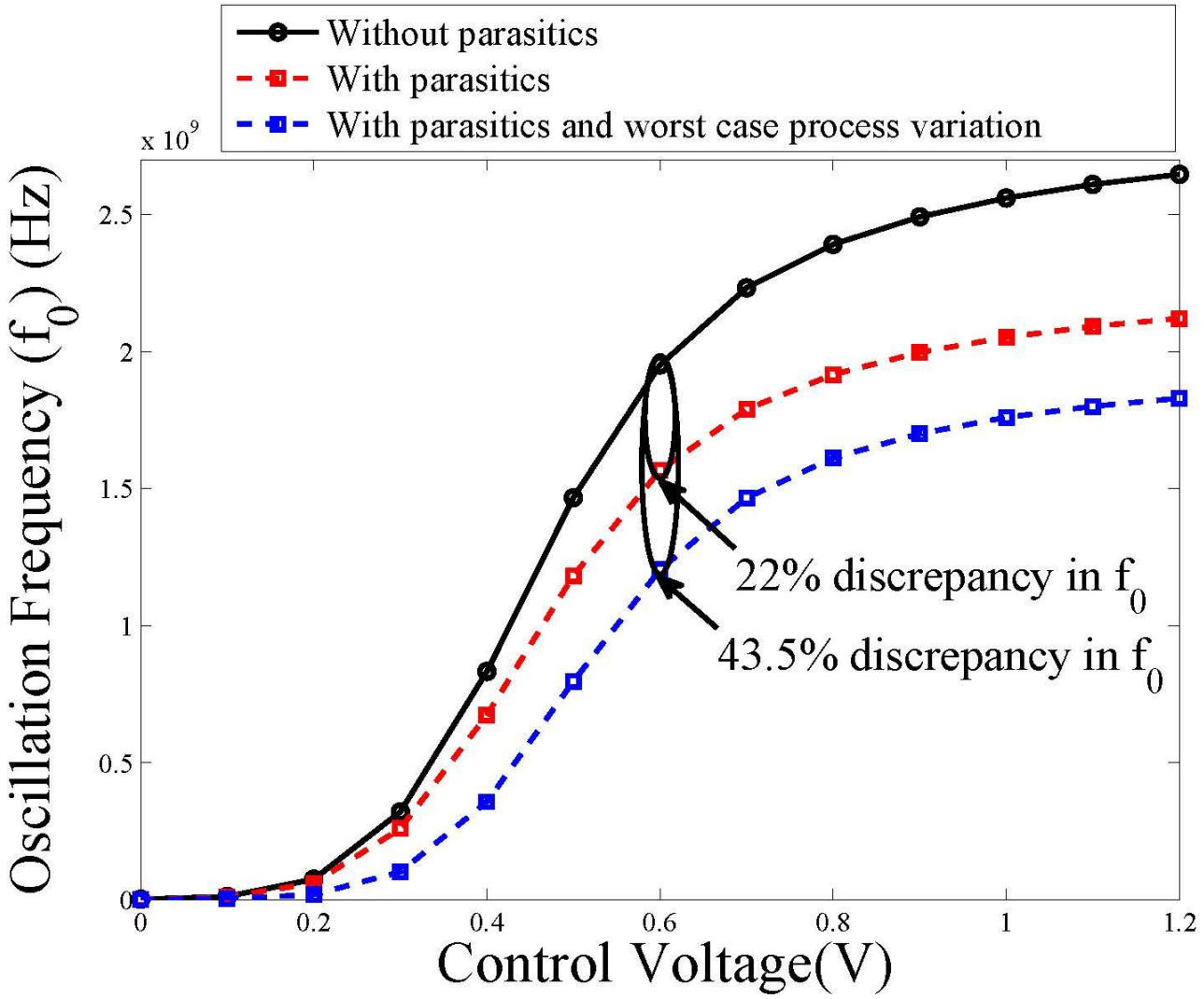


Process Variations Aware Optimization: Key Idea

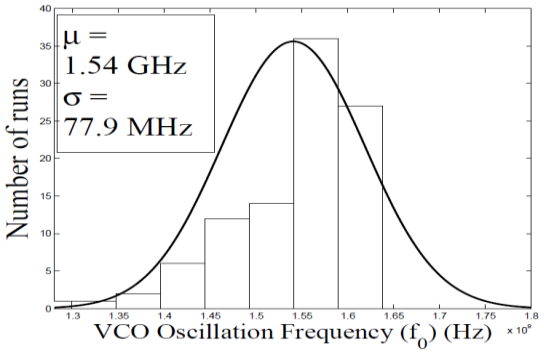


DFV: Statistical Nano-CMOS Physical Design Optimization

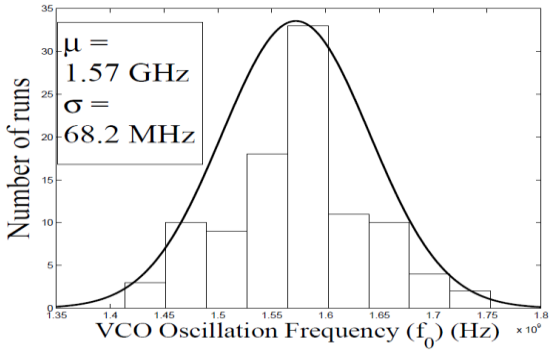
Variability Effects: VCO Case Study



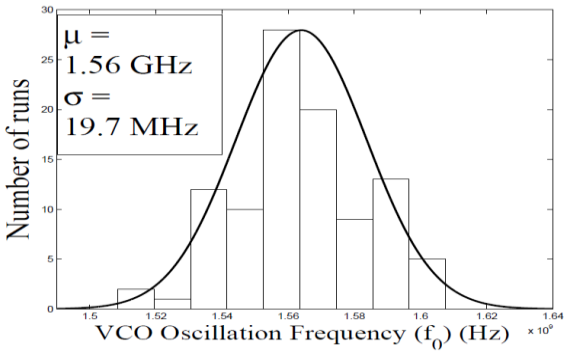
Variability Effects: VCO Case Study



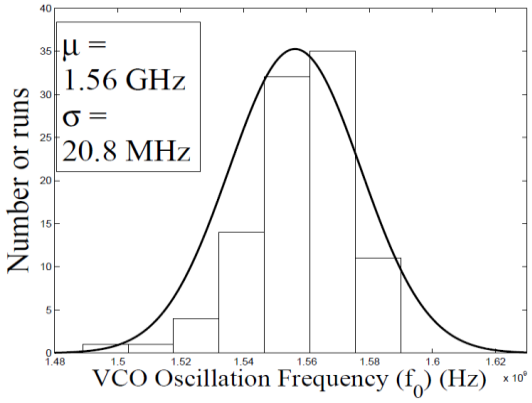
- V_{dd}



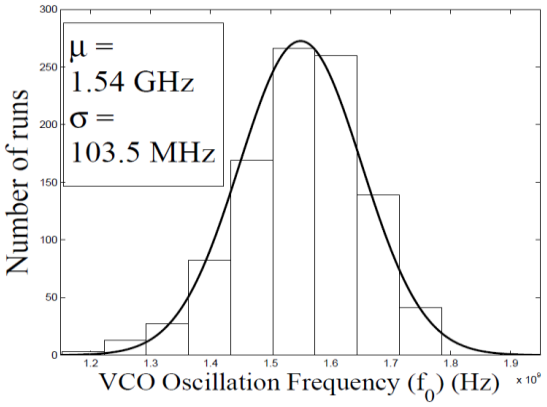
- V_{Tnmos}



- V_{Tpmos}

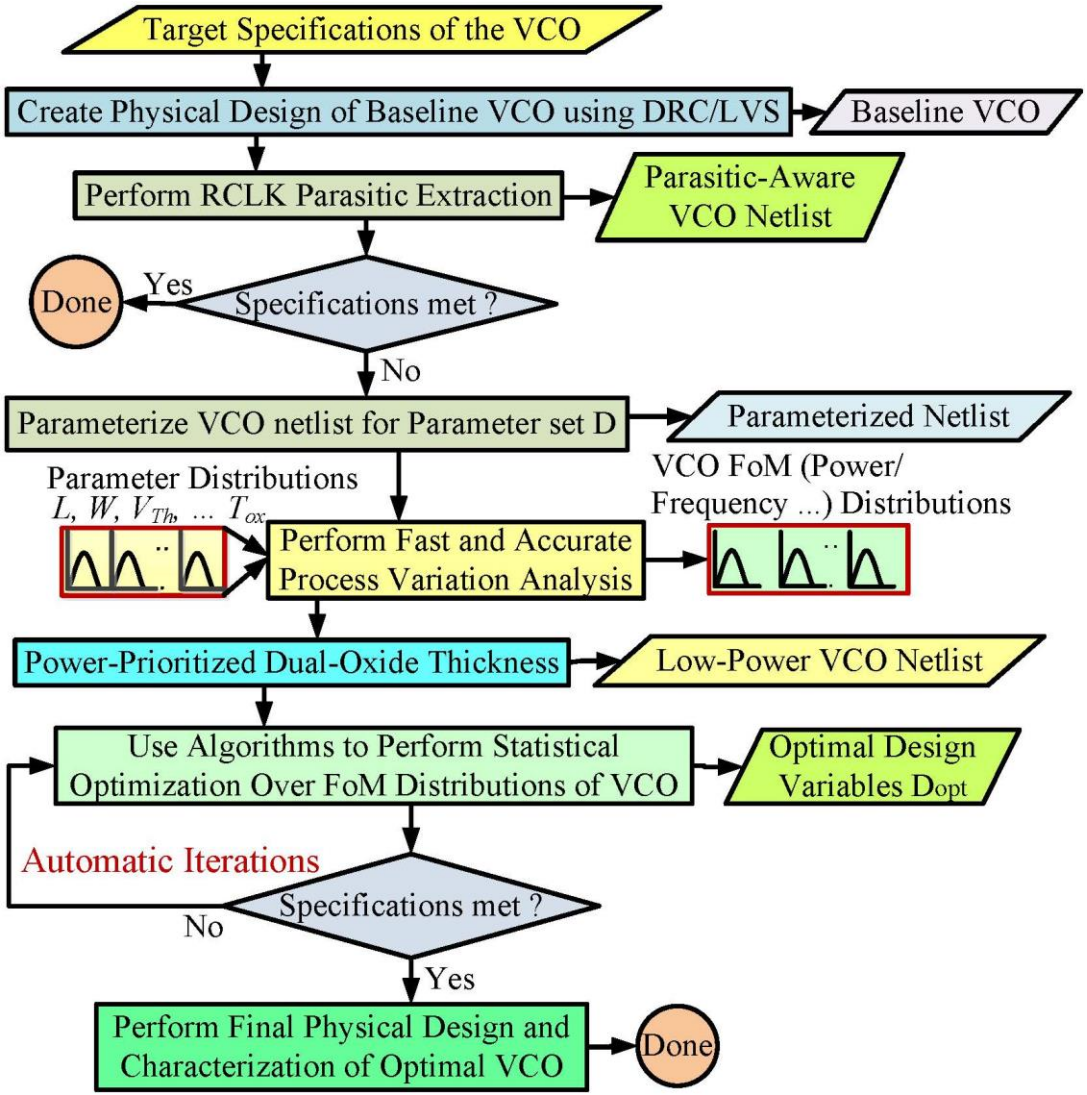


- $T_{oxnmos} + T_{oxpmos}$

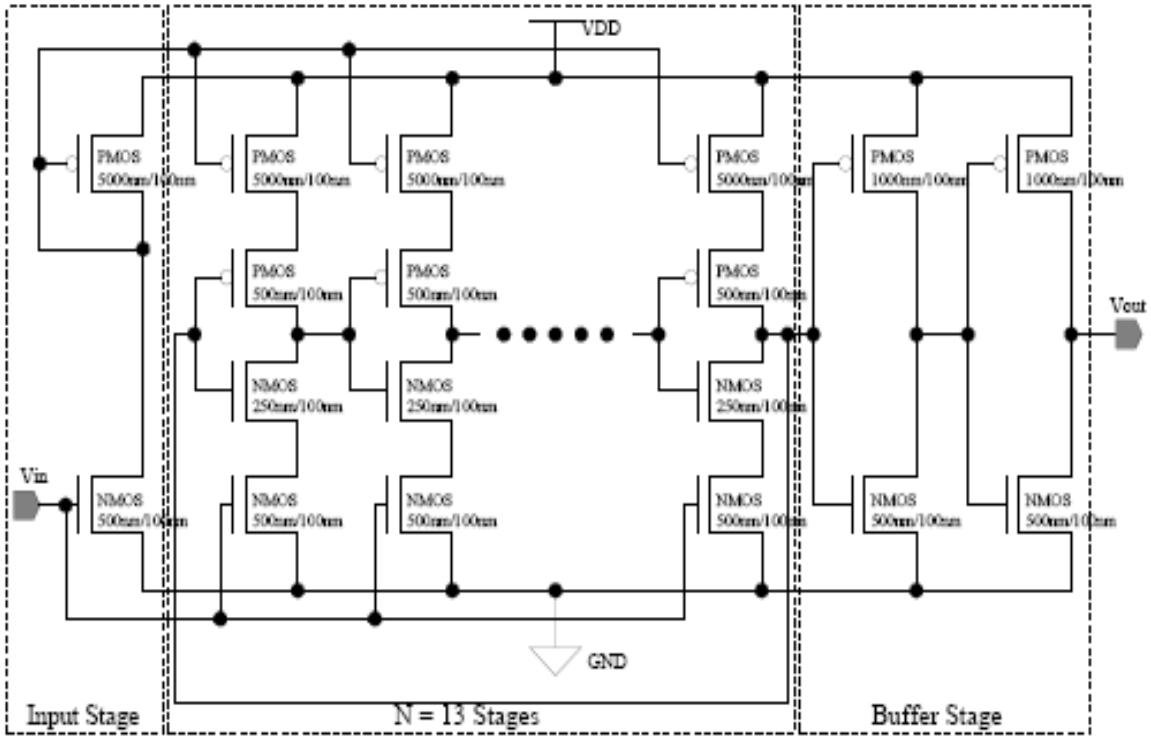


- $V_{dd} + V_{Tnmos} + V_{Tpmos} + T_{oxnmos} + T_{oxpmos}$

Variability Aware Optimization Flow



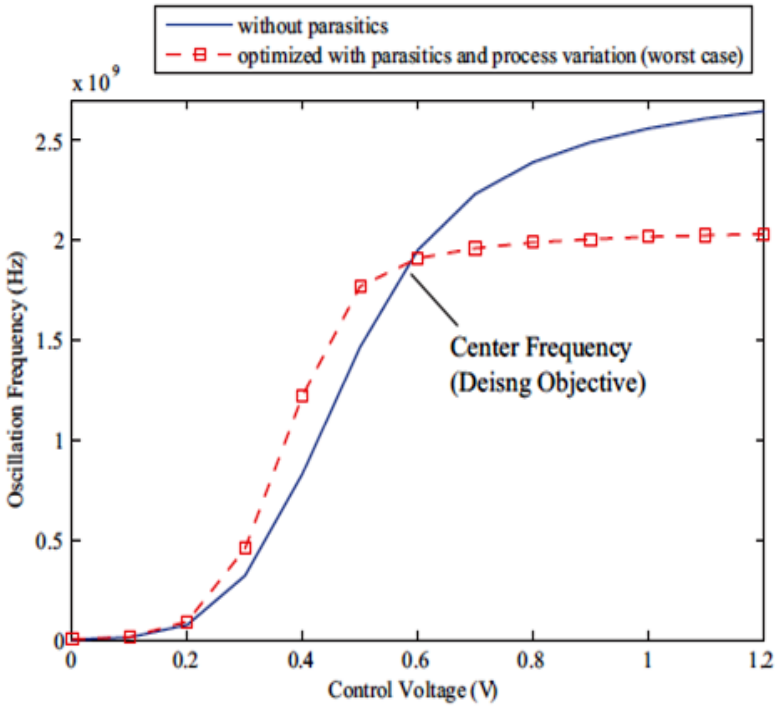
Variability Aware Optimization Flow



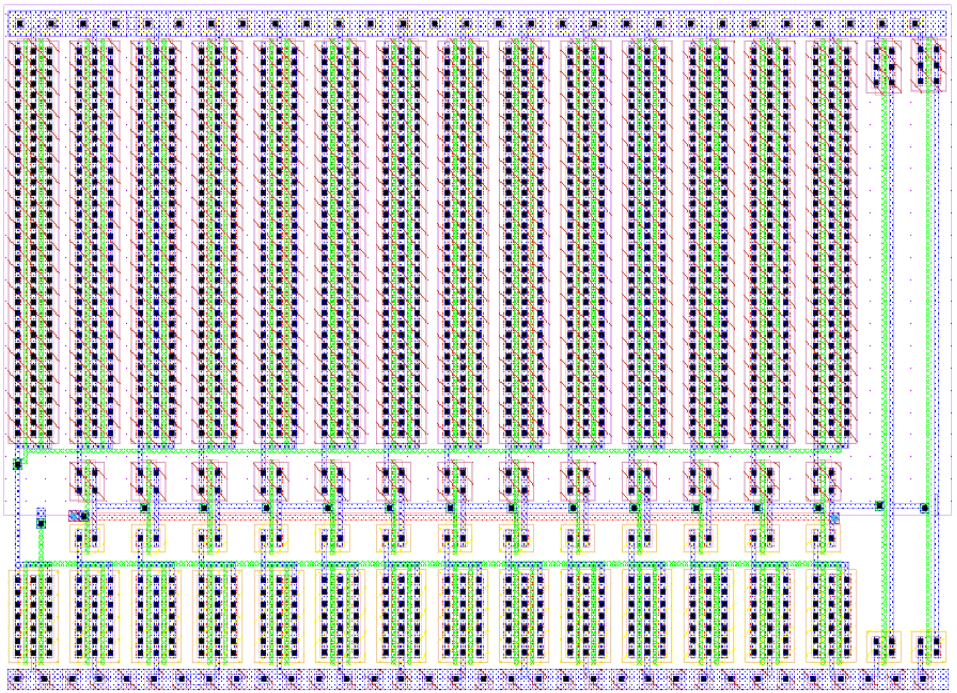
- Current Starved VCO

Parameter	C_{lower}	C_{upper}	$D_{optimal}$
Wn	200 nm	500 nm	415 nm
Wp	400 nm	1µm	665 nm
Wncs	1 µm	5 µm	4 µm
Wpcs	5 µm	20 µm	19 µm
L	100 nm	110 nm	100 nm

Variability Aware Optimization Flow



• Frequency-voltage characteristics of the optimized VCO. Discrepancy reduced to 4.5%

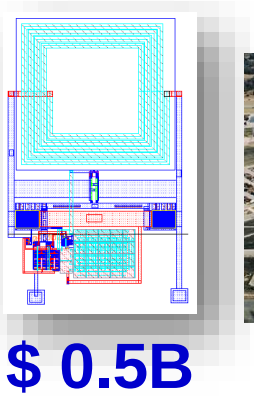


• Final Optimized layout of the VCO (RCLK Extraction carried out)

Design for Cost (DFC)

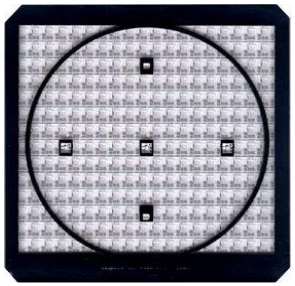
Chip Cost

- Total Chip Cost
  - Non-recurring (NRE)
    - Design
    - Plant Capitalization
    - Masks
  - Recurring
    - Fabrication
    - Packaging
    - Testing

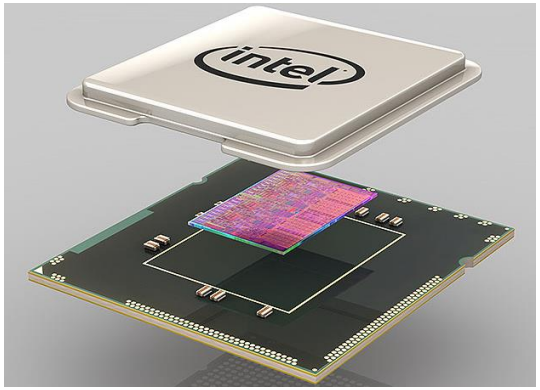


$ 0.5B

$ 5B

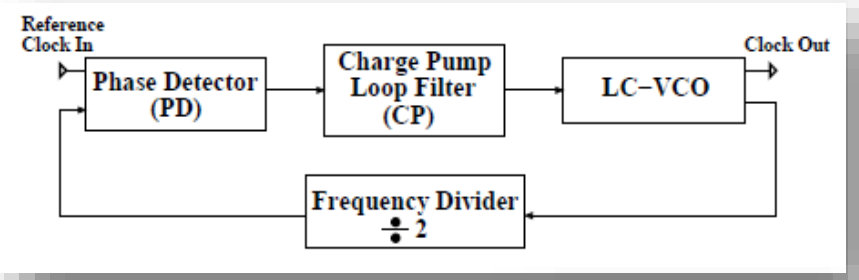


$ 2M



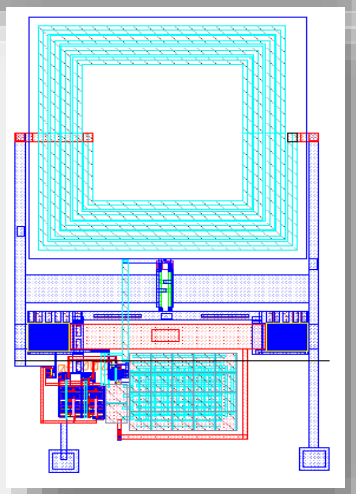
Source: http://www.ami.ac.uk/courses/ami4202_mdesign/u02/

One of the Key Issues: Time/Effort



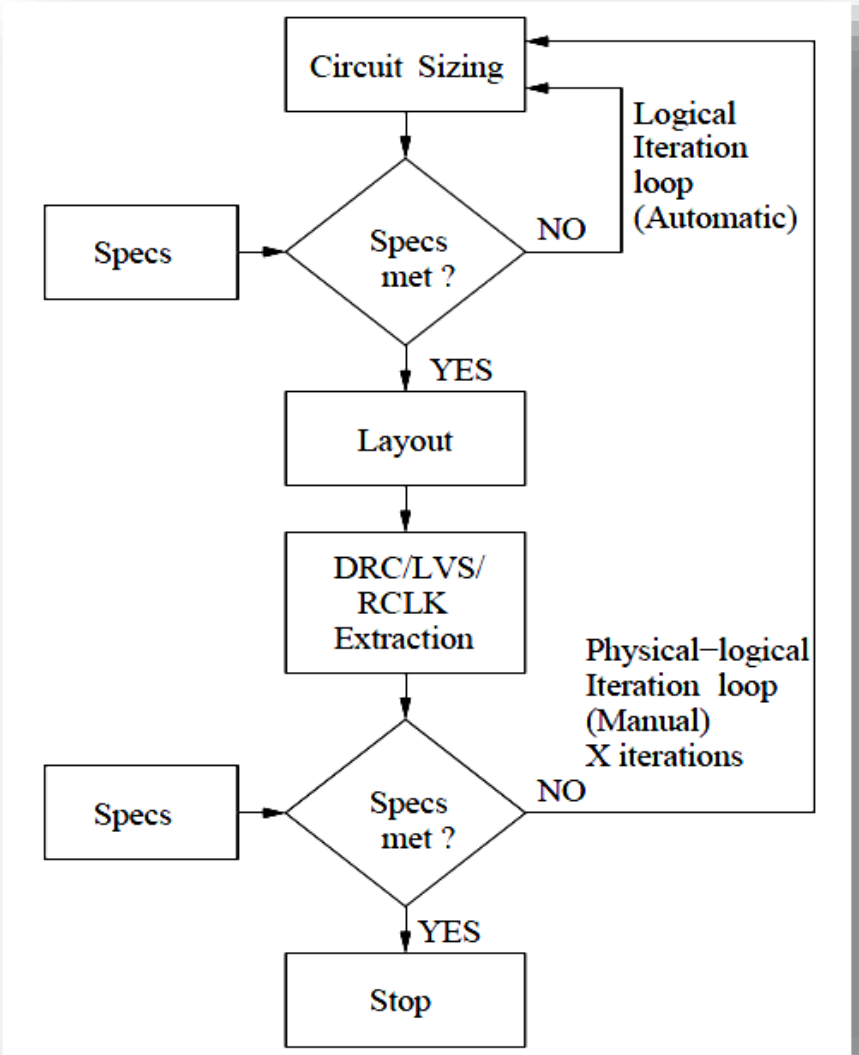
- The simulation time for a Phase-Locked-Loop (PLL) lock on a full-blown (RCLK) parasitic netlist is of the **order of many days**! → High NRE cost.

PLL



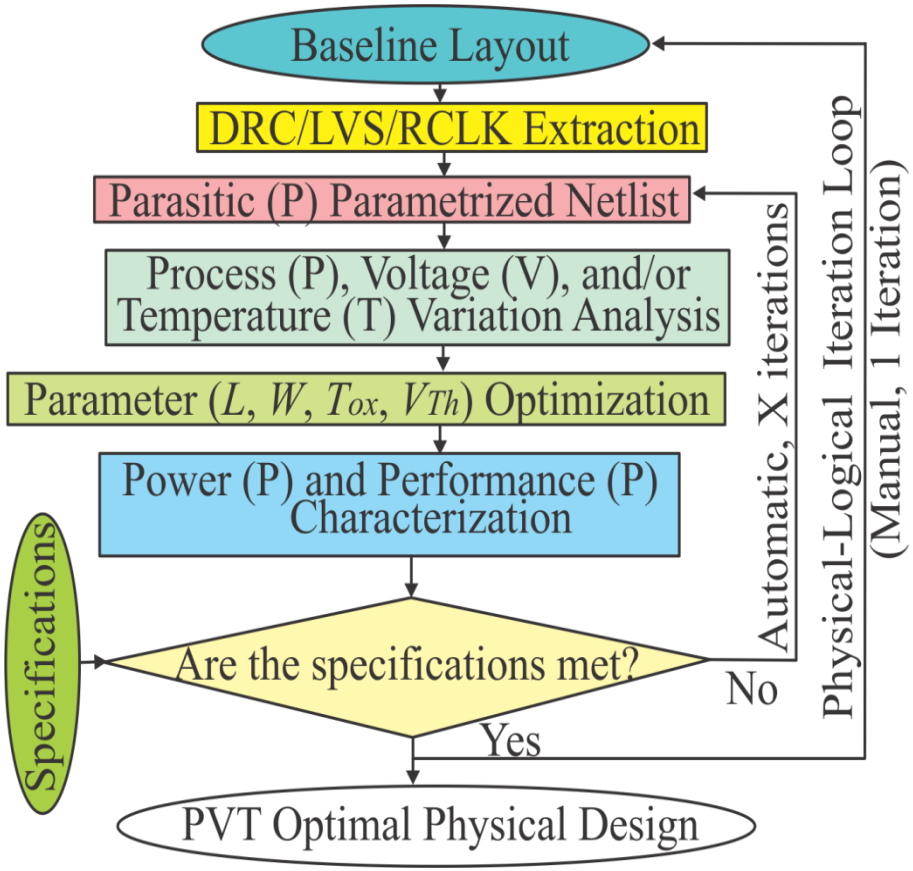
- **Issues for AMS-SoC components:**
  - How fast can design space exploration be performed?
  - How fast can layout generation and optimization be performed?

Standard Design Flow – Very Slow



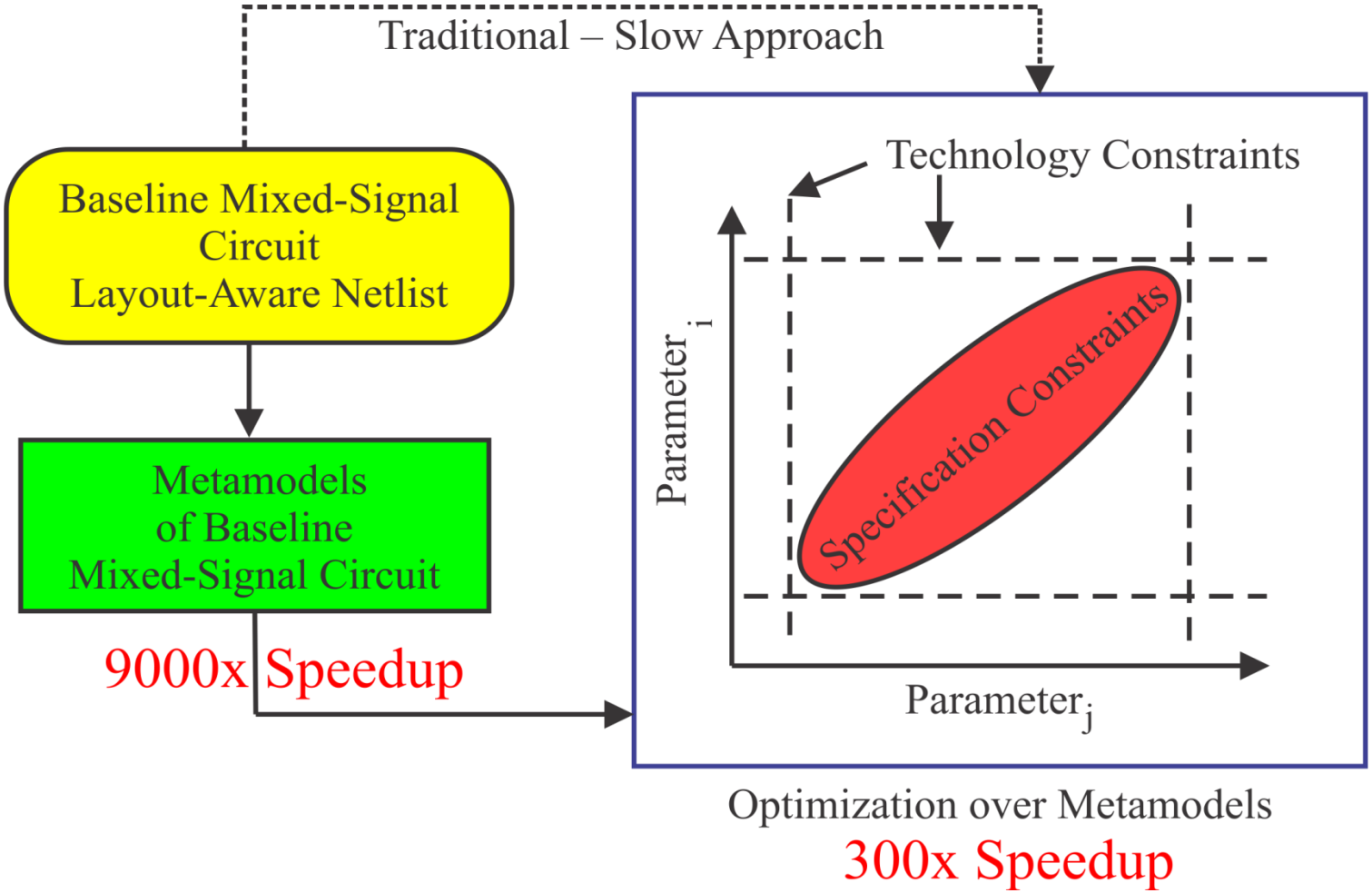
- Standard design flow requires multiple manual iterations on the back-end layout to achieve parasitic closure between front-end circuit and back-end layout.
- Longer design cycle time.
- Error prone design.
- Higher non-recurrent cost.
- Difficult to handle nanoscale challenges.

Automatic Optimization on Netlist (Faster than manual flow; still slow)



- Automatic iteration over netlist improves design optimization.
- Still needs multiple simulations using analog simulator (SPICE).
- SPICE is slow.

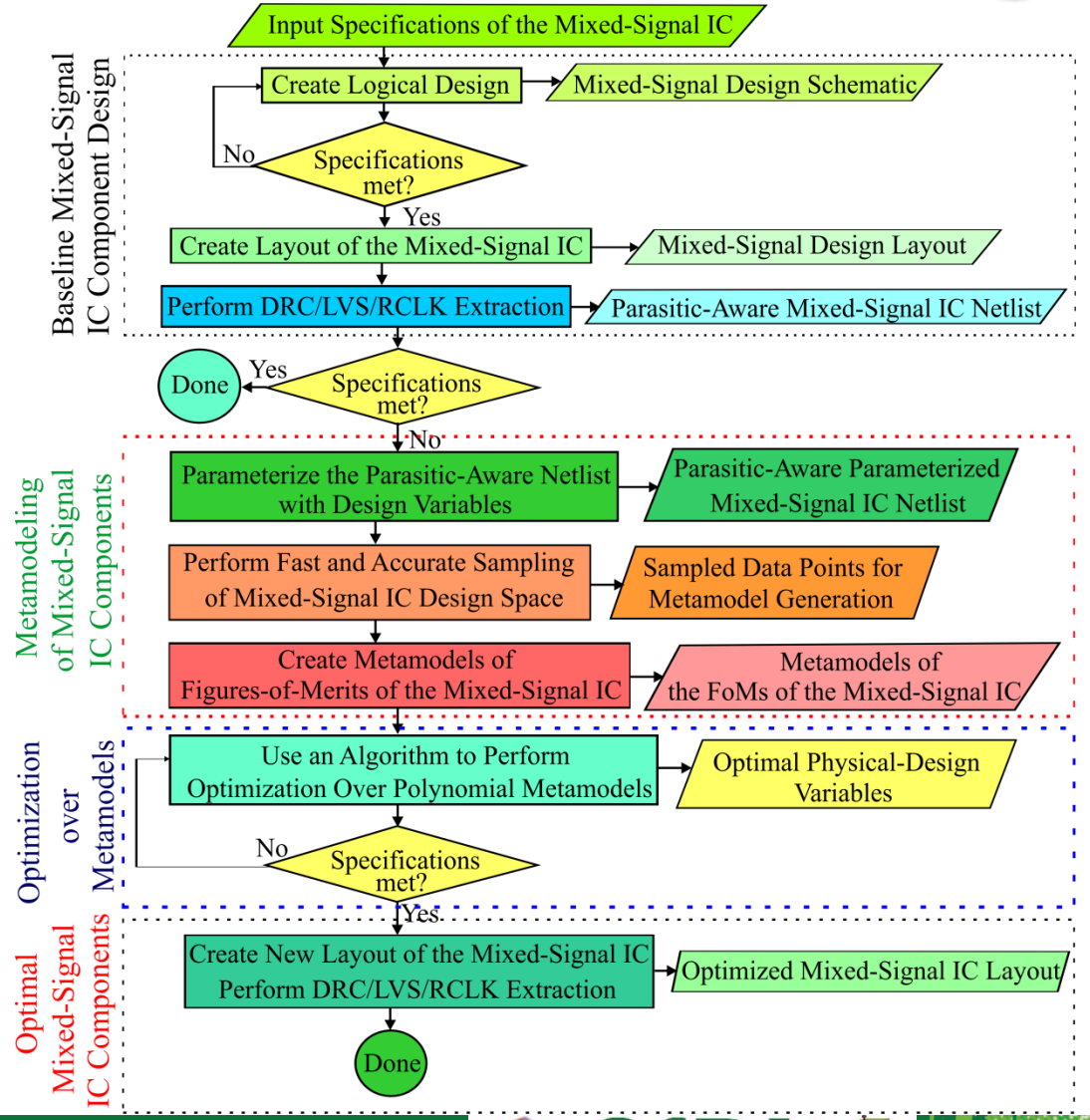
Two Tier Speed Up Through Metamodel



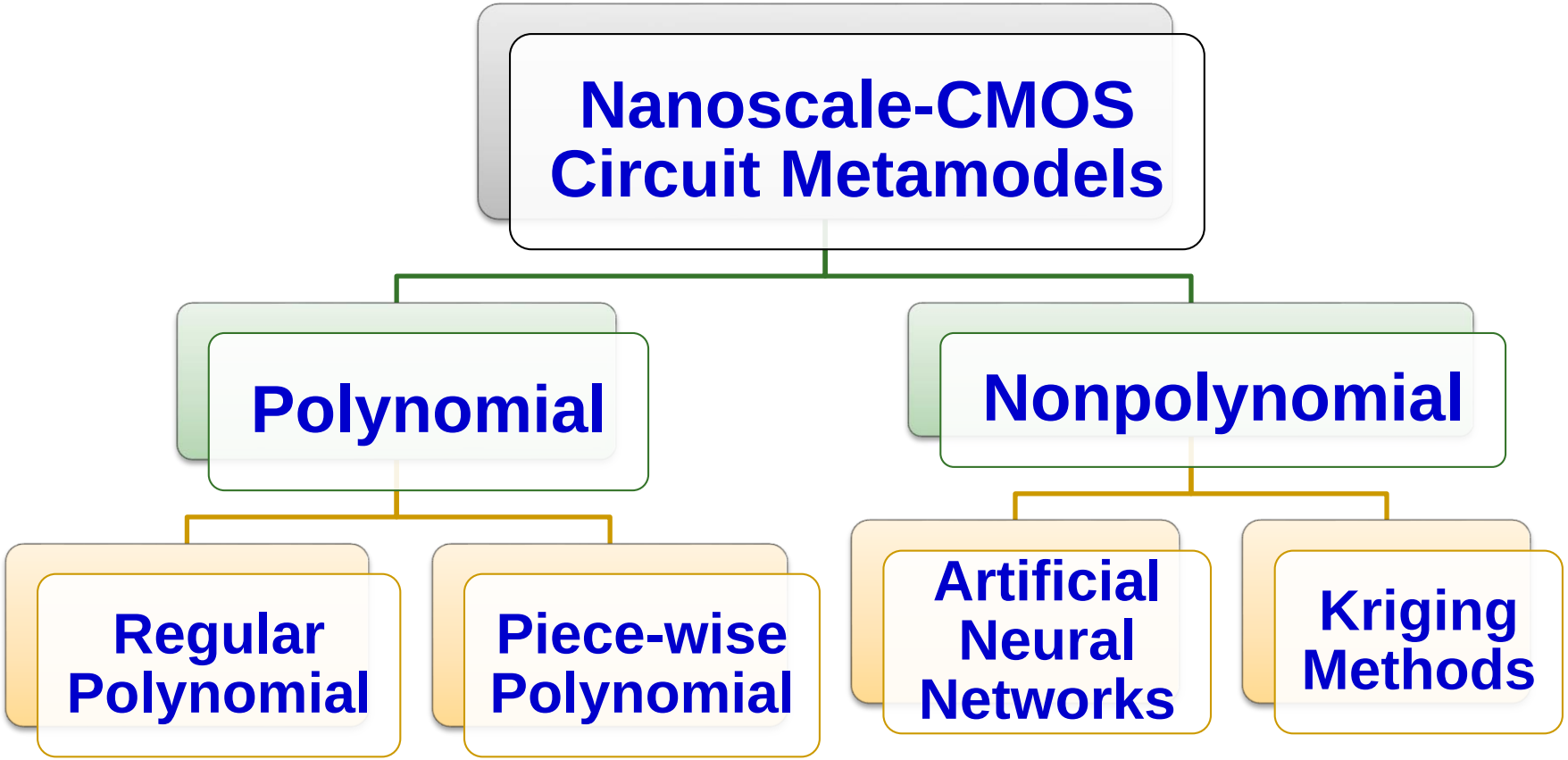
Proposed Flow: Key Perspective

- Novel design and optimization methodology that will produce robust AMS-SoC components using **ultra-fast automatic iterations over metamodels** (instead of netlist) and two manual layout steps.
- The methodology easily accommodates multidimensional challenges, reduces design cycle time, improves circuit yield, and reduces chip cost.

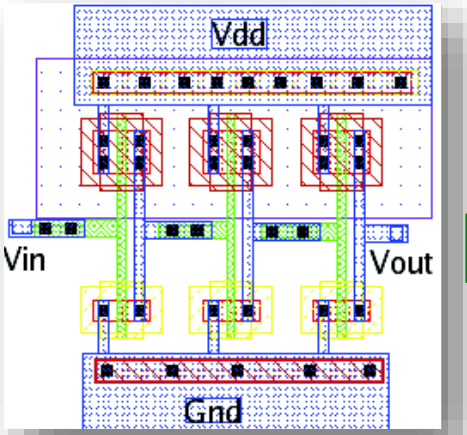
Metamodel-Based Design Flow



Metamodels : Selected Types

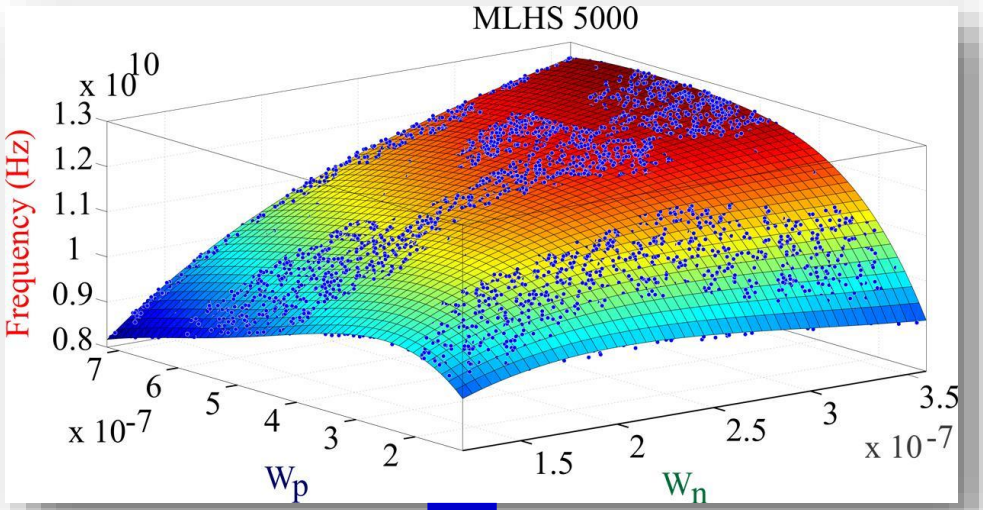


Metamodels : Polynomial Example



Actual Circuit (SPICE netlist) of AMS-SoC Components

Statistical Sampling

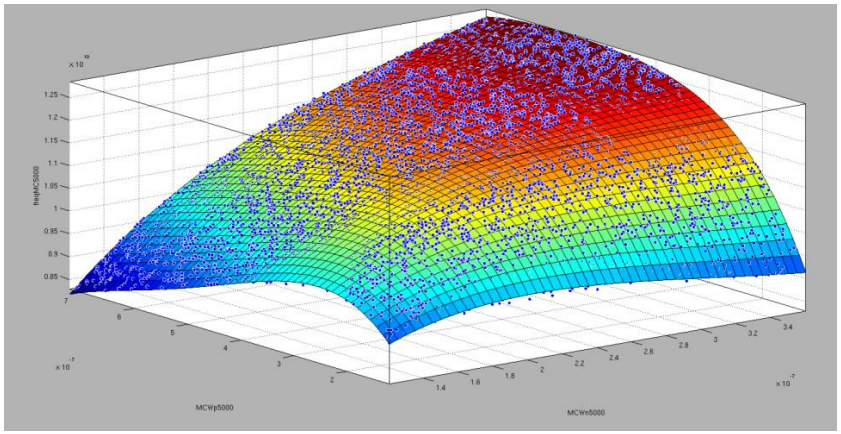


Polynomial Function Fitting

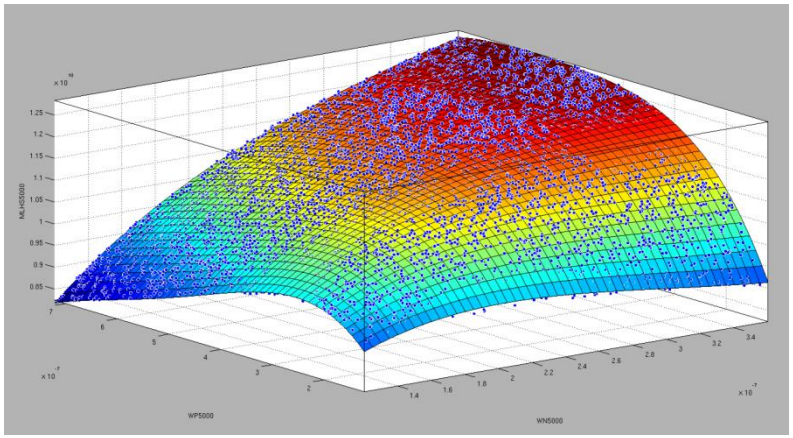
$$f(W_n, W_p) = 7.94 \times 10^9 + 1.1 \times 10^{16} W_n + 1.28 \times 10^{15} W_p.$$

Sampling Techniques: 45nm Ring Oscillator Circuit (5000 points)

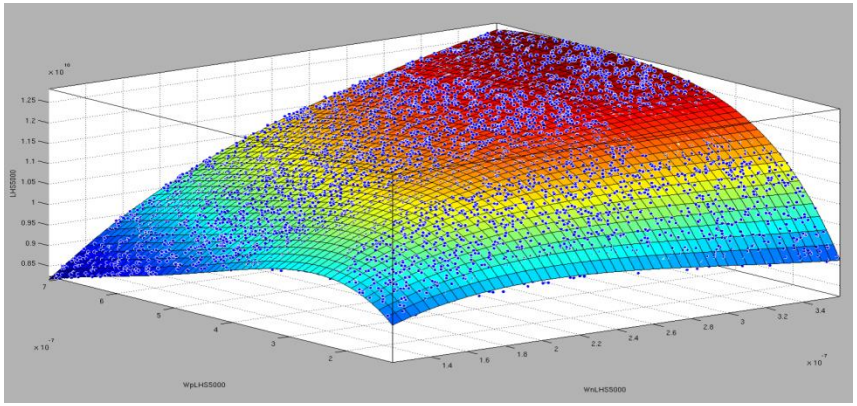
Monte Carlo



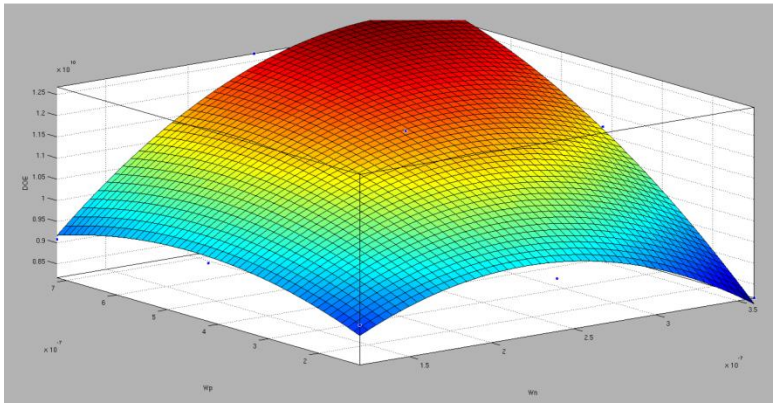
MLHS



LHS



DOE



Polynomial Metamodels

- The generated sample data can be fitted in many ways to generate a metamodel.
- The choice of fitting algorithm can affect the accuracy of the metamodel.
- A simple metamodel has the following form:

$$y = \sum_{i,j=0}^{k} \left(\alpha_{ij} \times x_1^i \times x_2^j \right)$$

- y is the response being modeled (e.g. frequency), $x = [W_n, W_p]$ is the vector of variables and α_{ij} are the coefficients.

Metamodel: Polynomial Comparison

Case Study Circuits	Polynomial Order	μ error (in MHz)	σ error (in MHz)
Ring Oscillator **45nm CMOS** **Target *f* : 10GHz**	1	571.0	286.7
	2	195.4	78.1
	3	37.2	18.0
	4	20.0	10.7
	5	17.1	9.6
LC-VCO **180nm CMOS** **Target *f* : 2.7GHz**	1	42.3	40.1
	2	39.4	37.8
	3	35.4	33.9
	4	30.5	29.3
	5	26.5	25.2

Ring oscillator – Order 1

$$f(W_n, W_p) = 7.94 \times 10^9 + 1.1 \times 10^{16} W_n + 1.28 \times 10^{15} W_p.$$

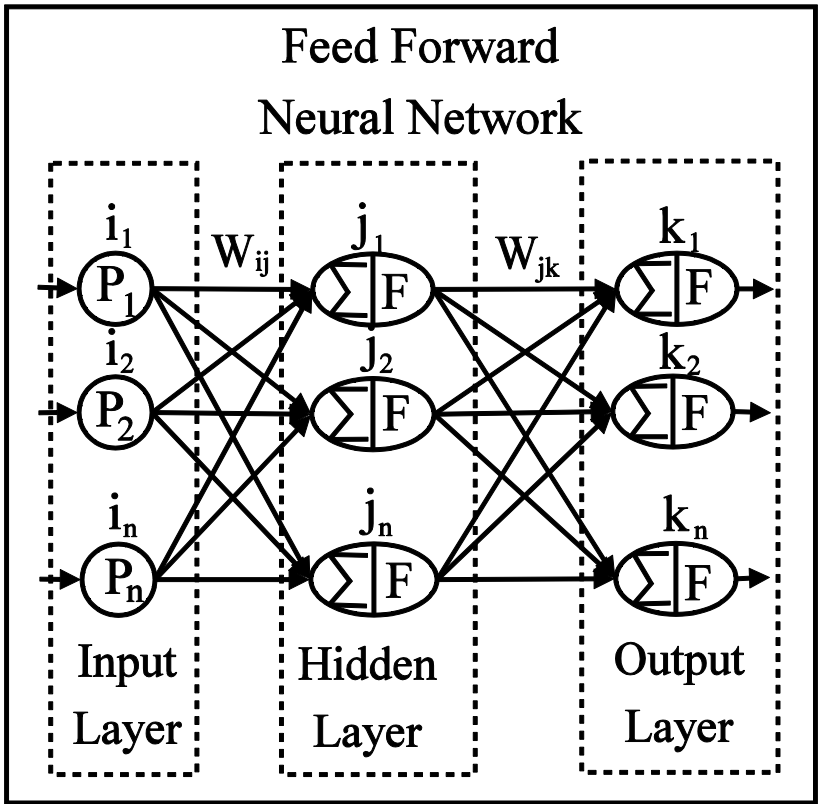
LC-VCO – Order 1

$$f(W_n, W_p) = 2.38 \times 10^9 - 3.49 \times 10^{12} W_n - 6.66 \times 10^{12} W_p.$$

Artificial Neural Network (ANN) Metamodeling

- Feed-forward dual layer (FFDL) ANNs are considered.
- FFDL ANN created for each FoM:
  - Nonlinear hidden layer functions are considered each varying hidden neurons 1-20:

$$b_j(v_j) = \tanh(\lambda v_j)$$



Metamodel Comparison: Polynomial Vs Nonpolynomial

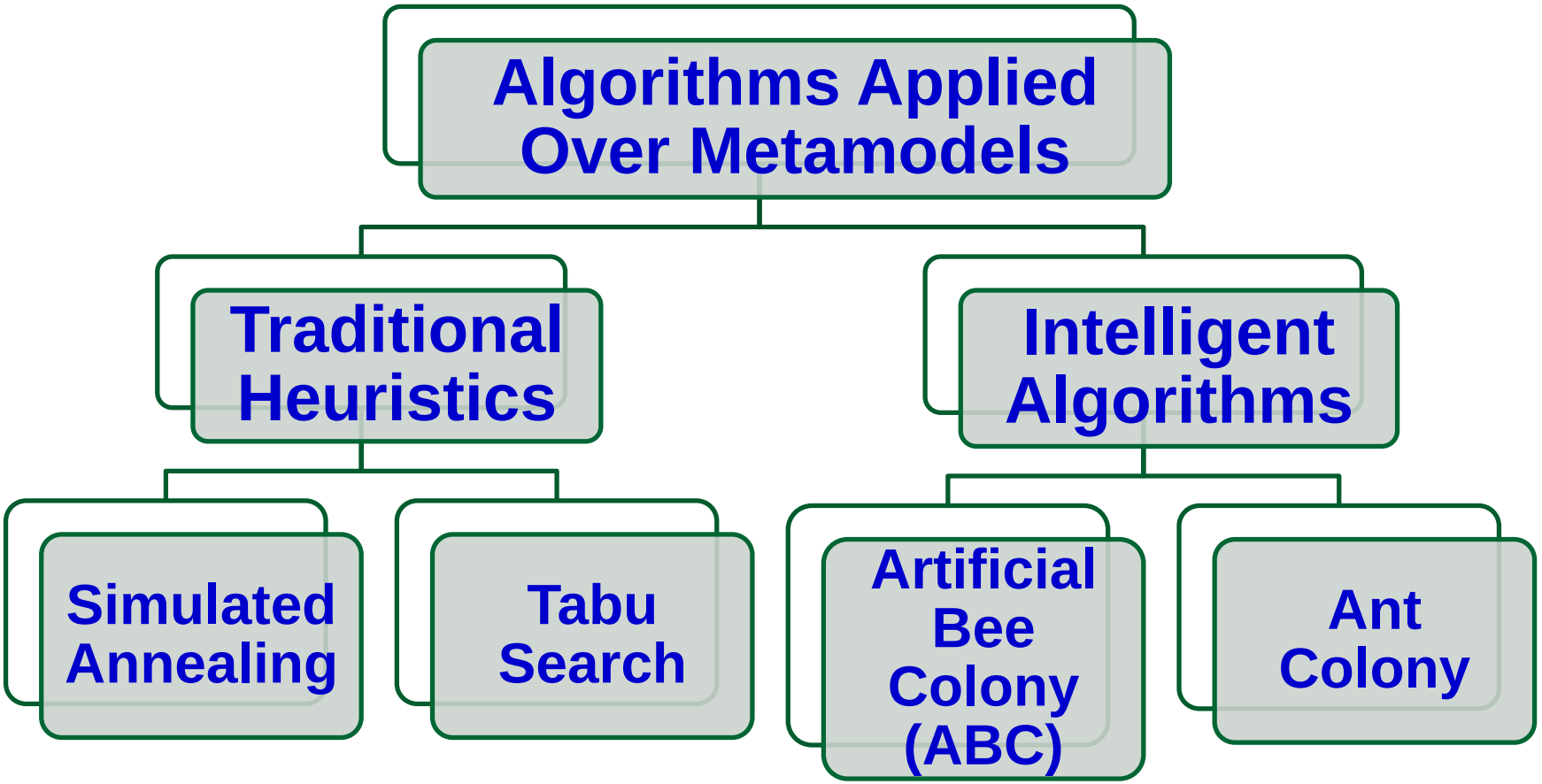
- Nonpolynomial (Artificial Neural Network) is more suitable large circuits.

180nm CMOS PLL with Target Specs: f = 2.7GHz, P = 3.9mW, 8.5μs.

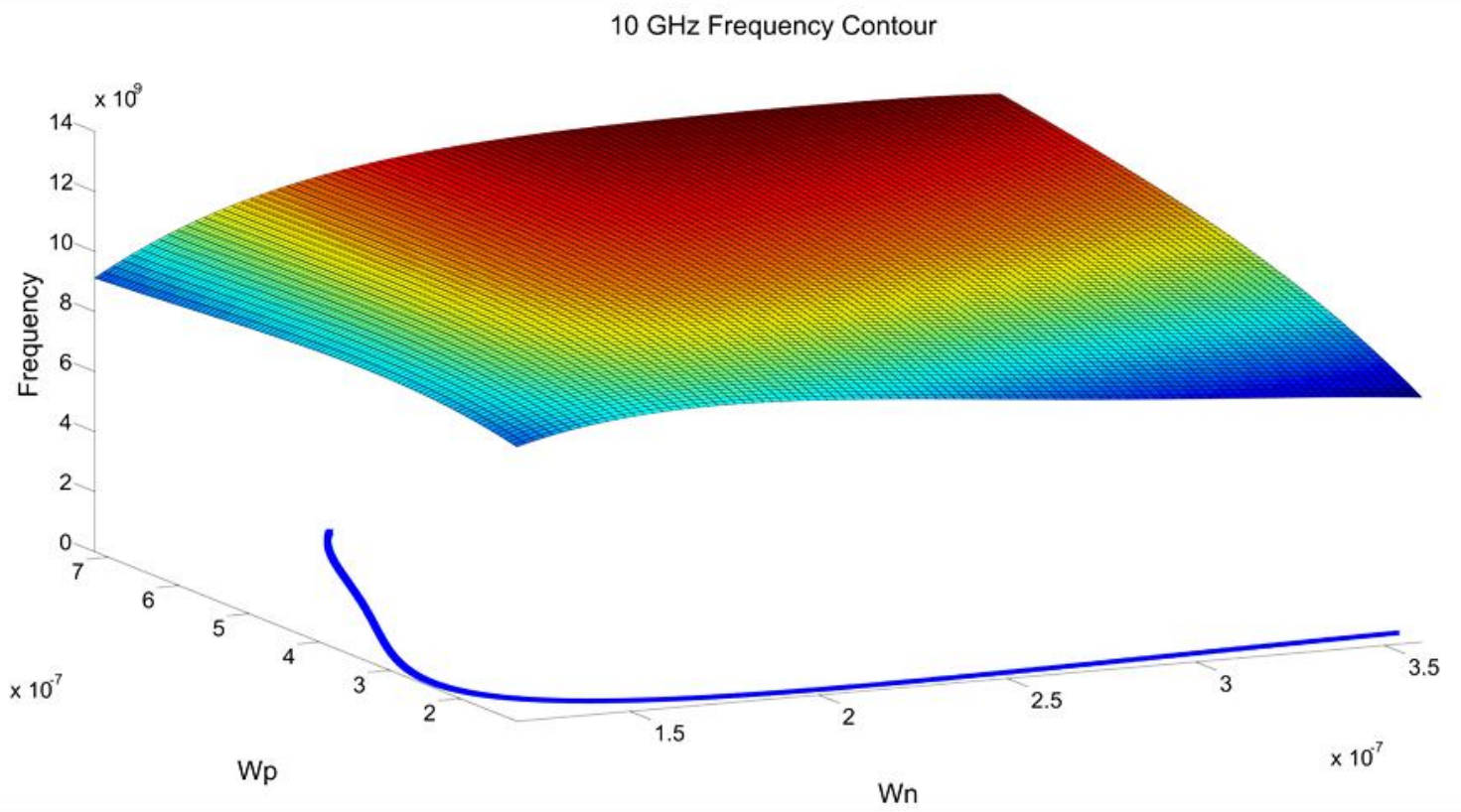
Figures-of-Merits (FoM)	Polynomial # of Coefficients	RMSE	Nonpolynomial (Neural Network)
Frequency	48	77.96 MHz	48MHz
Power	50	2.6mW	0.29mW
Locking Time	56	1.9μs	1.2μs

- 56% increase in accuracy over polynomial metamodels.
- On average 3.2% error over golden design surface.

Selected Algorithms for Optimization over Metamodels

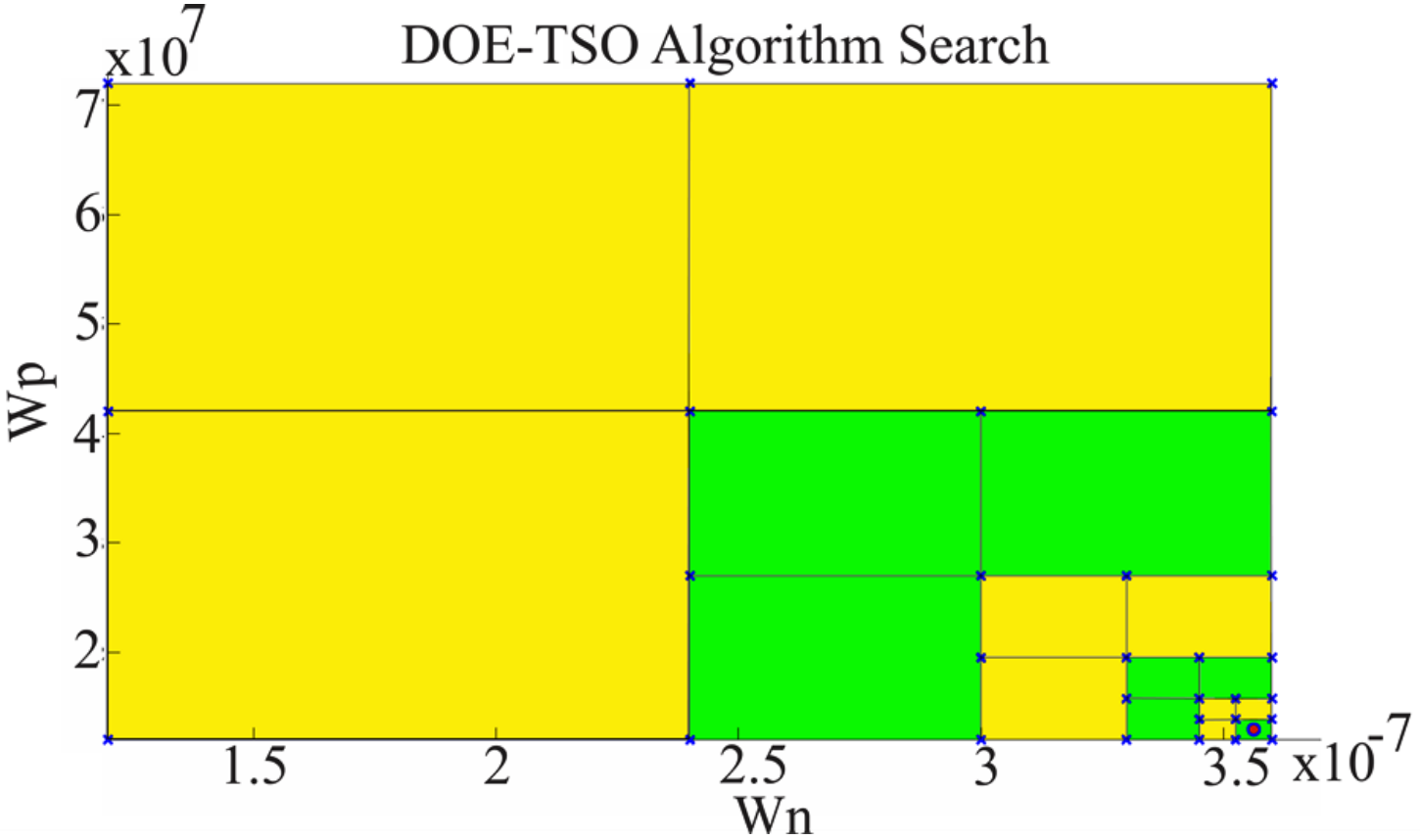


Exhaustive Search : 45nm RO



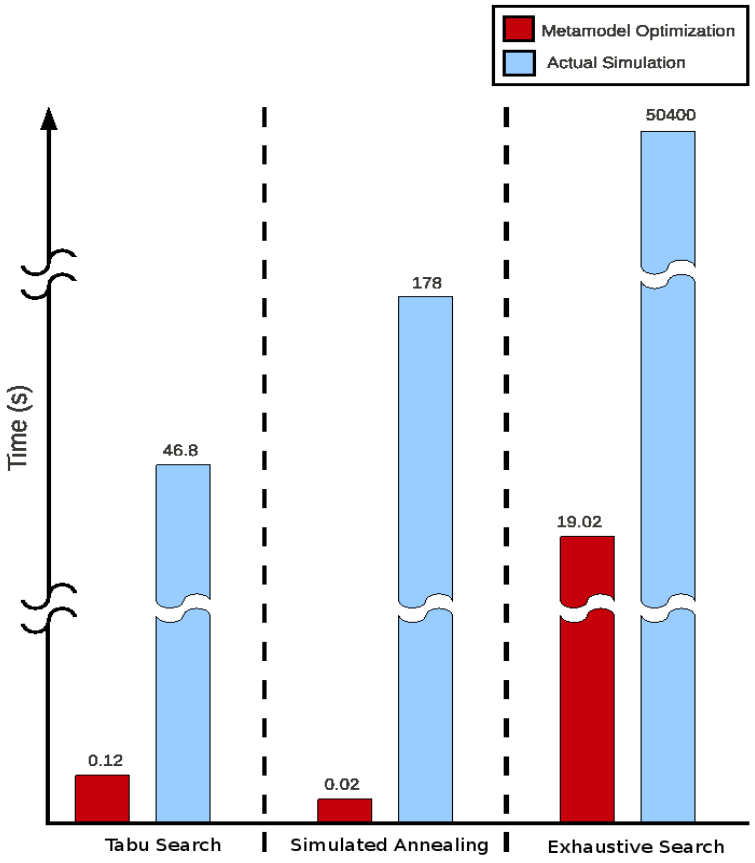
- Searches over two parameter space.
- Parameters incremented over specified steps.

DOE Assisted Tabu Search: 45nm RO



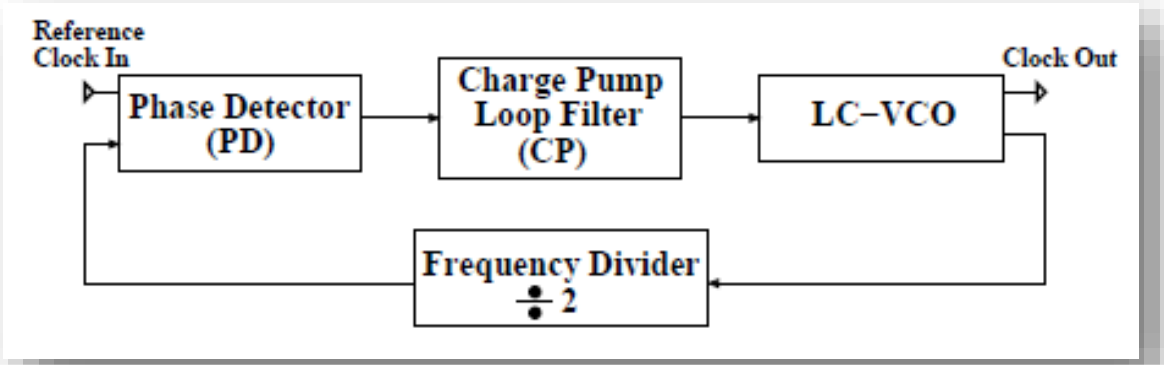
- Search space is recursively divided into rectangles and each time the rectangle with superior result is selected.

Comparison of the Running Time of Heuristic Algorithms: 45nm RO



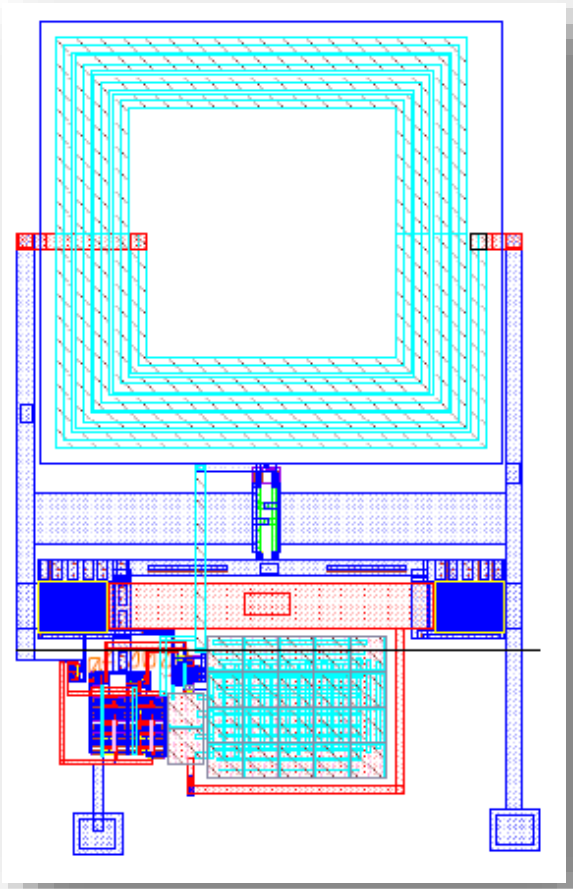
- **Optimization without metamodels:** the tabu search optimization is faster by ~1000× than the exhaustive search and ~4× faster than the simulated annealing optimization.
- **Optimization with metamodels:** the simulated annealing optimization is faster by ~1000× than the exhaustive search and ~6× faster than the tabu search optimization.

Case Study Circuit: 180nm PLL



Block diagram of a PLL.

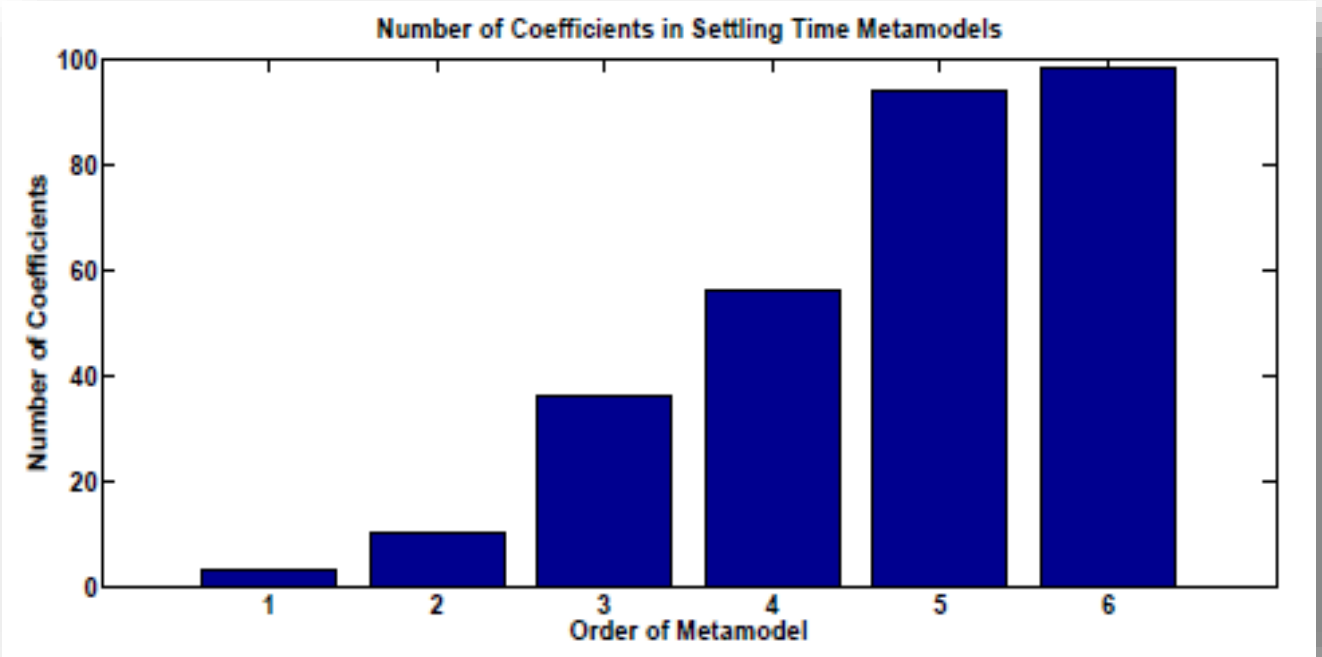
- PLL circuit is characterized for frequency, power, vertical and horizontal jitter (for simple phase noise), and locking time.
- Metamodels are created for each FoM from same sample set.



PLL for 180nm.

PLL: Polynomial Metamodels …

- The number of coefficients corresponding to the order of the generated metamodel for settling time.
- This means that the model is over fitted, therefore for the metamodel that represents settling time, a polynomial order of 4 will be used.



Artificial Bee-Colony : Overview

1. **Initial** food sources are produced for all worker bees.
2. **Do**
   1) Each worker bee goes to a food source and evaluates its nectar amount.
   2) Each onlooker bee watches the dance of worker bees and chooses one of their sources depending on the dances and evaluates its nectar amount.
   3) Determine abandoned food sources and replace with the new food sources discovered by scout bees.
   4) Best food source determined so far is recorded.
3. **While** (requirements are met)

A food source → a solution; A position of a food source → a design variable set; Nectar amount → Quality of a solution; Number of worker bees → number of quality solutions.

PLL: ABC over Poly. Metamodels

PLL parameters with constraints and optimized values.

Circuit	Parameter	Min (m)	Max (m)	Optimal Value (m)
Phase Detector	W_{ppd1}	400n	2μ	1.66μ
	W_{npd1}	400n	2μ	1.11μ
	W_{ppd2}	400n	2μ	784n
	W_{npd2}	400n	2μ	689n
	W_{ppd3}	400n	2μ	1.54μ
	W_{npd3}	400n	2μ	737n
Charge Pump	W_{nCP1}	400n	2μ	1.24μ
	W_{pCP1}	400n	2μ	1.35μ
	W_{nCP2}	1μ	4μ	1.35μ
	W_{pCP2}	1μ	4μ	2.88μ
LC-VCO	W_{nLC}	3μ	20μ	18.62μ
	W_{pLC}	6μ	40μ	37.48μ
Divider	W_{p1Div}	400n	2μ	1.65μ
	W_{p2Div}	400n	2μ	1.54μ
	W_{p3Div}	400n	2μ	1.38μ
	W_{p4Div}	400n	2μ	1.96μ
	W_{n1Div}	400n	2μ	1.09μ
	W_{n2Div}	400n	2μ	1.17μ
	W_{n3Div}	400n	2μ	1.29μ
	W_{n4Div}	400n	2μ	1.95μ
	W_{n5Div}	400n	2μ	536n

- An exhaustive search of the design space of 21 parameters with 10 intervals per parameter requires 10^{21} simulations.
- 10^{21} SPICE simulations is slow; 10min per one.
- 10^{21} simulations using polynomial metamodels is fast.
- Time savings: $\approx 10^{20}\times$ SPICE simulation time.

PLL: ABC Optimization: Poly Vs ANN

Optimization Results

FoM	Poly. Metamodel	ANN Metamodel
Average Power	3.9 mW	3.9 mW
Frequency	2.6909 GHz	2.7026 GHz

Optimization Time Comparison

Algorithm	Circuit Netlist	Poly. Metamodel	ANN Metamodel
ABC (100 iterations)	#bees(20) * 5 min * 100 iteration = 10,000 minutes = **7 days (worst case)**	5 mins	0.12 mins
Metamodel Generation	0	11 hours for LHS + 1 min creation	11 hours for LHS + 10mins training and verification.

Conclusions

- Nanoelectronic circuits and systems have multifold design challenges.
- DFX is design for X – Power, Variability, Cost …
- DFP:
  - 35% of total energy in USA is consumed by electronics.
  - Battery is an critical constraint for portable systems.
  - Energy efficient hardware, software at the same time better battery design needed for effective solutions.
- DFV: Reduce the variability in chip and enhance yield.
- DFC: Reduce NRE, yield, and time to market.
- Much more research is needed for combined consideration of issues, e.g. X ← Variability and Cost

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- **S. P. Mohanty** and E. Kougianos, "Incorporating Manufacturing Process Variation Awareness in Fast Design Optimization of Nanoscale CMOS VCOs", *IEEE Transactions on Semiconductor Manufacturing*, Volume 27, Issue 1, February 2014, pp. 22--31, DOI: http://libproxy.library.unt.edu:2083/10.1109/TSM.2013.2291112.
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- O. Garitselov, **S. P. Mohanty**, and E. Kougianos, "A Comparative Study of Metamodels for Fast and Accurate Simulation of Nano-CMOS Circuits", *IEEE Trans. on Semiconductor Manufacturing*, Vol. 25, No. 1, Feb 2012, pp. 26--36.
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