Fast Statistical Process Variation Analysis using Universal Kriging Metamodeling: A PLL Example

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Abstract

The design of Analog Mixed-Signal Systems-on-Chip (AMS-SoCs) presents difficult challenges given the number of design specifications that must be met. This situation is more aggravating in the presence of process variation effects for nanoscale technologies. Existing statistical techniques rely heavily on Monte-Carlo analysis for design parameters in an effort to mitigate the effects of process variation. Such methods, while accurate are often expensive and require extensive amount of simulations. In this paper we present a geostatistical based metamodeling technique that can accurately take into account process variation and considerably reduces the amount of time for simulation. An illustration of the proposed technique is shown using a 180nm PLL design. The proposed technique achieves an accuracy of 0.7 % and 0.33% for power consumption and locking time, respectively, and improves the run time by about 10 x.

Introduction

- Analog mixed-signal systems design and optimization are highly complex due to increasing integration.
- As technology scales impact of process variation becomes more pronounced.
- Process variation effects are conventionally explored using Monte-Carlo analysis simulations and other statistical method such as hierarchical statistical, symbolic and regression based techniques.
- Computer simulations are largely deterministic and average out the error due to correlation effects.
- Kriging techniques take into account the correlation effects between design parameters and can thus better capture the effects of process variation.
- Metamodels created with kriging techniques can be effectively used for statistical yield analysis.

Geostatistical Modeling

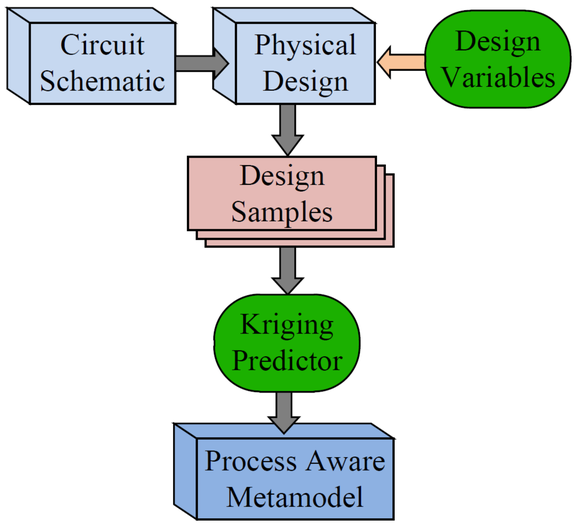
- Kriging techniques were originally used for geostatistical and have now been extended to other fields.
- A combination of polynomial methods and with stochastic approach to mitigate deterministic nature of computer simulations.
- The basis expression has a form:

$$\widehat{Z}(\mathbf{wn_0}) = \sum_{j=1}^{L} \lambda_j B_j(\mathbf{wn}) + z(\mathbf{wn}),$$

where λ is a set of unique weights for each predicted point .

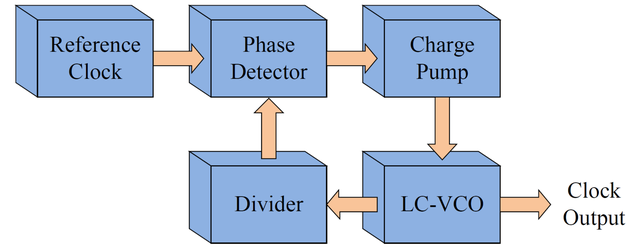
Process Variation Aware Metamodel

The proposed technique creates an efficient metamodel for statistical analysis of process variation.
The figure below summarizes the metamodel creation process.



Case Study Circuit: PLL

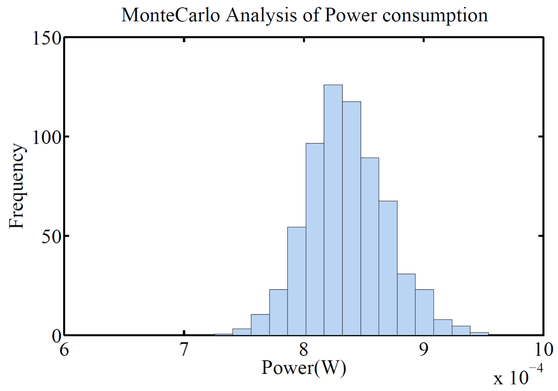
- The proposed technique is illustrated on a phased locked loop (PLL) shown as a system level in the figure to the right.
- Design objective was to minimize power dissipation using locking time as a constraint.
- The physical design of the PLL was implemented using 180nm technology.
- The parasitic netlist is extracted and parameterized for 21 design variables.

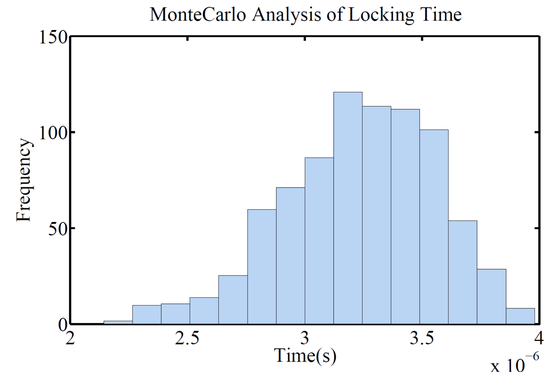


Experimental Results and Comparison

Statistical Analysis for Accuracy of Kriging Generated Metamodel for PLL

	Mean (μ)			Standard Deviation (σ)		
	Circuit	Kriging	Error	Circuit	Kriging	Error
P_{PLL}	0.877 mW	0.871 mW	0.7 %	0.073 mW	0.072 mW	1.4 %
$Lock_{PLL}$	3.24 μs	3.23 μs	0.31 %	1.07 μs	0.33 μs	69.16 %





Comparison with Related Metamodel Designs

Research	Technique	Power		Locking Time	
		Mean	Error	Mean	Error
[3]	Quasi-SA	-	-	3.45	2.2 %
[18]	ANN	0.90 mW	0.14 %	3.22 μs	0.7 %
[This Paper]	Kriging	0.87 mW	0.7 %	3.23 μs	0.33 %

Conclusion

- Kriging based statistical model for process variation analysis for PLL is presented.
- Process variation aware metamodel achieves 0.7 % and 0.33 % mean error in power dissipation and locking time respectively.
- Achieves a simulation speed up of 10x.