Double Gate FinFET based Mixed-Signal Design: A VCO Case Study

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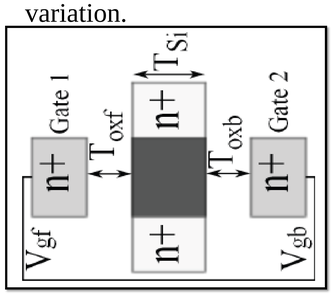
Abstract

• *We investigate mixed-signal design for double-gate (DG) FinFET technology using a current-starved voltage controlled oscillator (VCO) as a case study.*
• *Design issues of the DG FinFET-based VCO are presented in a comparative perspective with classical CMOS VCO.*
• *DG FinFET VCO is analyzed for the figures-of-merit like center frequency, frequency-voltage (f-v) characteristics.*
•*Statistical process variation analysis is presented to study the variability in DG FinFET VCO.*
•*Surface Models are investigated for the f-v characteristics and width quantization-aware modeling has been presented for the FinFET based VCO. The models can be used for fast design optimization..*

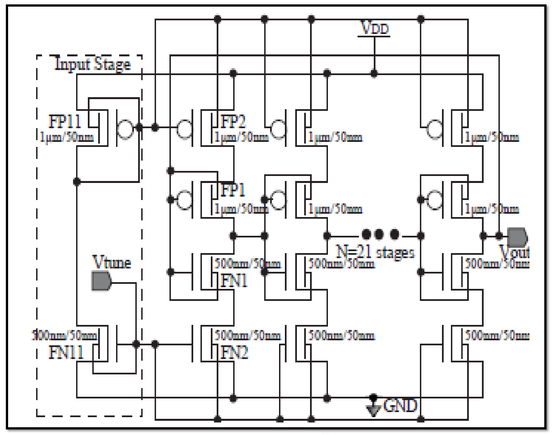
Introduction

The major advantages of FinFET over CMOS include the following:
(1) Nearly ideal sub-threshold slope.
(2) Small intrinsic gate capacitance.
(3) Smaller junction capacitances.
(4) Better immunity to SCEs.
(5) Higher *ION/ IOFF* ratio.
(6)Design flexibility at circuit level with shorted gate (SG) and independent gate (IG) options.
(7)Higher immunity to SCEs.
(8)Higher immunity to process variation.



DG FinFET VCO

45nm shorted double gate FinFET VCO



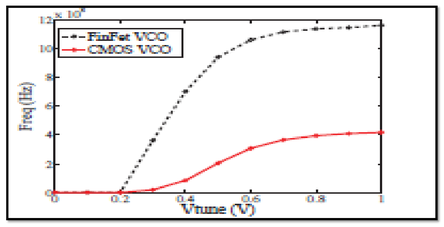
$$Freq_{VCO} = \frac{I_D}{(n \times C_t \times V_{DD})}$$

F-V Characteristics of VCO

Best Fit Equations and Curve

$$freq_{FinFET}(V_{tune}) = p_0 + p_1 V_{tune} + p_2 V^2_{tune} + p_3 V^3_{tune}$$

p_0	1.1 x 10^9
p^1	1.426 x 10^8
p^2	-1.646 x 10^8
p^3	6.802 x 10^7



$$freq_{CMOS}(V_{tune}) = a_0 e^{-\left(\frac{V_{tune}-b0}{c_0}\right)^2} + a_1 e^{-\left(\frac{V_{tune}-b1}{c_1}\right)^2}$$

a_0	4.126 x 10^8
b_0	1.368
c_0	1.351
a_1	2.059 x 10^8
b_1	-0.1438
c_1	0.8269

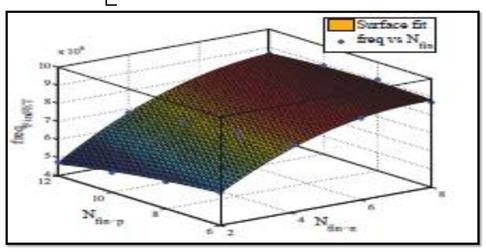
$$RMSE = \sqrt{\frac{1}{N}\sum_{i=0}^{N}\left(freq(V^i_{tune}) - \overline{(freq(V^i_{tune}))}\right)^2}$$

$$R^2 = 1 - \frac{\sum_{i=0}^{N}\left(freq(V^i_{tune}) - \overline{freq(V^i_{tune})}\right)^2}{\sum_{i=0}^{N}\left(freq(V^i_{tune}) - \overline{freq(V^i_{tune})}\right)^2}$$

Width-Aware Quantization Modeling

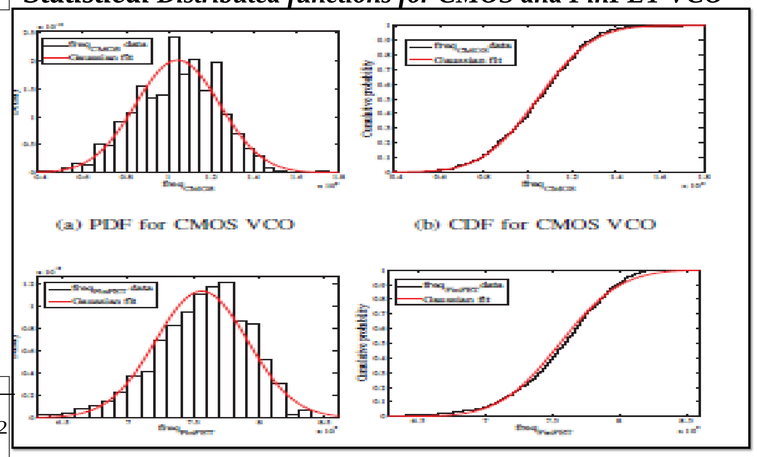
$$freqFinFET = 2H_{fin}\sum_{i,j=0}^{2} p_{ij} N^i_{fin-n} N^j_{fin-p}$$

$$p_{ij}(freq_{FinFET}) = \begin{bmatrix} 7.9\times10^8 & -2.5\times10^7 & -8.9\times10^6 \\ 1.3\times10^8 & 1.4\times10^7 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$



Statistical Process-Variation Analysis

Statistical Distributed functions for CMOS and FinFET VCO



Process Variation Data for CMOS and DG FinFET VCO

Measurement	μ	σ	C_v =(μ/σ)
$freq_{CMOS}$	104.37 MHz	19.812 MHz	0.1898
$freq_{FinFET}$	751.14 MHz	35.272 MHz	0.0466

Chi-square test statistic $X^2 = \sum_{i=1}^{N}\frac{(O(freq)_i - E(freq)_i)^2}{E(freq)_i}$

Conclusion and Future Work

• A comparison is drawn between classical CMOS and DG FinFET based VCO.
• The DG FinFET VCO has a 7× *higher center* frequency due to smaller intrinsic gate capacitance.
• FinFET VCO shows 4.66% variability due to V_{Th} fluctuations, as compared to 18.98% variability in the CMOS VCO.
• As part of future research, thermal effects will be examined, as FinFETs suffer from self-heating.
• Width quantization-aware models for power consumption will be developed, and a discrete multiobjective optimization will be performed using FinFET based mixed signal circuits.