Geostatistics Inspired Fast Layout Optimization of Nanoscale CMOS Phase Locked Loop

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Outline of the talk



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Background and Motivation

- Computer simulations are expensive
- Pronounced effects of process variations in deep nanometer regions
 - Increase in number of design parameters
 - Current modeling techniques not effective at capturing effects of process variation
- Complex and high density designs
- Designs for low power consumption







Novel Contributions

- Exploring Kriging for high dimensional metamodeling
- Design flow methodology
 - Kriging metamodeling and gravitational search algorithm optimization.







Prior Related Research

- Exploration of optimization algorithms for NanoCMOS designs
- Kriging Based Techniques
 - O. Okobiah --- simple and ordinary kriging metamodels
 - G.Yu --- re-iterative Pareto fronts
 - H. You --- kriging metamodeling







Fundamentals of Kriging

 Originally used in geostatistics for mining purposes.

$$y(\mathbf{x}_0) = \sum_{i=1}^{N} \lambda_j B_j(\mathbf{x}) + z(\mathbf{x}), \tag{1}$$

Each point is predicted based on a set of unique weights (λ_j) .

$$\sum_{j=1}^{n} \lambda_j = 1. \tag{3}$$







Fundametals of Kriging...

$$\begin{pmatrix} \lambda_1 \\ \vdots \\ \lambda_n \\ \mu \end{pmatrix} = \Gamma^{-1} \begin{pmatrix} \gamma(x_1, x_0) \\ \vdots \\ \gamma(x_n, x_0) \\ 1 \end{pmatrix}, \qquad (3)$$

$$\Gamma = \begin{pmatrix} \gamma(x_1, x_1) & \cdots & \gamma(x_1, x_n) & 1 \\ \vdots & \ddots & \vdots & 1 \\ \gamma(x_n, x_1) & \cdots & \gamma(x_n, x_n) & 1 \\ 1 & 1 & 1 & 0 \end{pmatrix}, \quad (4)$$

$$\widehat{P_{PLL}}(\mathbf{Wn_0}) = \sum_{j=1}^{L} \lambda_j B_j(\mathbf{wn}) + z(\mathbf{wn}), \quad (7)$$







Gravitational Search Algorithm

- Part of swarm Intelligence family
 - population based heuristic algorithms
- Based on gravitational laws of attraction and motion

$$F_{ij}^{d}(t) = G(t) \frac{M_{pi}(t) \times M_{aj}(t)}{R_{ij}(t) + \epsilon} (x_{j}^{d}(t) - x_{i}^{d}(t)),$$

where F^d_{ij}(t) is design objective, M is the quality of solution at search location i or j, x_i is the set of design parameters at location i







Gravitational Search Algorithm



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Gravitational Search Algorithm









Case Study Circuit: 180nm PLL



Fig. 3. System level diagram of the PLL



Fig. 4. 180nm layout of the PLL







Proposed **Design Flow**



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Design Flow Components

- Design and netlist optimization
 - Baseline design
 - Ischematic and layout)
 - Extract parasitic netlist



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Design Flow Components

- Sampling and Metamodel Generation
 - Parameterize parasitic netlist
 - Identify performance objectives
 - LHS sampling
 - L, W as sampling corners
 - process variation
 - Metamodel for each design objective is generated
 - using mGstat (MATLAB Kriging tool)
 - Design objectives are functions of design parameters

• **e.g.**
$$\widehat{P_{PLL}}(\mathbf{Wn_0}) = \sum_{j=1}^{L} \lambda_j B_j(\mathbf{wn}) + z(\mathbf{wn}),$$
 (7)







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Design Flow Components

- Design Optimization
 - Kriging metamodels optimized with GSA algorithm
 - Conflicting design objectives used as goal and constraint

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Final physical design is drawn



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Experimental Results

TABLE IIIOptimized Parameter Variables

PLL Components	Parameter	Min (m)	Max (m)	Optimal (m)		
Phase Detector	W_{pPD1}	400n	2μ	1.53μ	IVI	etric
	W_{pPD1}	400n	2μ	0.95μ	R	MSE
	W_{pPD1}	400n	2μ	1.00μ		2
	W_{nPD1}	400n 400n	$\frac{2\mu}{2\mu}$	1.16μ	K	2
	$\frac{W_n P D 1}{W_n P D 1}$	400n	$\frac{2\mu}{2\mu}$	1.58μ	-	
	$W_m C D1$	400n	2.11	1.12µ		
	W_{nCP1}	400n	$\frac{2\mu}{2\mu}$	1.32μ	-	
Charge Pump	W_{nCP2}	2μ	4μ	2.07μ	_	
	W_{pCP2}	4μ	4μ	4.72μ		
	W_{nLC}	3μ	20μ	12.22μ		
10-700	W_{pLC}	6μ	40μ	14.83μ		
	W_{pDIV1}	400n	2μ	1.06μ		
	W_{pDIV2}	400n	2μ	1.11μ		
Divider	W_{pDIV3}	400n	2μ	0.75μ	-	
	W_{pDIV4}	400n 400 n	$\frac{2\mu}{2\mu}$	1.78μ	-	
	$\frac{W_{nDIV1}}{W_{DIV1}}$	400n 400n	$\frac{2\mu}{2\mu}$	1.55μ		
	$\frac{W_{nDIV1}}{W_{nDIV1}}$	400n	$\frac{2\mu}{2\mu}$	1.65μ		
	W_{nDIV1}	400n	$\frac{2\mu}{2\mu}$	1.96µ	-	
	W_{nDIV1}	400n	2μ	0.43µ	-	
Metric		Power ((mW)	Locking Ti	me (ns)	Area (µm²
Baseline Design		8.27		2.74		525 x 326
Optimal Design Reduction		1.67 79 %		2.63 4 %		525 x 326
						0 %

Metric	Value
RMSE	6.46 x 10 ⁻¹⁰
R ²	0.9959









Fig. 5. Optimization Steps of the PLL

Metric	Power (mW)	Locking Time (ns)	Area (µm²)
Baseline Design	8.27	2.74	525 x 326
Optimal Design	1.67	2.63	525 x 326
Reduction	79 %	4 %	0 %







Related Comparison

Research	Test Circuits	Metamodeling Technique	Accuracy	Optimization Technique	
You	Integrated Op-Amp	Kriging	0.5658	-	
Yu	Ring Oscillator	Kriging	0.5325% (MSE)	-	
	LC-VCO		0.5563% (MSE)	-	
Okobiah	Sense Amplifier	Kriging	3.2 x10 ⁻⁹	ACO	
Garitselov	PLL	Polynomial	0.5658	ABC	
		ANN	0.5658		
This work	PLL	Kriging	6.46 x10 ⁻⁹	GSA	







Conclusions

A novel design flow methodology was presented
Incorporating Kriging metamodeling
Demonstrating GSA algorithm based optimization

Optimized PLL power by 79%







Thank you !!!