Energy Efficient Nanoelectronic System Design

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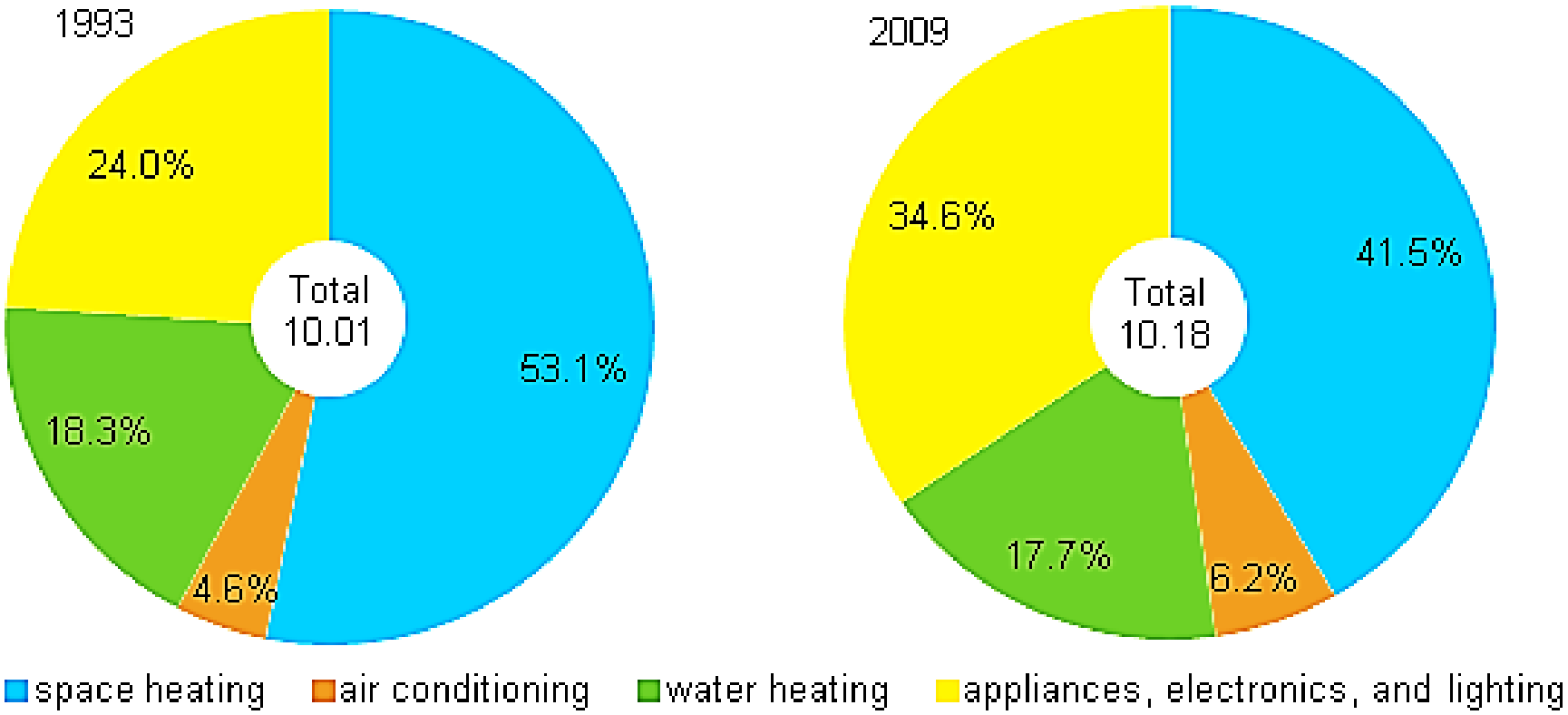
Outline of the Talk

- Example Consumer Electronic Systems
- Typical Electronic System Components
- The Power Issue: In a Nanoelectronic System
- Options for Energy Efficient System Design
- Conclusions and Future Research

Consumer Electronics Demand More and More Energy

Energy consumption in homes by end uses
quadrillion Btu and percent



Quadrillion BTU (or quad): 1 quad = 10^{15} BTU = 1.055 Exa Joule (EJ).

Source: U.S. Energy Information Administration.

Electronic System: Smart Phone

- Smarter … Faster … High Throughput …

→ Power Hungry !! Battery Hungry !!

Electronic System: Many Others (Same Story)

- Smarter … Faster … High Throughput …

→ Power Hungry !! Battery Hungry !!

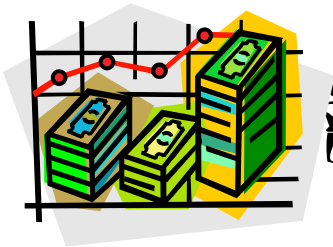
Battery Dependency: Not Overstated

One 787 Battery:
12 Cells / 32 V DC

- Boeing 787's across the globe were grounded.

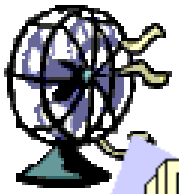
Source: http://www.newairplane.com

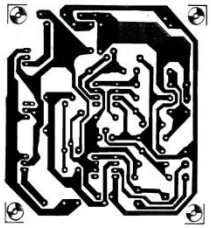
Why Energy Efficient Design ?

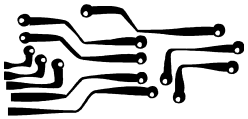


Packaging costs

Chip and system cooling costs



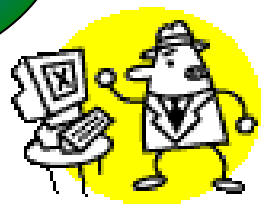




Power supply rail

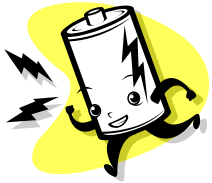
Power affects

Noise and reliability

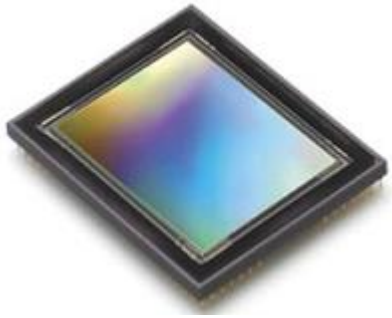


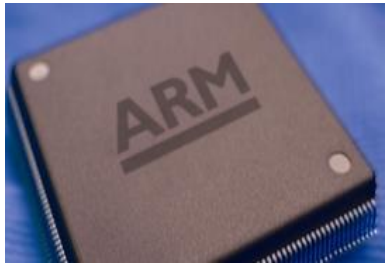
Environmental

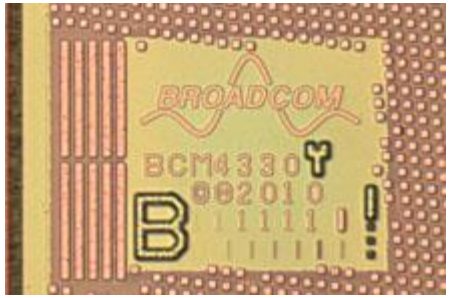
Battery life



A Typical Electronic System

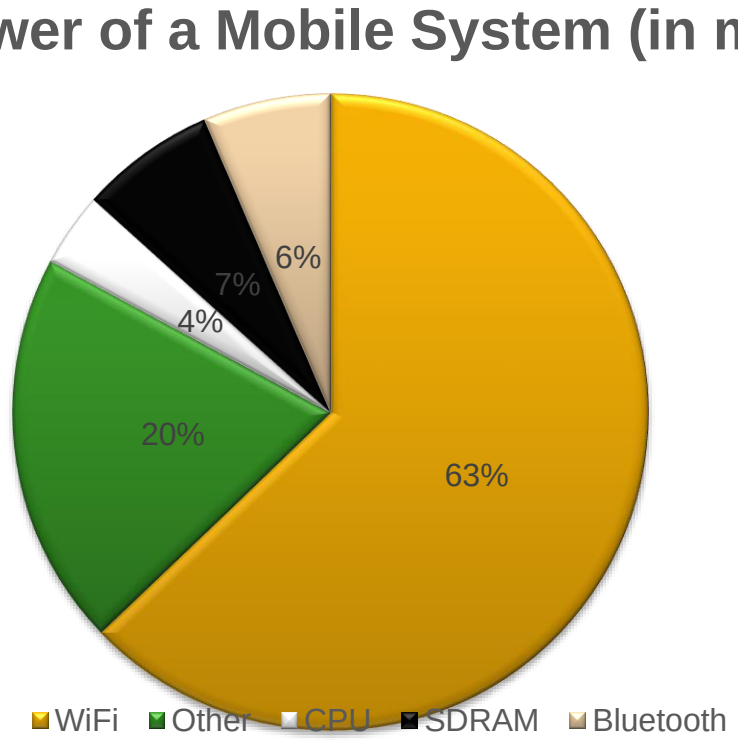






- Consists of several heterogeneous components.

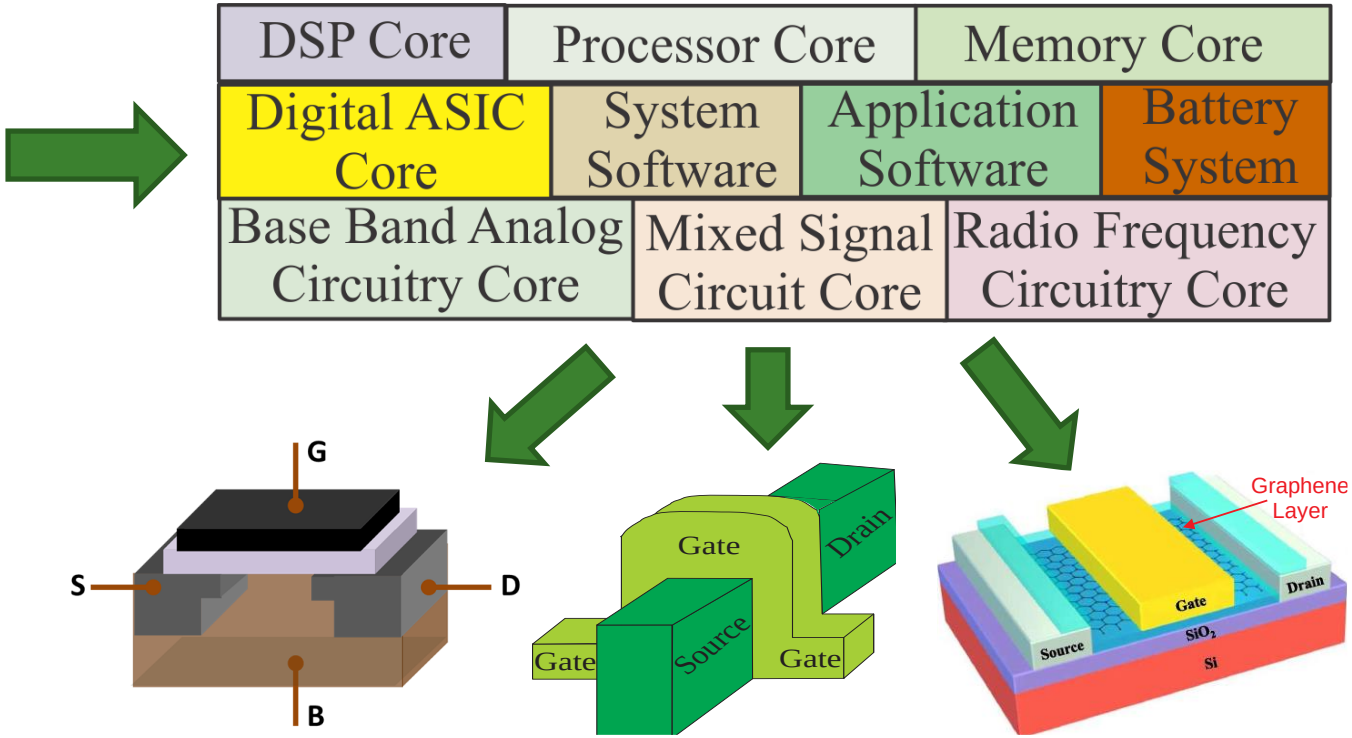
A Typical Electronic System: Where Energy Consumed??



Power dissipation breakdown in idle mode of a connected mobile device

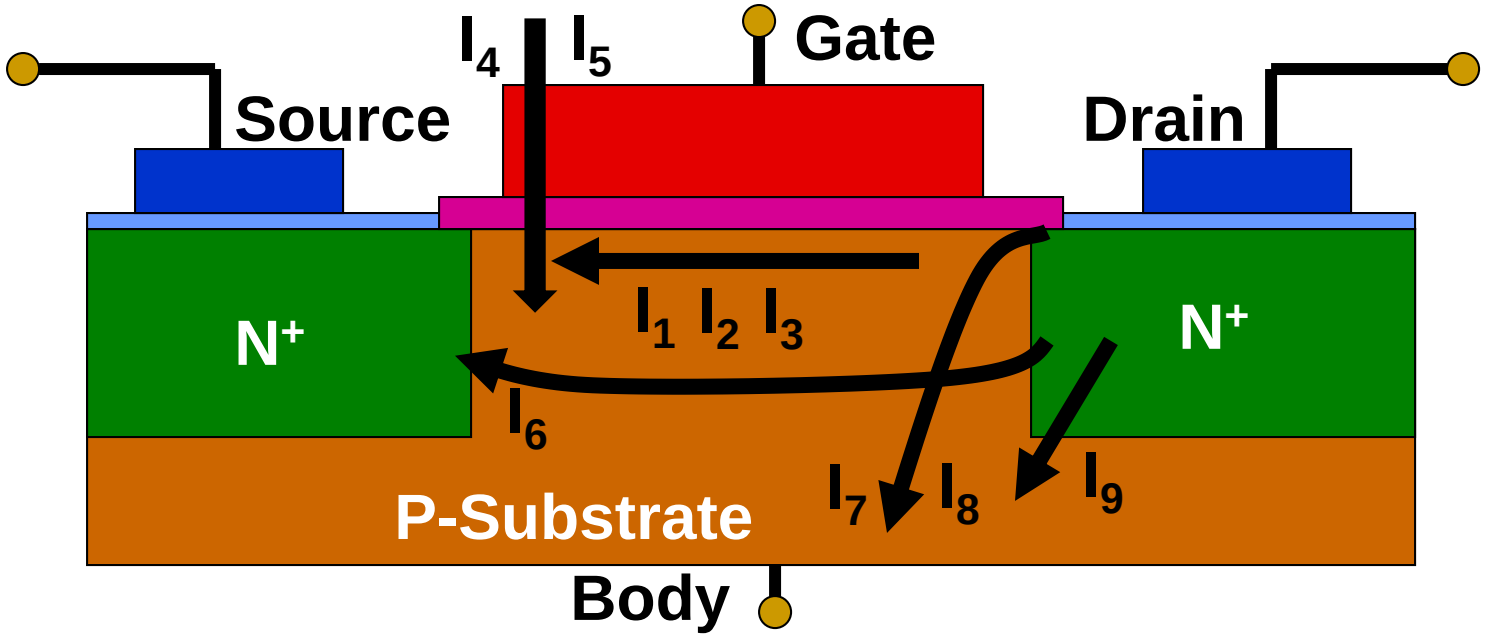
Source: Pering MobiSys 2006

A Typical Nanoelectronic System: (Many Diverse Components)



- Components have millions of nanoscale transistors.

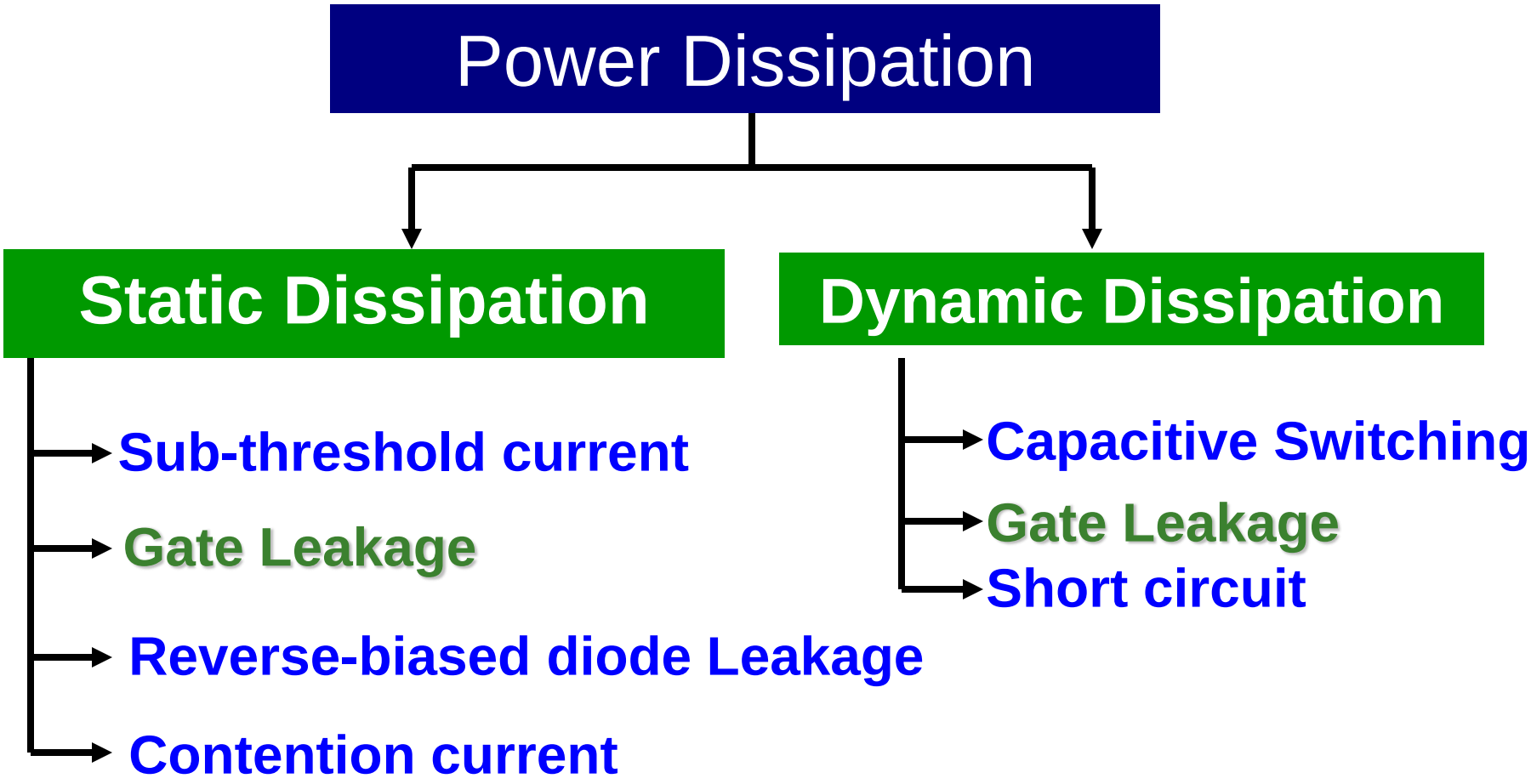
Nano-CMOS: Transistor Currents



I_1 : drain-to-source active current (ON state)
I_2 : drain-to-source short circuit current (ON state)
I_3 : subthreshold leakage (OFF state)
I_4 : gate Leakage current (both ON & OFF states)
I_5 : gate current due to hot carrier injection (both ON & OFF states)
I_6 : channel punch through current (OFF state)
I_7 : gate induced drain leakage (OFF state)
I_8 : band-to-band tunneling current (OFF state)
I_9 : reverse bias PN junction leakage (both ON & OFF states)

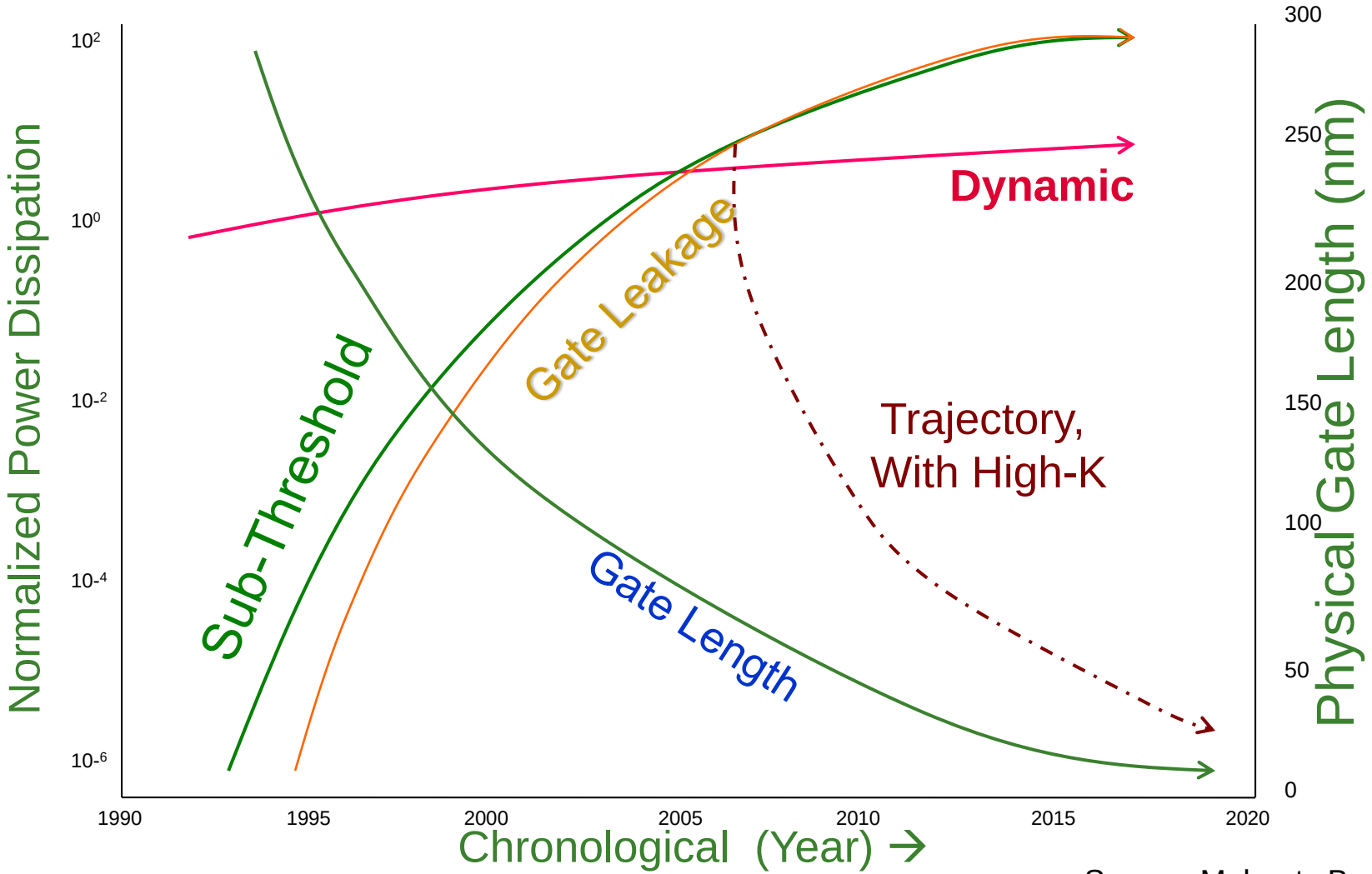
Source: Mohanty Book 2008

Nano-CMOS: Power Dissipation Types



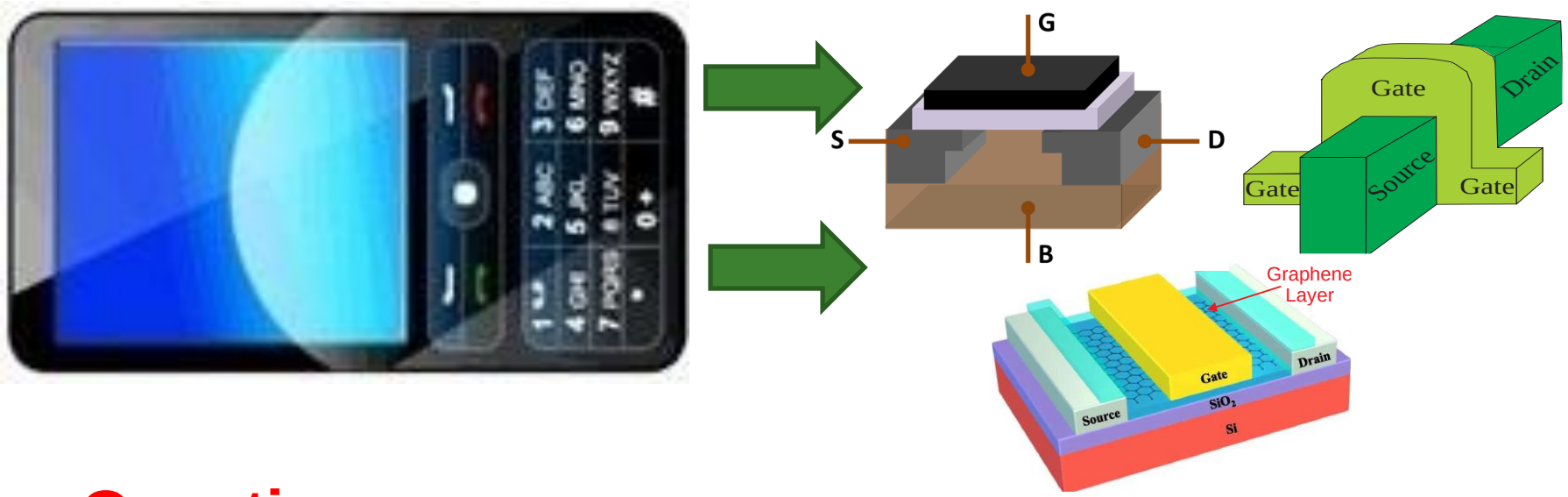
Source: Mohanty Book 2008

Nano-CMOS: Power Dissipation Trend



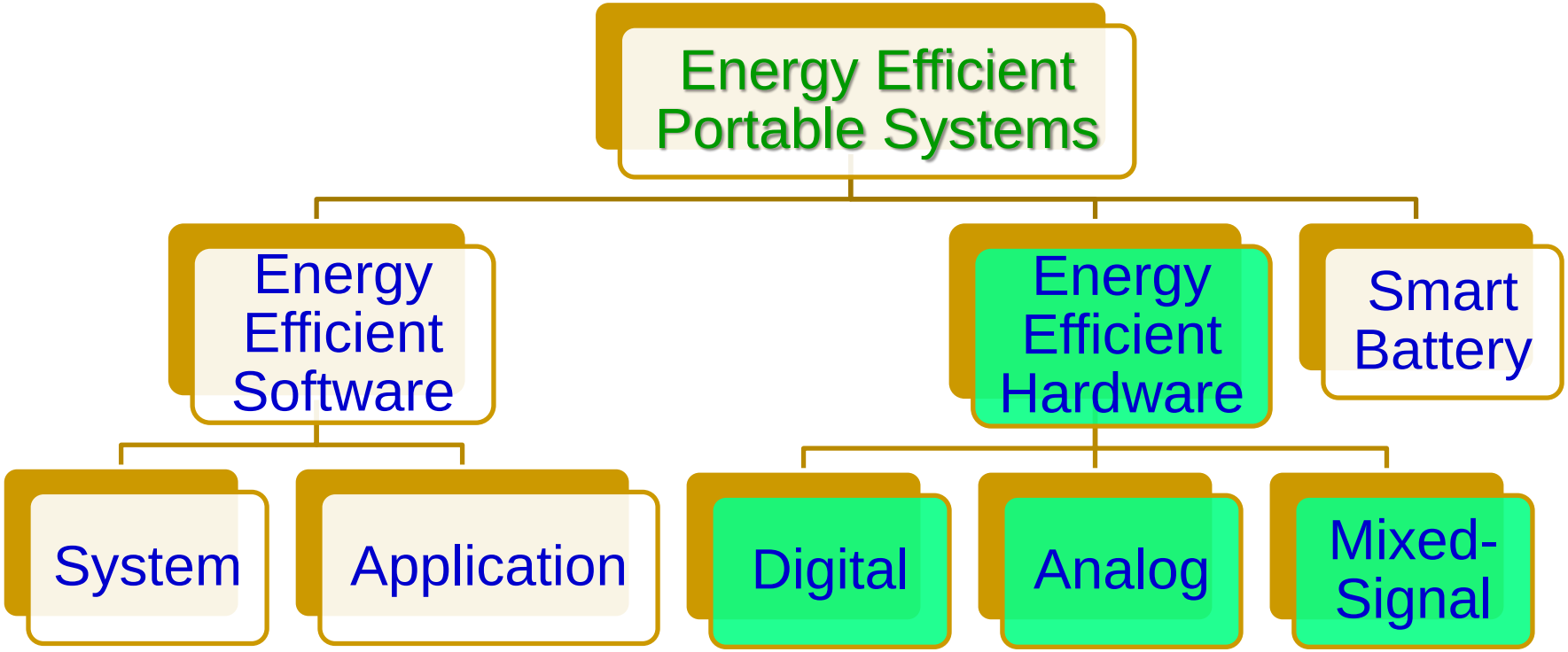
Source: Mohanty Book 2008

A Typical Nanoelectronic System: Research Questions



- **Questions:**
  - How to perform energy-efficient designs.
  - How to perform high-yield, energy efficient designs.
  - How to perform effortless, high-yield, energy efficient designs.

Energy Efficient Nanoelectronic Systems: Possible Solution Fronts

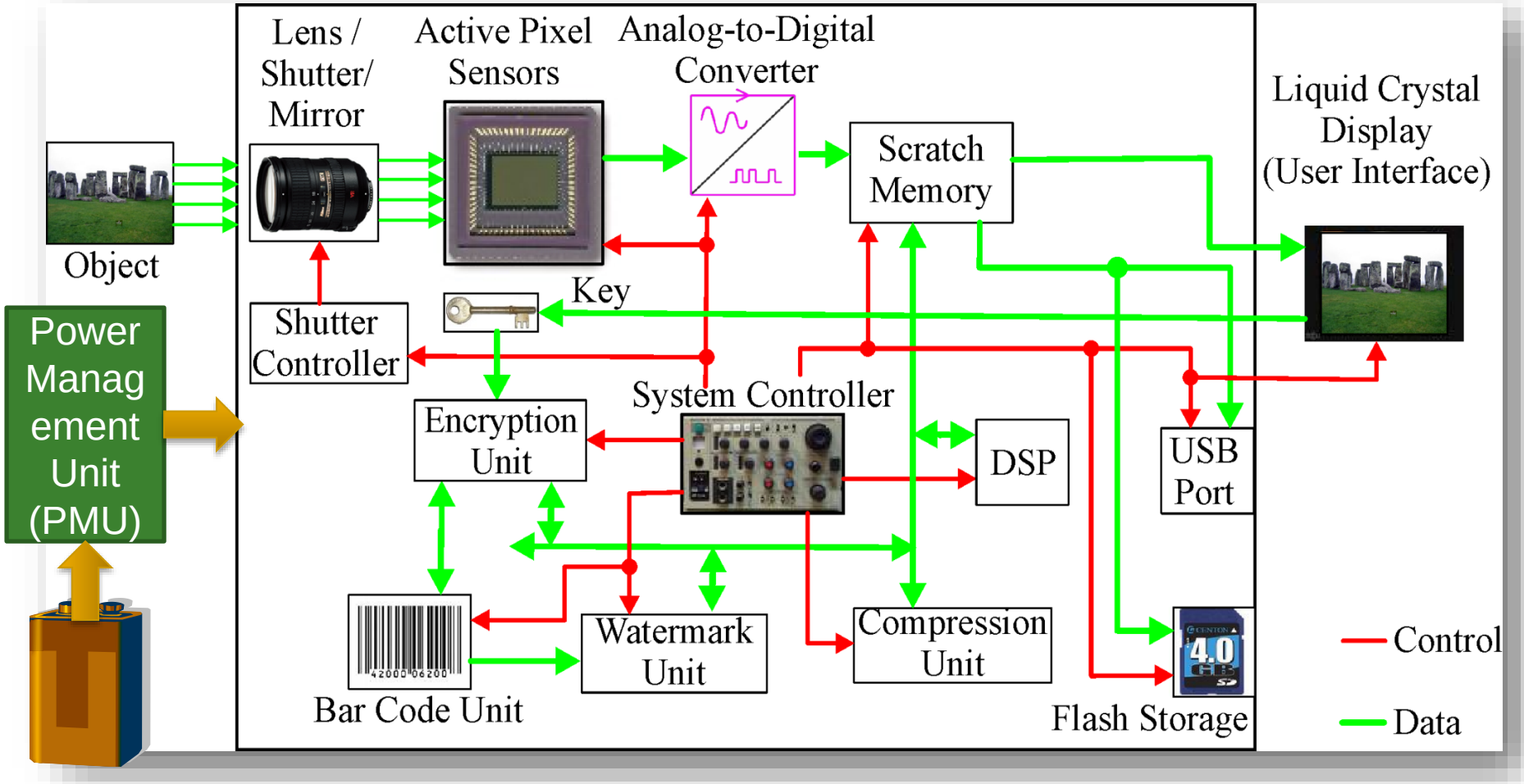


Energy Efficient Hardware -- 1

- Design of an Universal Level Converter for Dynamic Power Management

- S. P. Mohanty, E. Kougianos, and O. Okobiah, “Optimal Design of a Dual-Oxide Nano-CMOS Universal Level Converter for Multi-*Vdd* SoCs”, *Springer Analog Integrated Circuits and Signal Processing Journal*, Vol. 72, No. 2, August 2012, pp. 451--467.

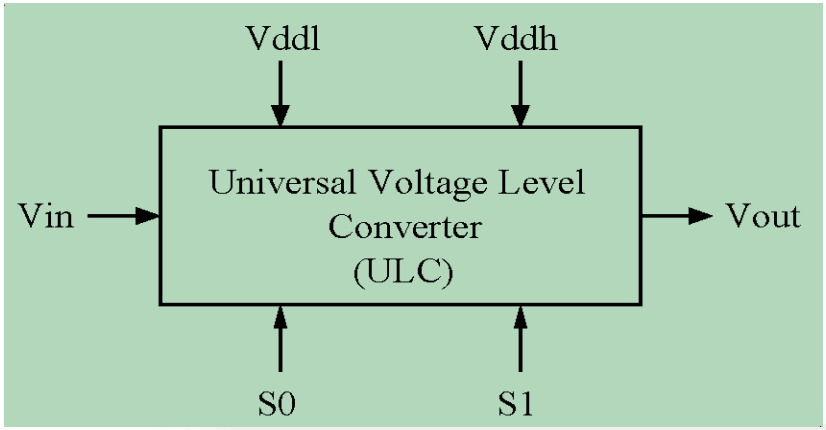
One Example Electronic System: Secure Digital Camera



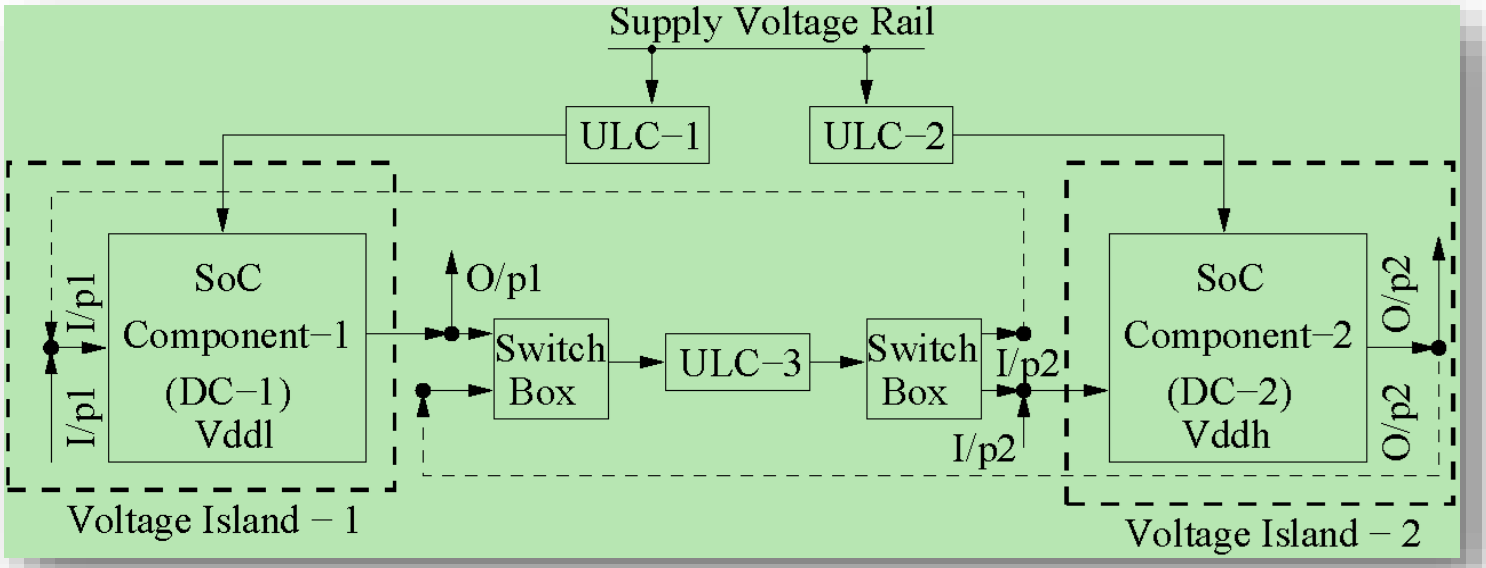
Power Management Unit (PMU)

- Manages the power distribution to the various subsystems to optimize energy consumption.
- Has built-in timers that put the different components to “sleep” or “wake-up”.
- The heart of PMU is a bank of Universal Voltage-Level Converters (ULCs).
- ULC sends different operating voltages to various subsystems and facilitates reconfigurability for power management.

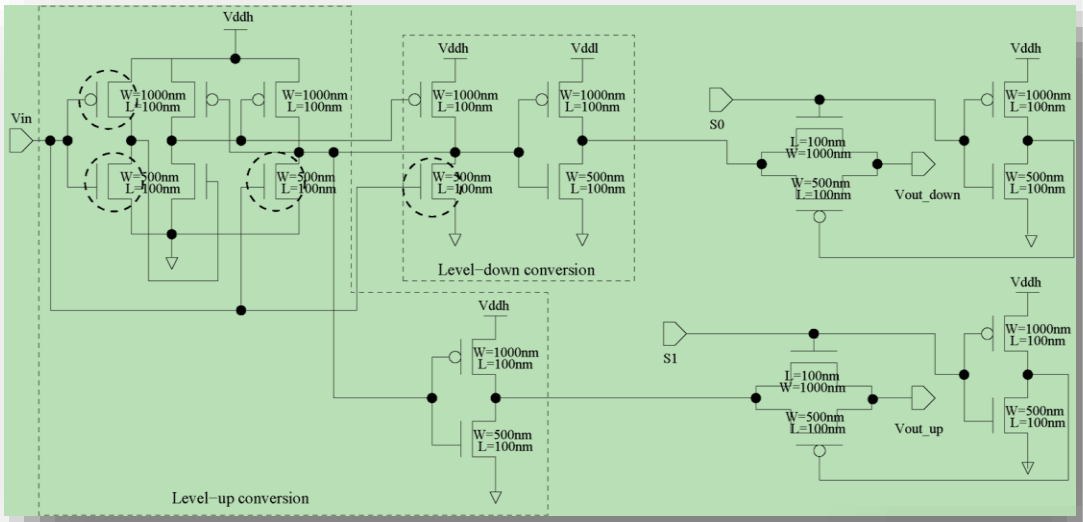
Universal Voltage-Level Converter: Use in a System



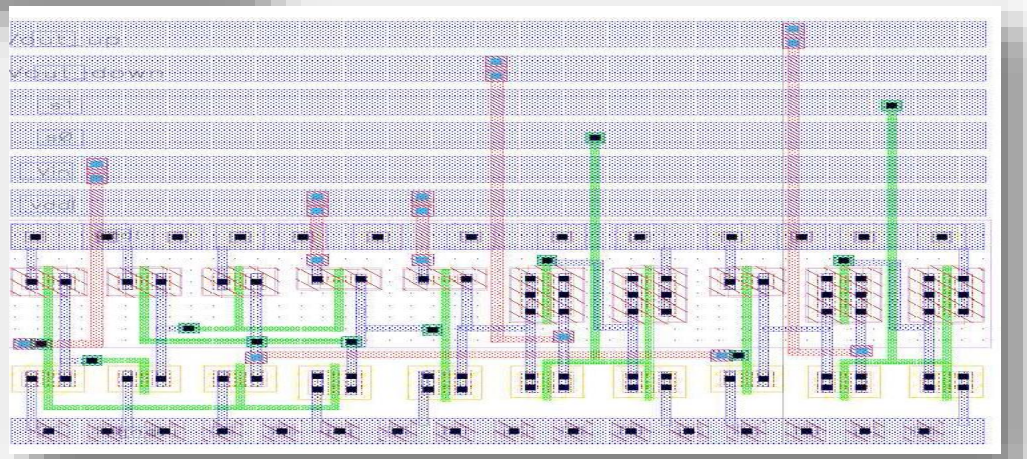
- ULC Input voltage signal V_{in}
- ULC Control signals S_1 and S_0
- ULC Supply voltages V_{ddl}, V_{ddh}
- ULC Output voltage signal V_{out}



Universal Voltage-Level Converter: One Topology



- 20 transistor area efficient design.
- Energy hungry transistors are circled.



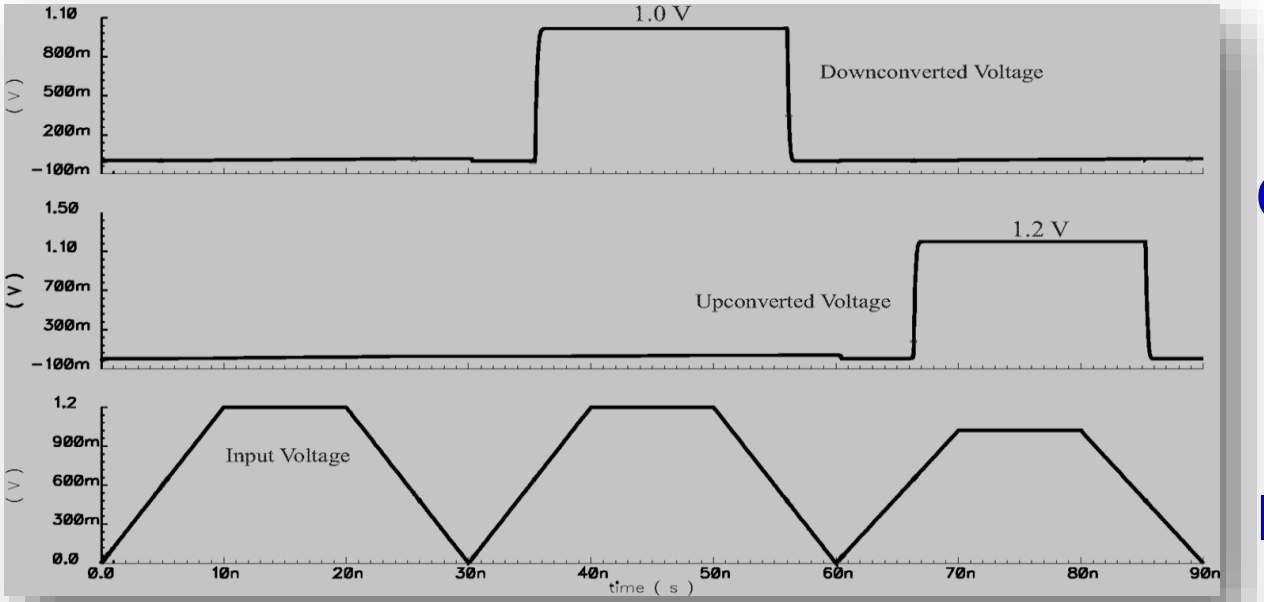
- Energy hungry transistors have thicker oxide.
- 90nm CMOS dual-oxide physical design of ULC.

Universal Voltage-Level Converter: Operations

Operations of the ULC:

- Level-up conversion
- Level-down conversion
- Blocking of input signal

Select Signal		Type of Operation
0	0	Block Signal
0	1	Up Conversion
1	0	Down Conversion



Output

Input

Universal Voltage-Level Converter: Has Minimal Overhead

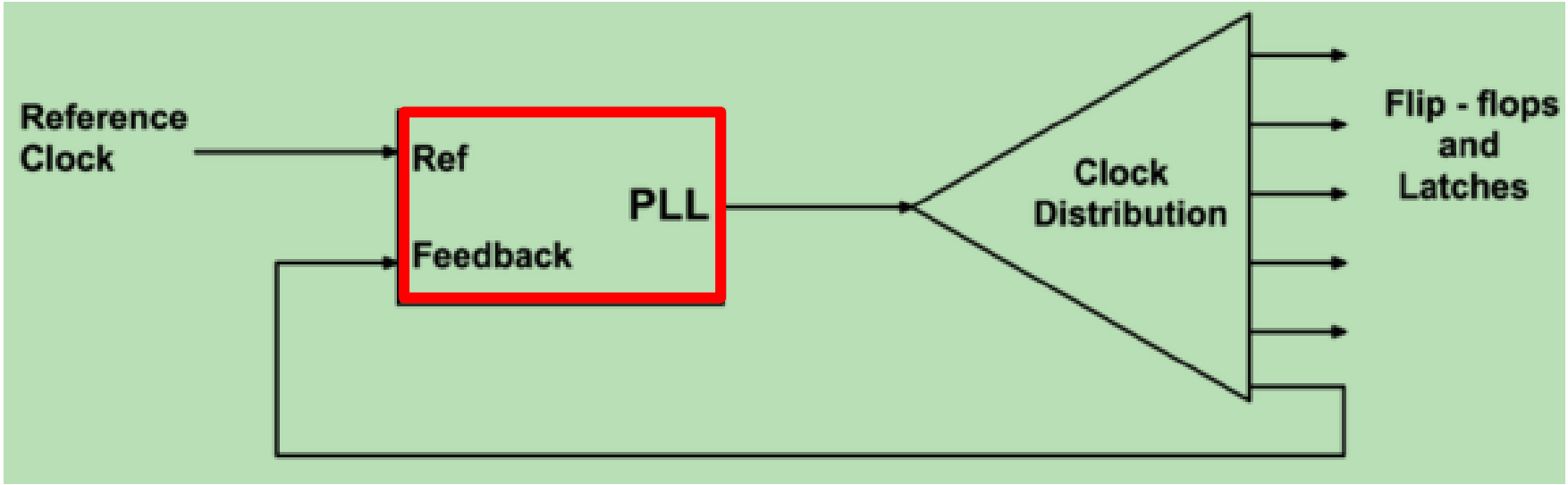
Designs	Technology (nm)	Power	Delay	Conversion	Design Approach
Ishihara 2004	130nm	---	127 ps	Level-up and down	Level converting flip flops
Yu 2001	350nm	220.57 µW	---	Level-up	SDCVS
Sadeghi 2006	100nm	10 µW	1 ns	Level-up	Pass transistor and Keeper transistor
Our ULC	90 nm	12.26 µW	113.8 ps	Level-up/down and block	All conversion types and Programmable

Energy Efficient Hardware -- 2

- Design of Energy-Efficient Phase-Locked Loop (PLL) for Clock Generation

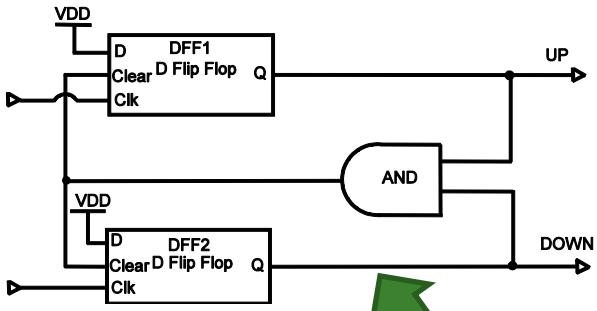
- O. Garitselov, S. P. Mohanty, and E. Kougianos, "Accurate Polynomial Metamodeling-Based Ultra-Fast Bee Colony Optimization of a Nano-CMOS PLL", *Journal of Low Power Electronics*, Volume 8, Issue 3, June, 2012, pp. 317--328.

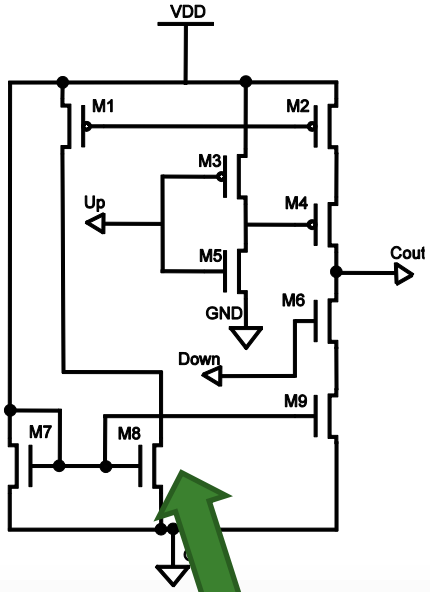
Phase Locked Loop: Application

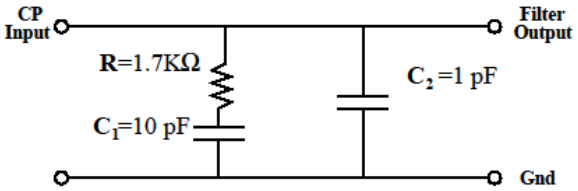


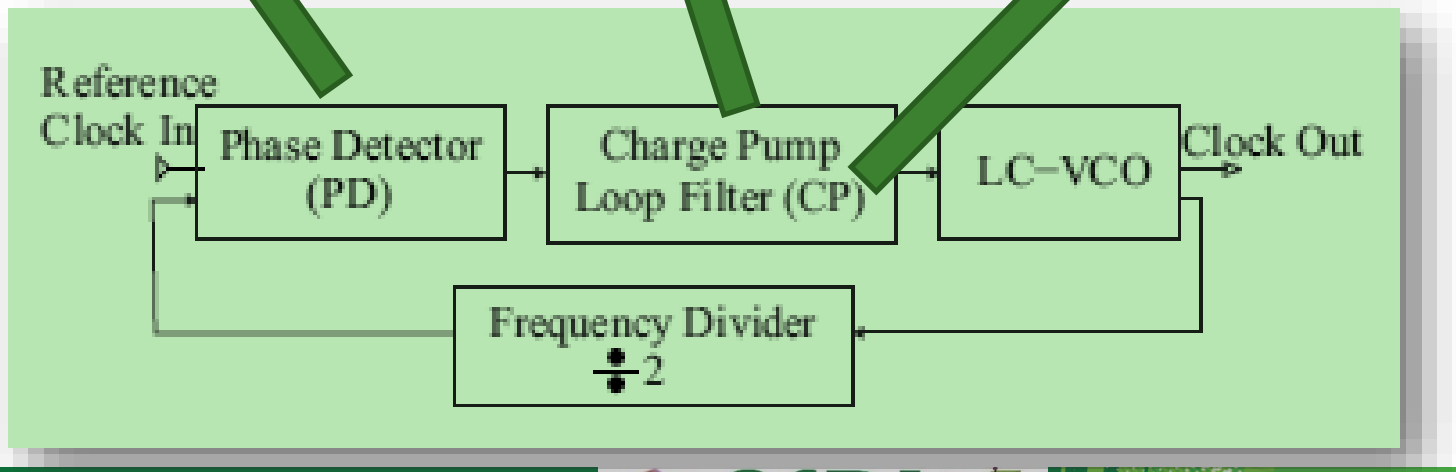
- PLLs are everywhere.
- PLLs drive clock distribution of a synchronous system.
- Sequential elements like Flip-Flop, Latches, and Registers need clock.

Phase Locked Loop: Block Diagram



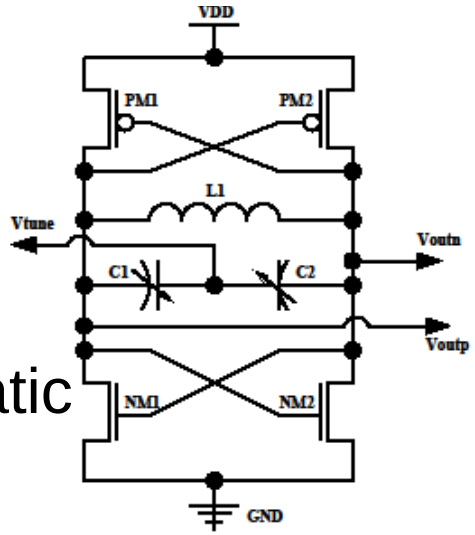




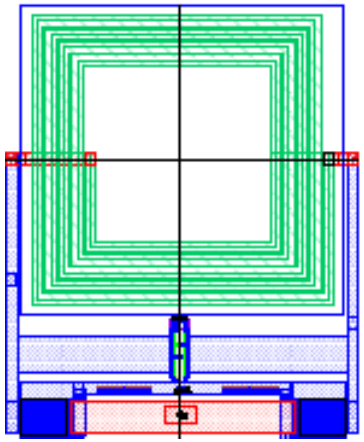


PLL Component: 180nm LC-VCO

Schematic

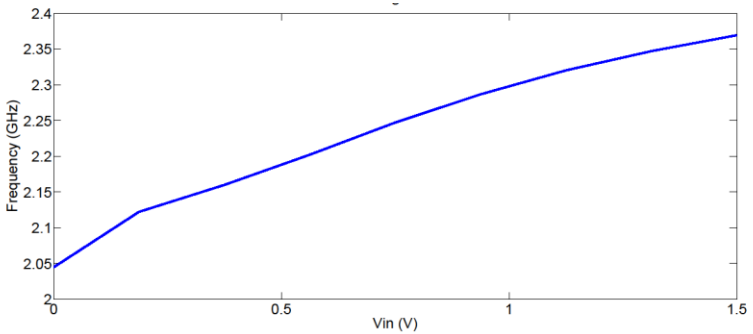


Layout



- LC-VCO oscillations are based on the sizes of L1 and C1=C2 varactors.

LC-VCO Tuning Range



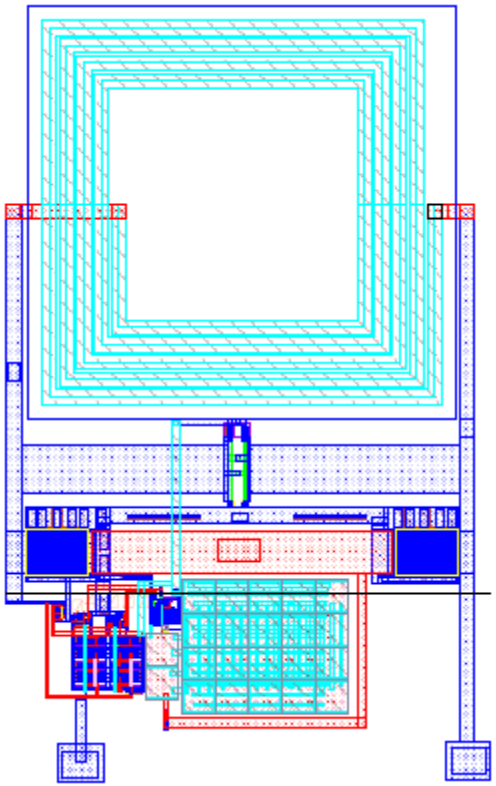
Optimization of the PLL

PLL parameters with constraints and optimized values.

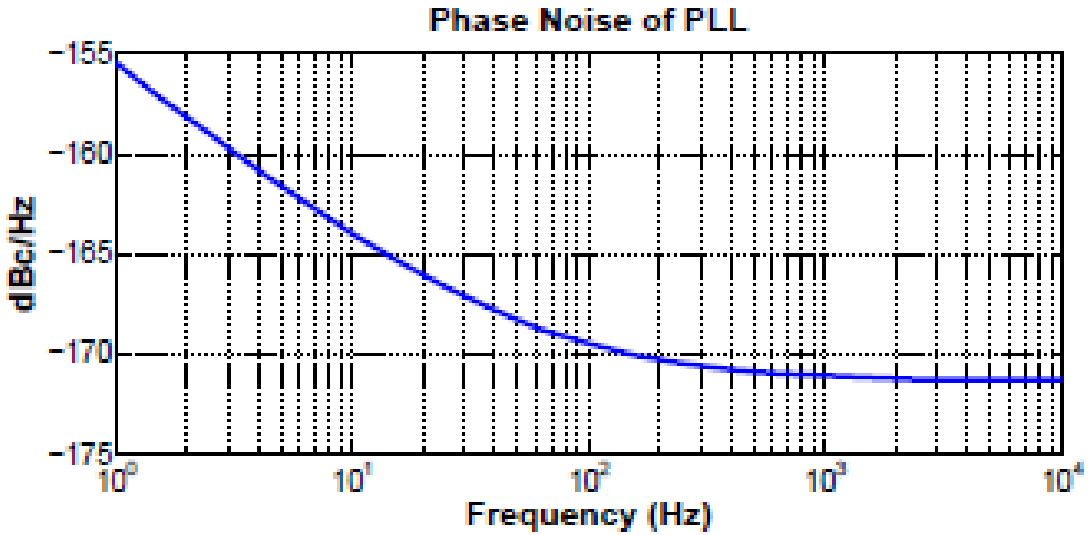
Circuit	Parameter	Min (m)	Max (m)	Optimal Value (m)
Phase Detector	W_{ppd1}	400n	2μ	1.66μ
	W_{npd1}	400n	2μ	1.11μ
	W_{ppd2}	400n	2μ	784n
	W_{npd2}	400n	2μ	689n
	W_{ppd3}	400n	2μ	1.54μ
	W_{npd3}	400n	2μ	737n
Charge Pump	W_{nCP1}	400n	2μ	1.24μ
	W_{pCP1}	400n	2μ	1.35μ
	W_{nCP2}	1μ	4μ	1.35μ
	W_{pCP2}	1μ	4μ	2.88μ
LC-VCO	W_{nLC}	3μ	20μ	18.62μ
	W_{pLC}	6μ	40μ	37.48μ
Divider	W_{p1Div}	400n	2μ	1.65μ
	W_{p2Div}	400n	2μ	1.54μ
	W_{p3Div}	400n	2μ	1.38μ
	W_{p4Div}	400n	2μ	1.96μ
	W_{n1Div}	400n	2μ	1.09μ
	W_{n2Div}	400n	2μ	1.17μ
	W_{n3Div}	400n	2μ	1.29μ
	W_{n4Div}	400n	2μ	1.95μ
	W_{n5Div}	400n	2μ	536n

- An exhaustive search of the design space of 21 parameters with 10 intervals per parameter requires 10^{21} simulations.
- Time savings are enormous: ~10^{20}x.
- This can lead to reduction of design effort and chip cost.

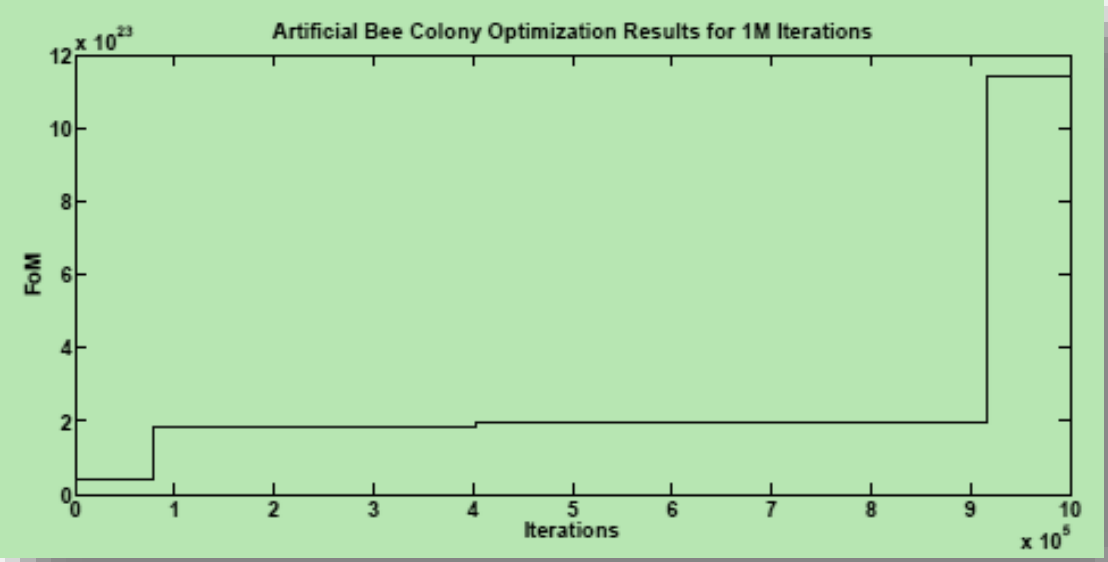
Complete PLL : 180nm



PLL physical design for 180nm



Optimization of the PLL …



Artificial Bee-Colony Optimization algorithm progression for the selected FoM.

Power and Jitter Results of the PLL

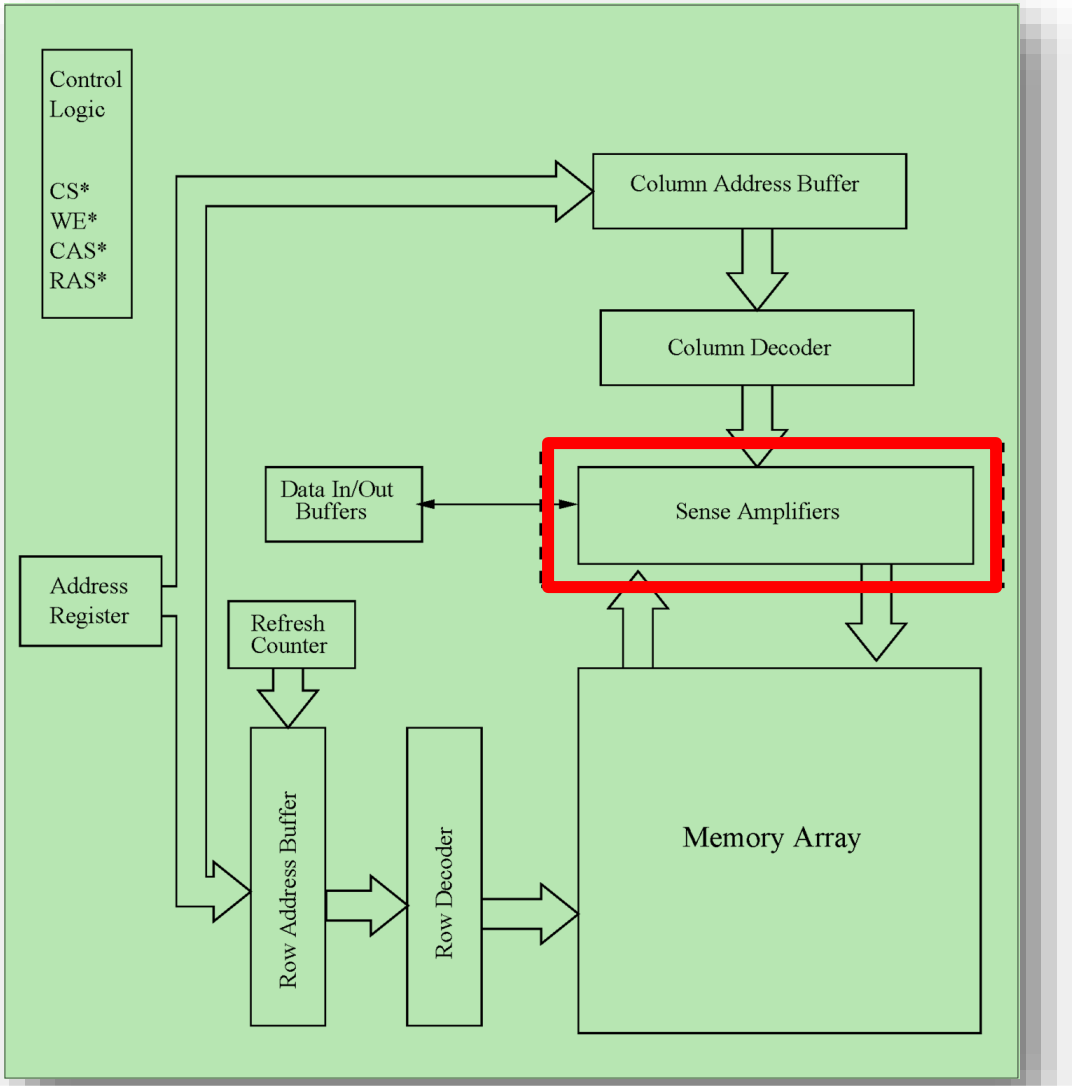
Metric	Before Optimization	After Optimization	Improvement
Power	9.29 mW	0.87 mW	90.6%
Jitter Vertical	168.35μV	3.28 nV	$\sim$100%
Jitter Horizontal	189 ps	180 ps	4.8%

Energy Efficient Hardware -- 3

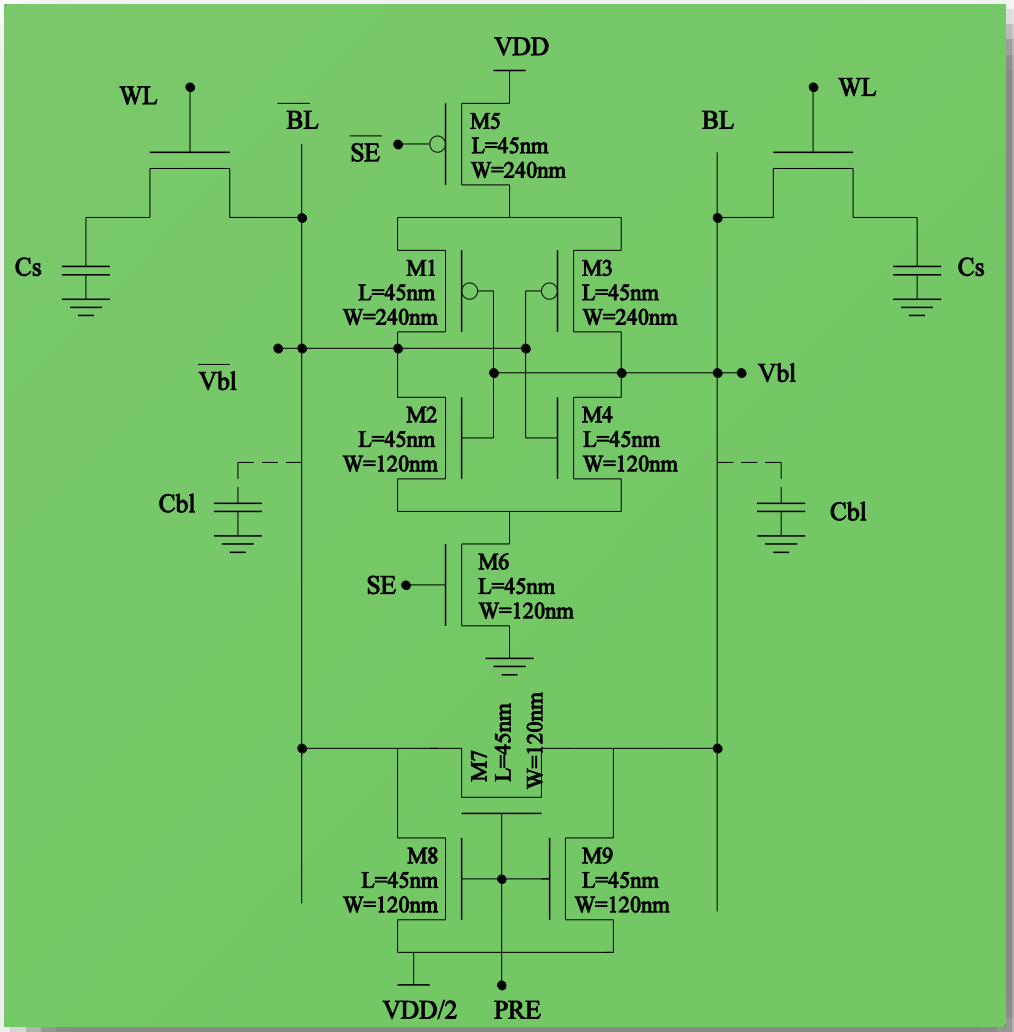
- Design of Energy-Efficient Sense Amplifier for Memory

- O. Okobiah, S. P. Mohanty, E. Kougianos, and M. Poolakkaparambil, “Towards Robust Nano-CMOS Sense Amplifier Design: A Dual-Threshold versus Dual-Oxide Perspective”, in *Proceedings of the 21st ACM/IEEE Great Lakes Symposium on VLSI (GLSVLSI)*, 145--150, 2011.

Sense Amplifier : Application

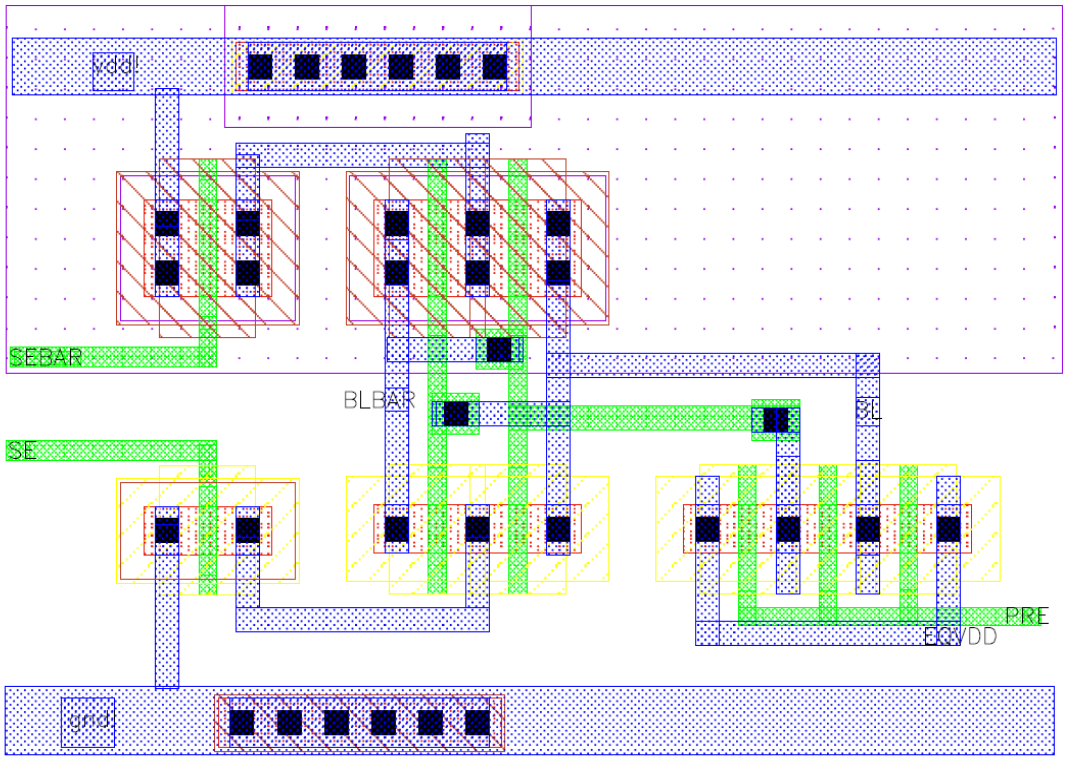


Functional Design of Sense Amplifier



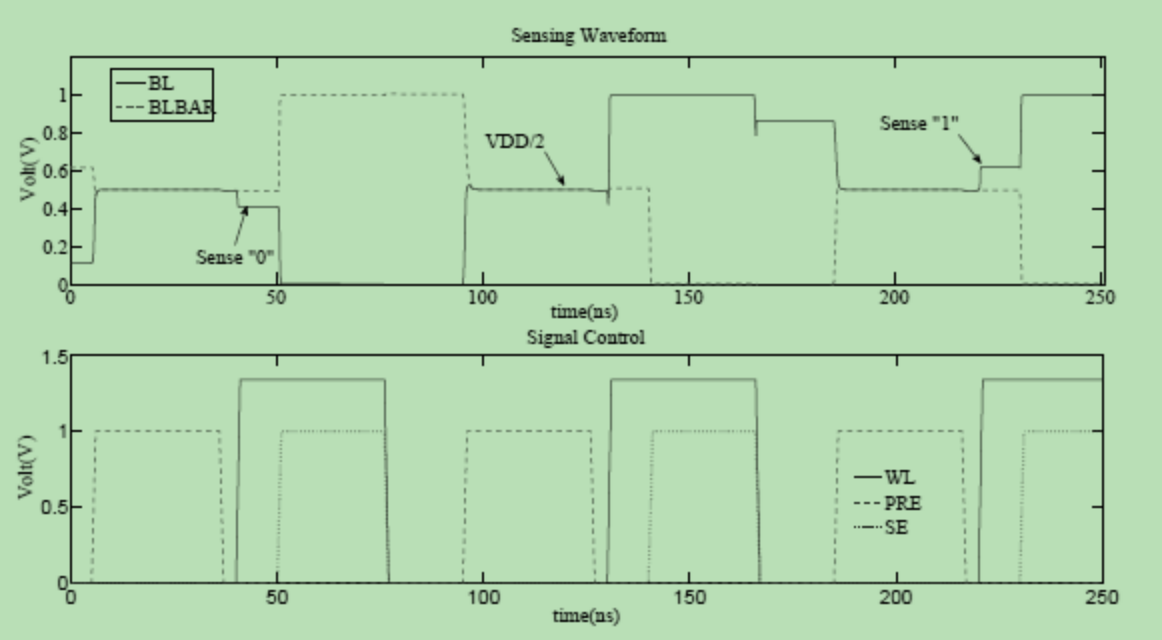
- M1, M3, M2 and M4 form cross-coupled inverters.
- M7, M8 and M9 form the precharge circuit

45nm Sense Amplifier Layout



- L_n = 45nm
- L_p = 45nm
- W_n = 120nm
- W_p = 240nm

45nm Sense Amplifier: Simulation



Design	Precharge time (ns)	Sense delay (ns)	Power, (µW)	Sense Margin (mV)	Area (µm²)
Schematic	10.31	1.79	1.84	26.91	-
Layout	10.40	1.91	1.88	26.86	6.045

45nm Sense Amplifier: Characterization of Optimal Design

Circuit	Precharge Time	Power Dissipation	Sense Delay	Sense Margin
Schematic	18.024 ns	1.166 µW	7.460 ns	29.331 mV
Layout	18.20 ns	1.175 µW	7.45 ns	29.256 mV
Dual-V_{th}	6.61 ns	0.941 µW	3.476 ns	40.851 mV
Dual-T_{ox}	6.596 ns	0.895 µW	3.464 ns	40.77 mV

Sense Amplifier: Comparison

Research	Parameter	Feature	Approach	Result Improvement
Chow MWSCAS-2007	C_{BL}	Sense Speed	Spice simulations	Sense speed – 40%
Laurent TCASI 2002	C_{BL}, V_{th}, β	Signal Margin	Spice Simulations	-
Choudhary ISVLSI 2009	V_{th}, L, W	Yield	Monte Carlo analysis	Improved Yield
Singh TVLSI 2004		SE rise time	Spice simulations	Eliminated offset voltage
Our Sense Amplifier	Dual-V_{th}, T_{ox}	Process variability	Optimization	Sense delay – 54% Sense margin – 40% Average Power – 24%

Conclusions

- 35% of total energy in USA is consumed by electronics.
- Battery dependency is an critical constraint for portable systems.
- Energy efficient hardware, software at the same time better battery design needed for effective solutions.
- Smartphones need to have energy-efficient analog and RF components as WiFi and GSM communication consume significant portion of battery life.
- Energy-efficient level converters can perform better power management.
- 180 nm PLL design example consumed 90% less power.
- 45nm sense amplifier example consumed 24% less power.

Thank You !!!

Slides Available at:
http://www.cse.unt.edu/~smohanty