iVAMS: Intelligent Metamodel-Integrated Verilog-AMS for Circuit-Accurate System-Level Mixed-Signal Design

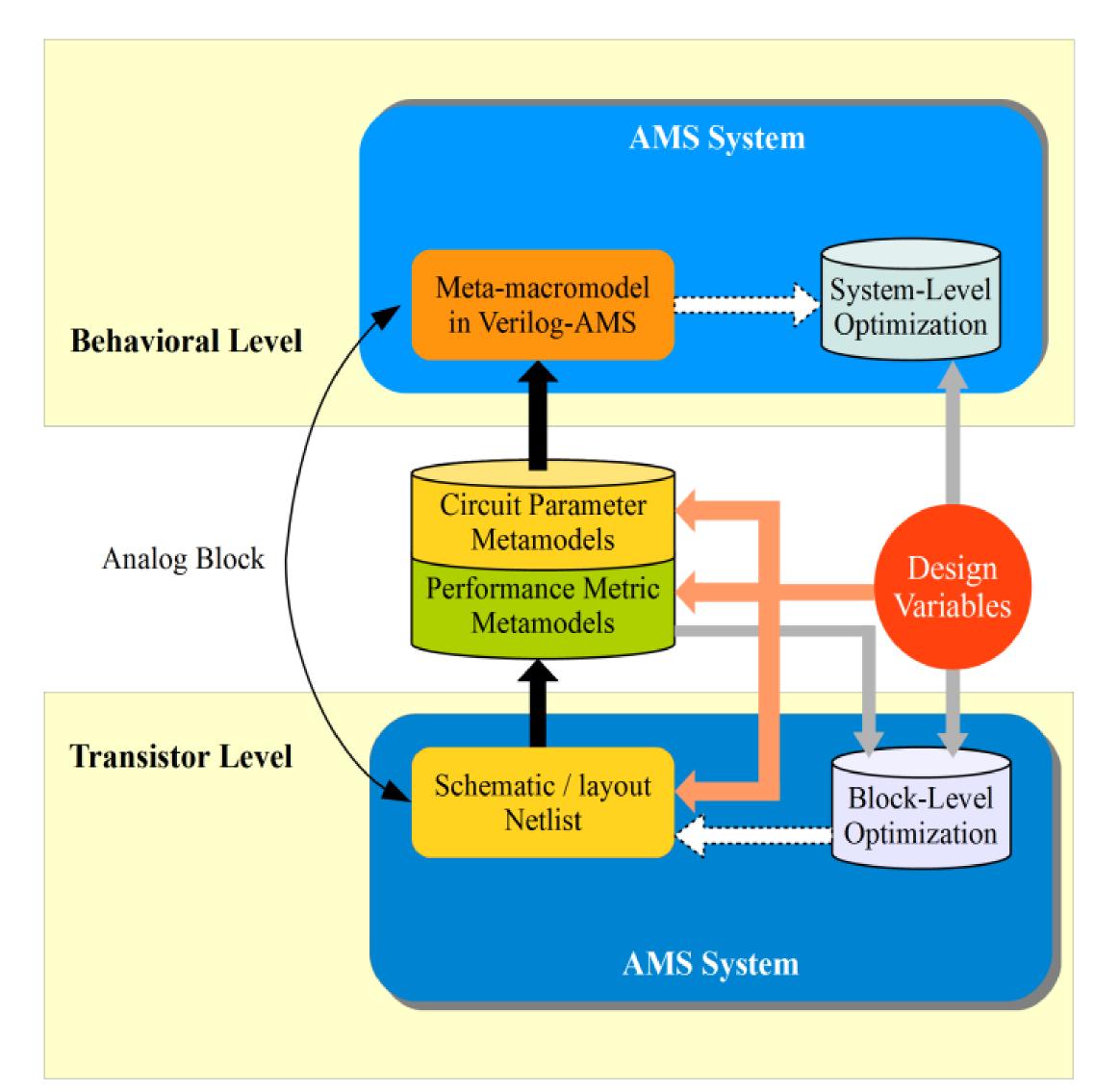
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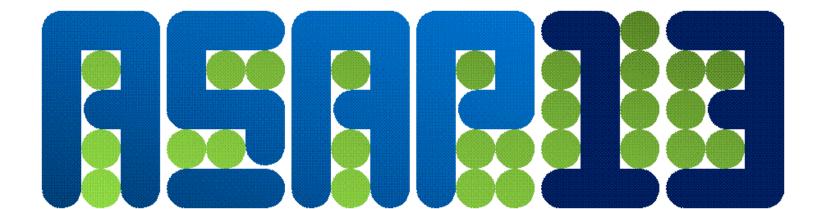
Abstract

The gap between abstraction levels in analog design is a major obstacle for advancing analog and mixedsignal design automation. Intelligent surrogate models for low-level analog building blocks are needed to bridge behavioral and transistor-level simulations. Parameterized behavioral models in Verilog-AMS the neural network metamodels are based on efficient system-level design constructed for exploration. To the best of the authors' knowledge this is the first paper to integrate artificial neural network models in Verilog-AMS. To demonstrate the application of iVAMS, a biologically-inspired "firefly optimization algorithm" is applied to an OP-AMP design. The optimization process is sped up by $5580 \times$ due to the use of iVAMS with negligible loss in accuracy.

iVAMS Concept

iVAMS aims at closing the gap between behavioraland transistor-level Analog/Mixed-Signal (AMS) design exploration. Parameterized Verilog-AMS modules incorporating transistor-level non-idealities are provided for high-level design exploration. Efficient metamodels are generated for low-level block optimization. The concept is illustrated below:

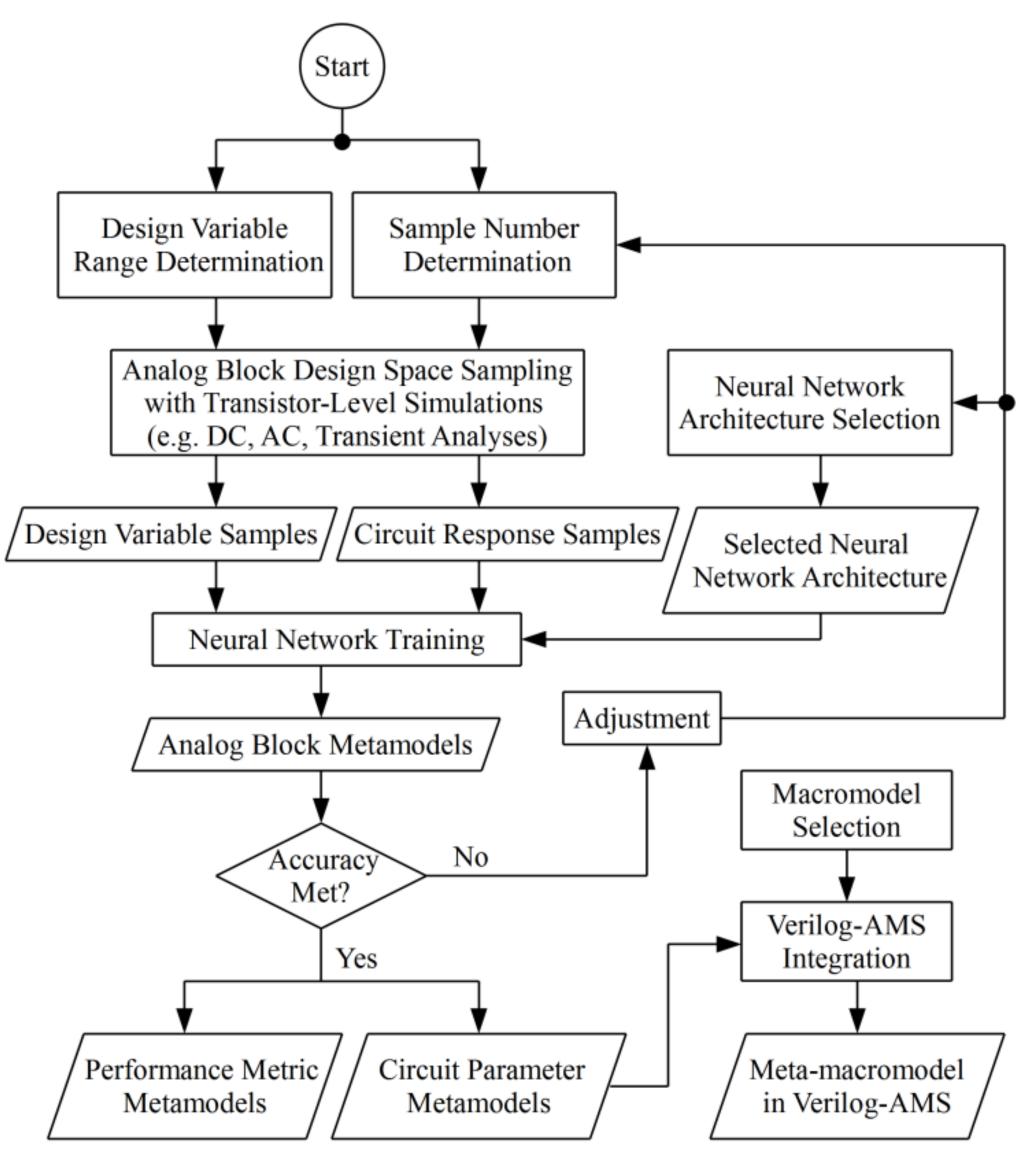




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iVAMS Generation

Given an analog block, the goal of iVAMS generation is to obtain the neural network metamodels and the meta-macromodel integrated Verilog-AMS module.

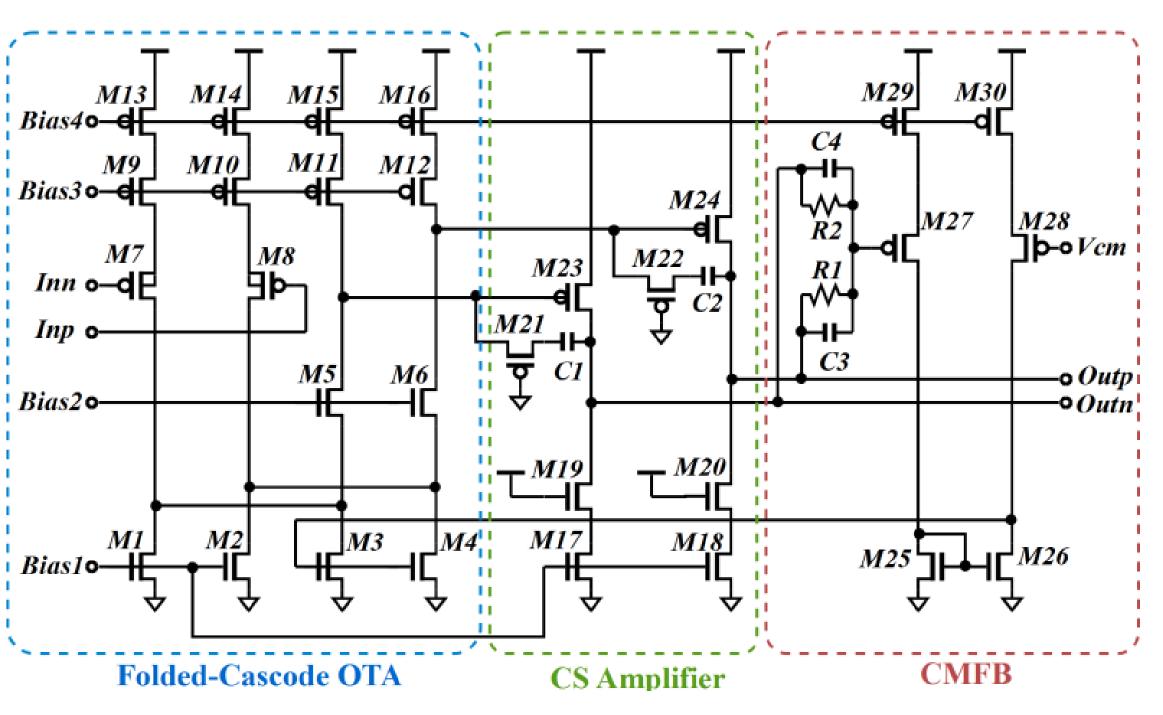


Case Study Circuit: Op Amp

iVAMS is applied to a fully-differential Op Amp: • 90 nm CMOS process, 1-V supply.

• 16 design variables (Ls and Ws, bias current...). Metamodels:

- neural networks with a single hidden layer.
- 4-neuron hidden layer is used.





Metamodel Accuracy

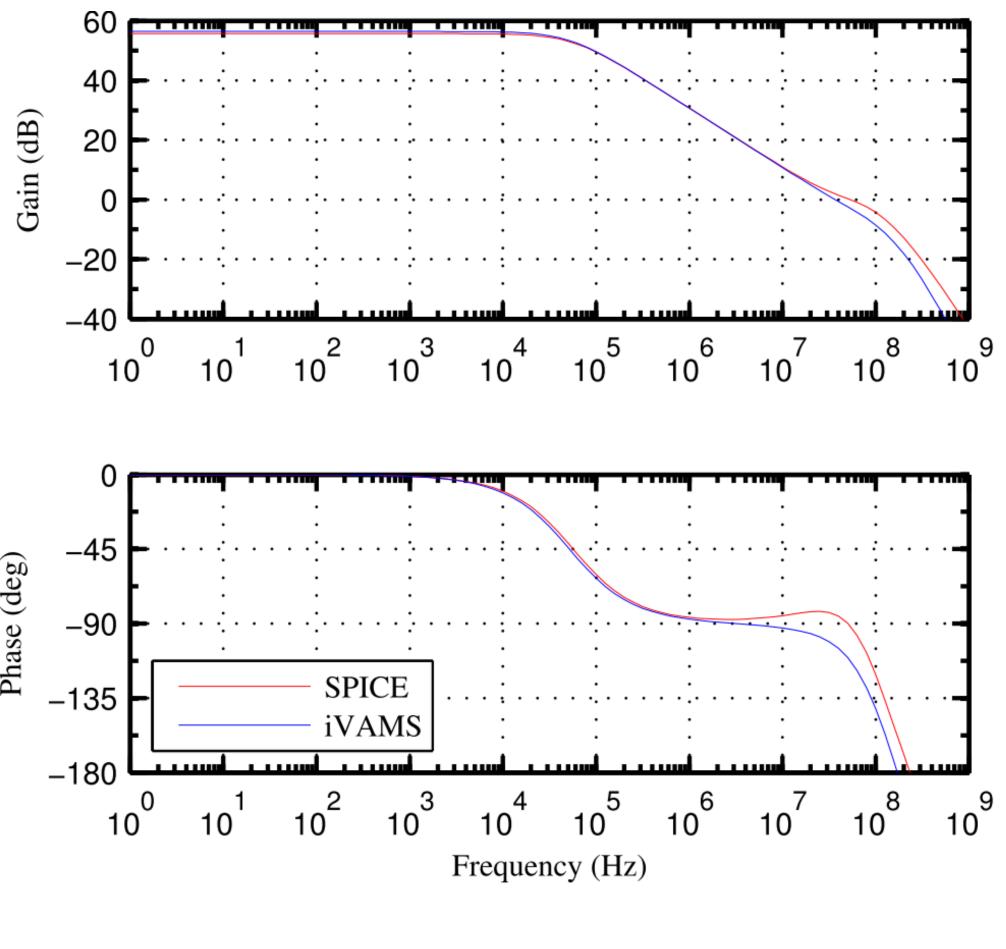
• The neural networks were trained using 500 samples. • A verification set consists 2000 samples were used.

Metamodel		Accuracy Metric				
Output	Туре	R^2	RMAE	RRSE	RMSE	
A_0 PO 0.973 1.044	NN	0.959	1.324	0.202	41.93 V/V	
	1.044	0.163	33.78 V/V			
BW	NN	0.987	0.894	0.116	2.12 kHz	
DW	PO	0.986	0.965	0.117	2.14 kHz	
PM	NN	0.901	2.161	0.317	RMSE 41.93 V/V 33.78 V/V 2.12 kHz	
1 111	PO	0.348	4.466	4 0.202 41.93 V/V 4 0.163 33.78 V/V 4 0.116 2.12 kHz 5 0.117 2.14 kHz 6 0.317 4.99° 5 0.105 0.292 mV/ns 6 0.105 0.292 mV/ns 8 0.062 8.306 μW		
SR	NN	0.989	0.483	0.105	0.292 mV/ns	
	PO	0.985	0.662	0.119	0.332 mV/ns	
P_D	NN	0.996	0.523	0.062	$8.306 \ \mu W$	
	PO	0.980	1.314	0.141	$18.817 \ \mu W$	

The circuit parameters, Ip, In, gm, the poles and zeros in the transfer function are parameterized and estimated using neural network metamodels:

 $\hat{y} =$

The above mathematical function is implemented in Verilog-AMS. The SPICE and iVAMS simulations are compared:

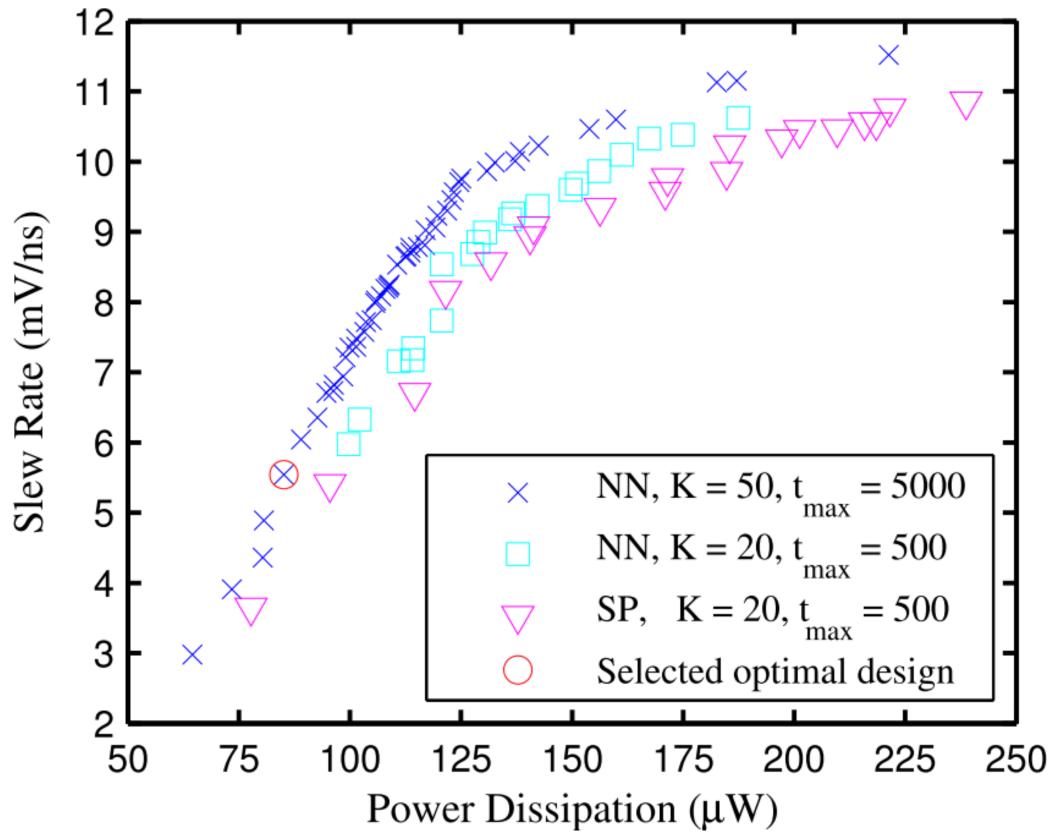




Block-Level Multi-objective Optimization

• Objective: minimize power and maximize slew rate. • A metaheuristic multi-objective firefly algorithm is employed to generate the Pareto front.

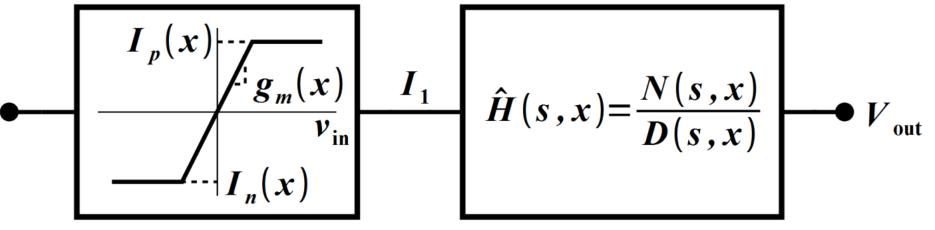
• The results from neural network metamodel and SPICE simulations are compared:



Optimization #	1	2	3
Model Type	NN	NN	SP
Number of Pareto Points, K	50	20	20
Number of Iterations, t_{max}	5000	500	500
Runtime	0.57 h	84.63 s	131.18 h
Normalized Speed	_	$\times 5580$	1

Meta-Macromodel Construction

The following macromodel is selected to be implemented in Verilog-AMS:



$$b_{21} + \sum_{j=1}^{M} w_{2,j} \cdot \tanh\left(b_{1j} + \sum_{i=1}^{N} w_{1,ij} \cdot x_i\right)$$

Conclusion

iVAMS:

- is a circuit-level modeling framework.
- creates efficient models that bridge different abstraction levels of AMS designs.
- is compatible with optimization algorithm.
- Future research includes adding yield-estimation capability.



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