Process Variation Tolerant 9T SRAM Bit Cell Design

G. K. Reddy[1], K. Jainwal[1], J. Singh[2] and S. P. Mohanty[3]
[1]Jaypee University of Engineering and Technology, India.
[2]Indian Institute of Information Tech., Design and Manufacturing, Jabalpur, India.
[3]University of North Texas, Denton, TX, USA.
Email: {gk.reddy,kapil.jainwal}@juet.ac.in, jawar@iiitdmj.ac.in, saraju.mohanty@unt.edu

Presented By
Oghenekarho Okobiah

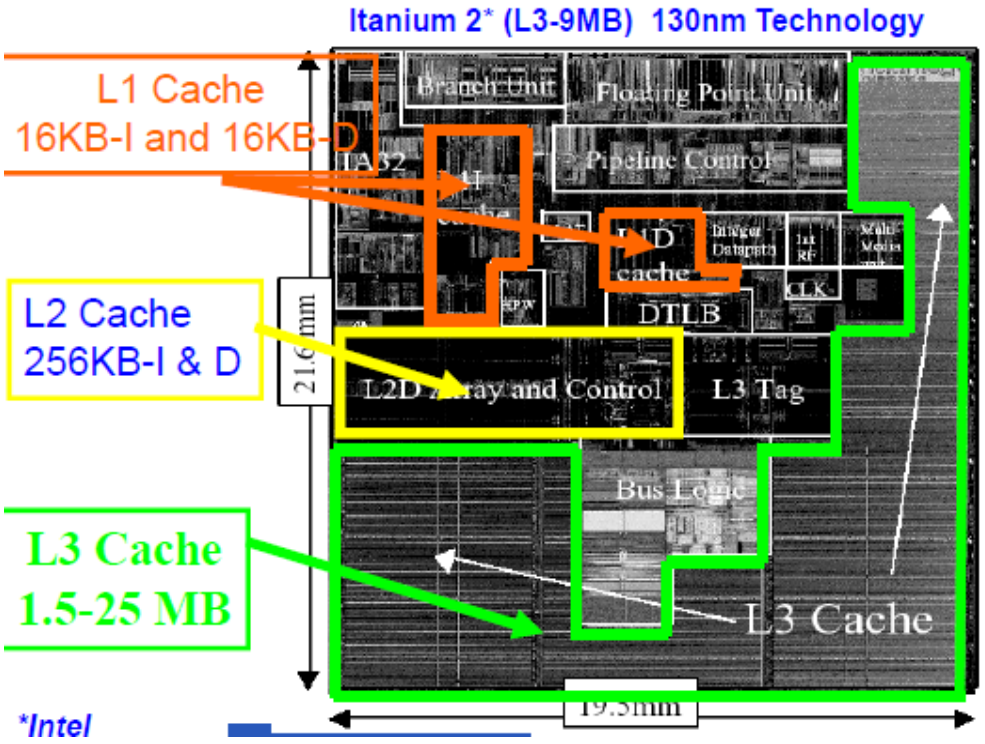
For any questions contact:
Jawar Singh (jawar@iiitdmj.ac.in)

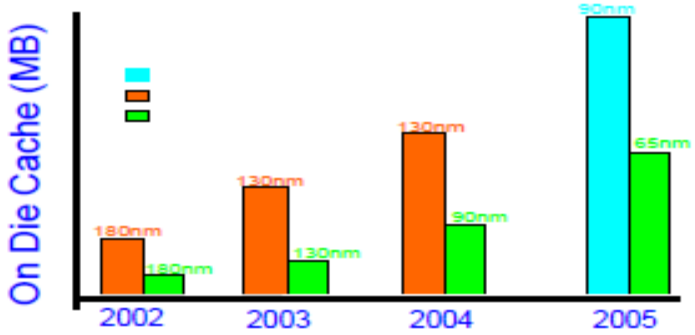
Contents

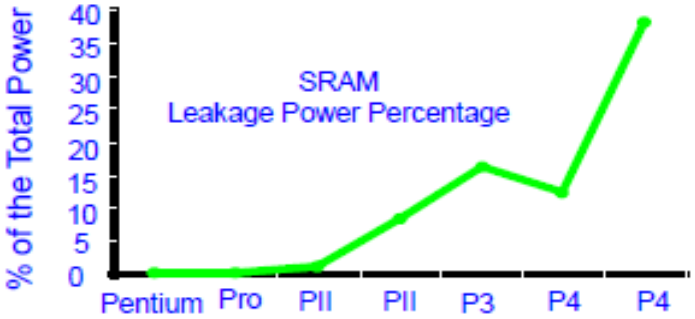
- Introduction
- Need of Efficient SRAM Design
- Nano-CMOS SRAM Design Challenges
- Standard 6T SRAM
- Proposed 9T SRAM
- Simulation Results
- Conclusion

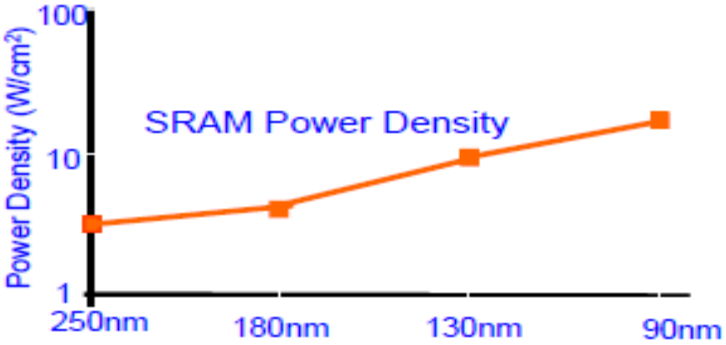
Why Efficient SRAM Design ?

- Amount of on-die caches increases.
- Up to 60% of the die area is devoted for caches.
  in typical processor and embedded application.
- Largely contributes for leakage and power density.







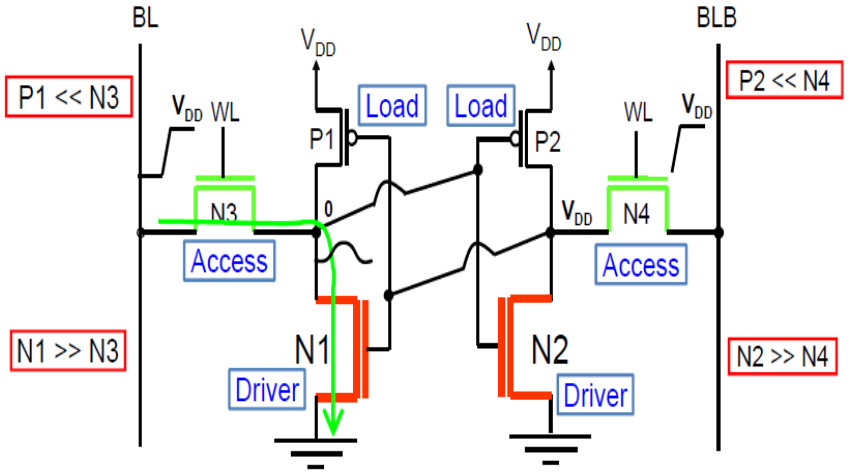


Single – Ended SRAM (SE-SRAM)

Nano-CMOS SRAM Design Challenges...

In Nano-CMOS regime following are the major issues:

- Data stability and functionality
  - Non-destructive read
  - Successful write
  - Noise sensitivity
- Proper sizing of the transistors
  - To improve the write ability
  - To improve the read stability
  - To improve the data retention



- Minimum size of transistors to maximize the memory density.
- Minimum leakage for low-power design.
- Minimum read access time to improve the performance.

- For proper read stability: N1 and N2 are sized wider than N3 and N4.
- For successful write: N3 and N4 are sized wider than P1 and P2.
- Minimum sized transistors do not provide good stability and functionality.
- SRAM cell ratio (β): Ratio of driver transistor's W/L to access transistor's W/L.

Introduction

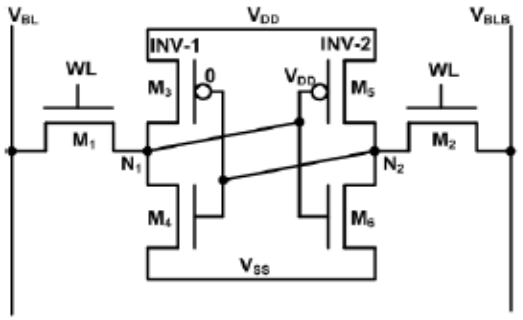
- As cache is embedding in every Integrated Circuit (IC) for better performance.The importance of SRAM which will work at low power and in nano-regime has been increased in the recent past to meet energy requirement of the portable or hand held devices.
- Several SRAM bitcell topologies have been proposed in the recent past to improve read stability like 6T,8T,10T,9T(with separate read buffer), but every proposed topology works under certain limitations.
  - 6T SRAM Bitcell : Fails to operate in sub-V**TH.**
  - 8T SRAM Bitcell : Uses Single ended sensing, high bitline leakage affects the number of rows (or cells) that can be connected to a single bitline.
  - 10T SRAM Bitcell : Uses Single ended sensing, large signal sensing and hierarchical bitline organization results in poor array efficiency and high power consumption.
  - 9T SRAM Bitcell (with separate read buffer): Read speed decreases because of body effect.
- To overcome all these limitations, in this paper, we have proposed a new 9T SRAM without separate read and write bitlines (or a read buffer).

Standard 6T SRAM ….

The main parameters should keep in mind while designing SRAM bitcells are bitcell area, speed, stability, power consumption and yield.

Operations performed by 6T SRAM

1. Read Operation
2. Write Operation
3. Hold Operation

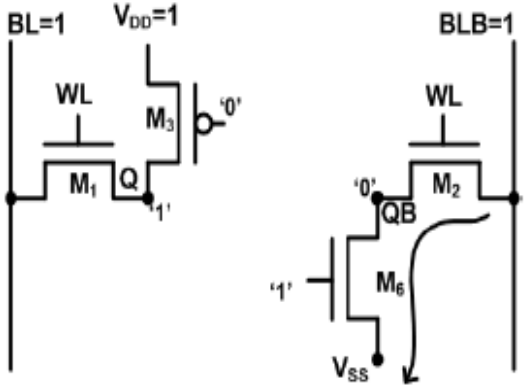


1. Schematic diagram of a standard 6T SRAM bitcell.

6T SRAM Limitations :

- A standard 6T SRAM shows poor read stability as technology scale down to nano-regime.
- By increasing the bitcell ratio, power consumption and write time increases which incur loss of power, performance and increase in area overhead (as shown in Table I).

Cell Ratio : $\frac{W_4/L_4}{W_1/L_1} = \frac{W_6/L_6}{W_2/L_2}$



2. Read equivalent diagram of a standard 6T SRAM bitcell.

Standard 6T SRAM

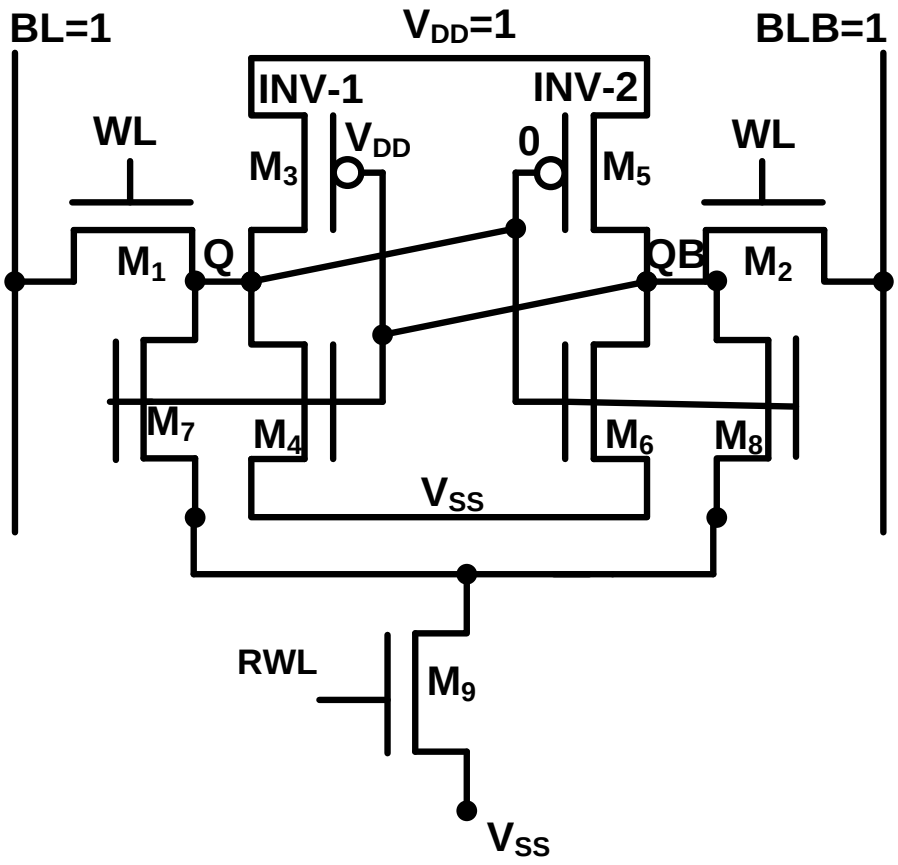
TABLE I
VARIATION IN DIFFERENT PARAMETERS OF STANDARD 6T WITH BITCELL RATIO.

bitcell Ratio	1	1.5	2	2.5	3
SNM (mV)	27.4	60.7	79.7	91.9	102.3
Write Time (ps)	35.38	42.25	47.48	52.17	57.15

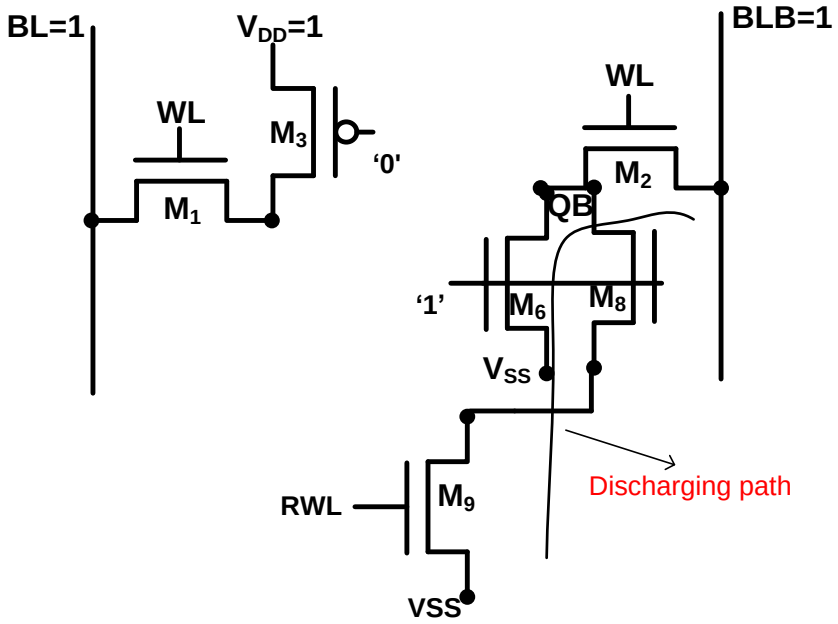
From the above table, we can conclude that by increasing the cell ratio, we can improve read SNM, at the same time there is increase in write time .

In the design, we proposed a new 9T SRAM cell in which read SNM improves by increasing the cell ratio without affecting its write speed.

Proposed 9T SRAM Cell



9T SRAM Read Equivalent



Cell Ratio= $\frac{(W_4/L_4 + W_7/L_7)}{W_1/L_1} = \frac{(W_6/L_6 + W_8/L_8)}{W_2/L_2}$

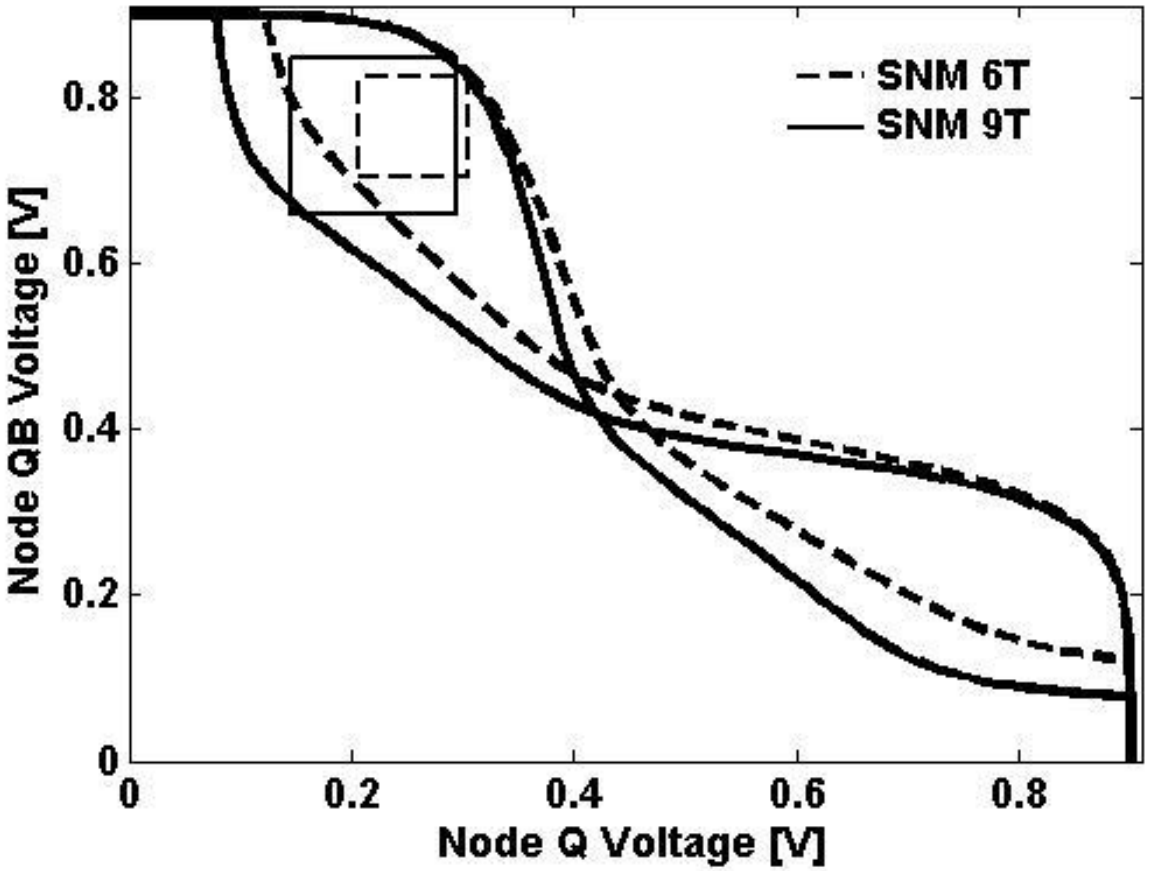
During write RWL=0 ,so Proposed cell will work as standard 6T SRAM cell. Increasing cell ratio does not affect write speed

Simulation Results

- In order to investigate the effect of process variations, 3000 Monte Carlo (MC) simulations were preformed for 6T and the proposed 9T SRAM bit cells for read stability margins.
- We assumed a 15% variation in V_{TH} with ±3 Gaussian distribution as an independent random variable for all the transistors in SRAM cells (6T and 9T). We use, 32nm Predictive Technology Model (PTM) models for low power applications incorporating high k/metal gate and stress effect.
- Following technology parameters were used for simulation:

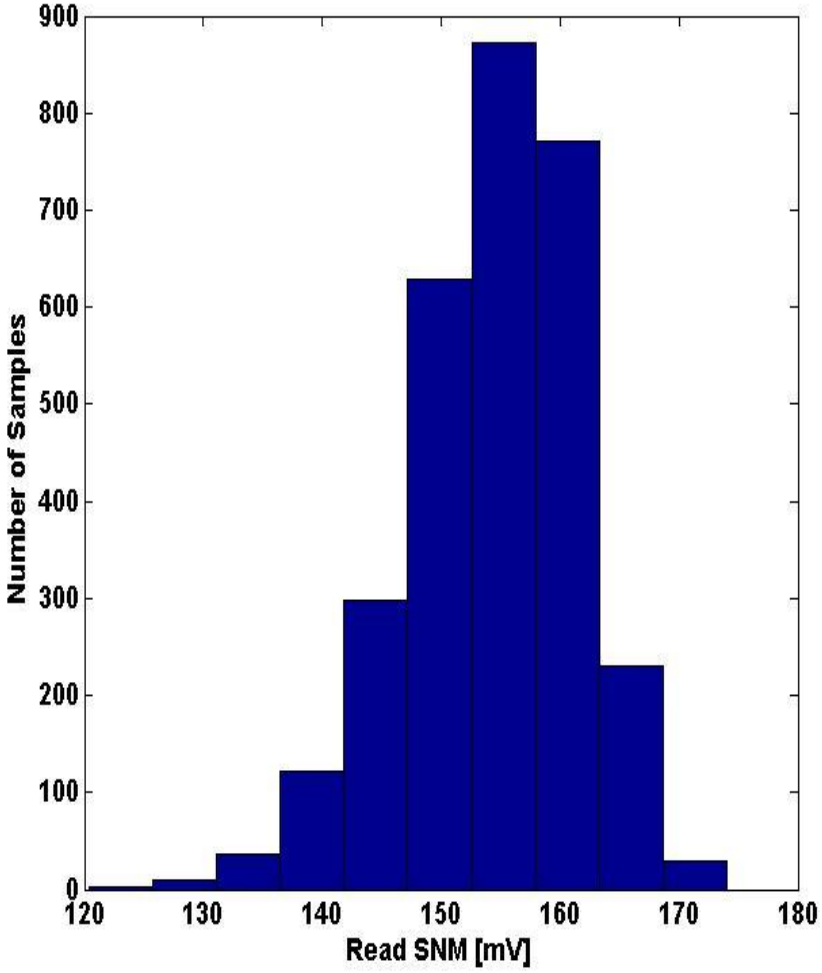
  VDD =0.9V, V_{TH0}=0.63V, V_{TH0n} = - 0.58V, T_{OXP} =1.3nm and T=110 ^{o}c

Read SNM Curve

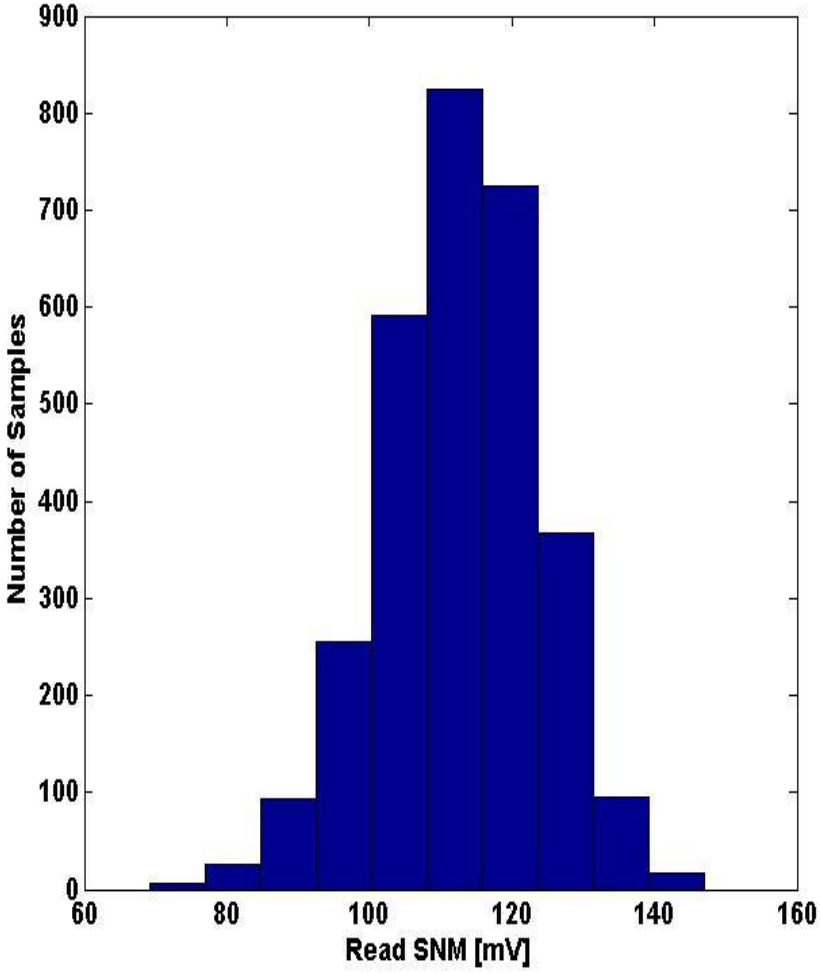


Read SNM Distribution: V_{DD}=0.9V

Fig 1 9T SRAM

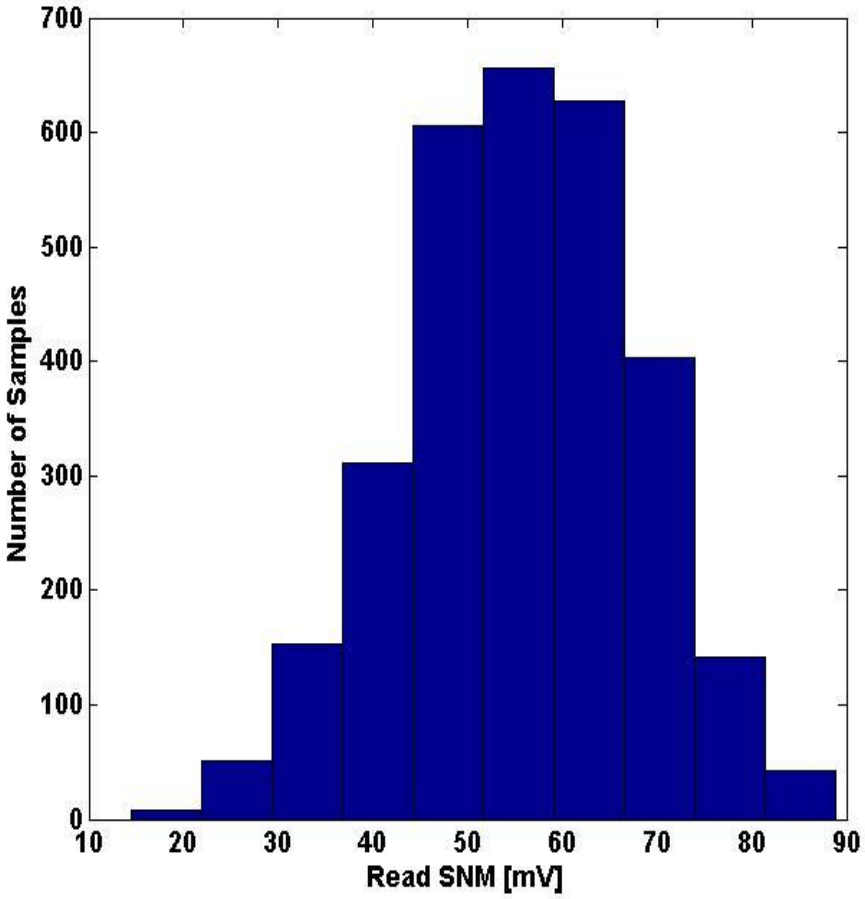


6T SRAM **Fig 2**

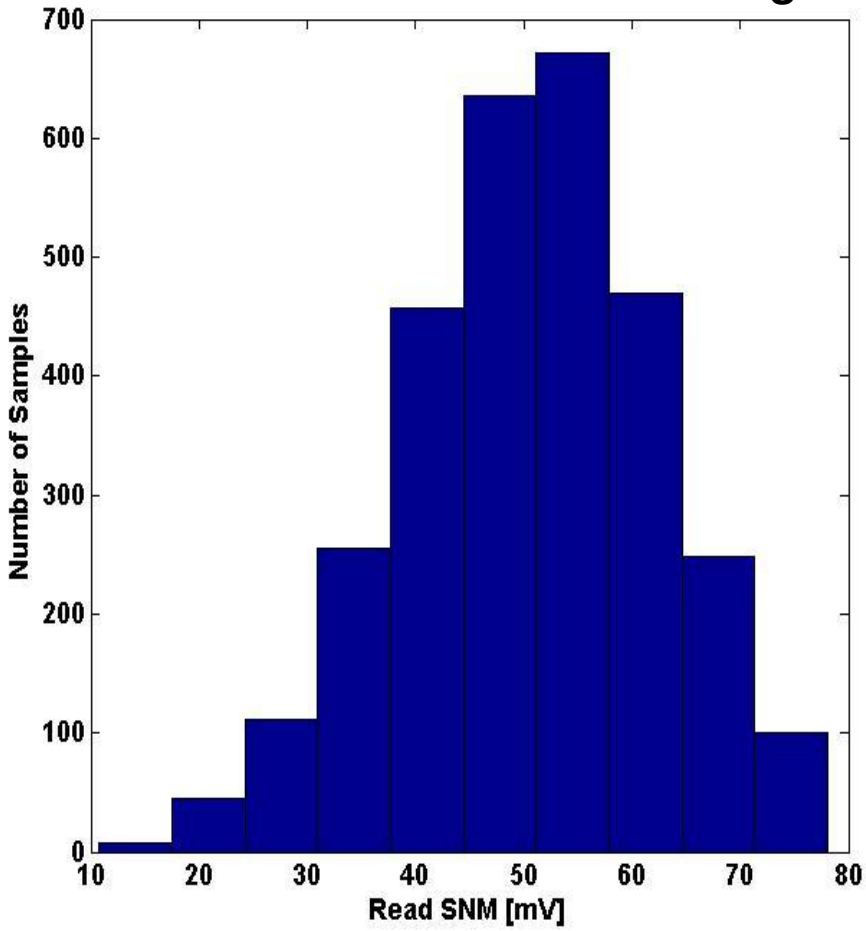


Read SNM Distribution: V_{DD}=0.4V

Fig 3 9T SRAM



6T SRAM **Fig 4**



Read SNM Distribution: Discussions …

- Fig. 1 and 2 show the distribution of read SNM of the proposed 9T and standard 6T SRAM bitcells, respectively, for V_{DD} = 0.9V . The mean value (μ) of read SNM of the proposed design is 37% higher than the standard 6T SRAM bitcell (i.e. 155mV against 113mV). The standard deviation in the proposed design is about 54% less as compared to standard 6T SRAM bitcell (i.e. 7.19mV against 11.03mV).
- **Therefore, the proposed design has better read SNM and process variation tolerance as compared to standard 6T SRAM bitcell.**

Read SNM Distribution: Discussions

- The low voltage applicability of the proposed design is compared at V_{DD} = 0.4V . Fig. 3 and 4 show the distribution of read SNM of the proposed 9T and standard 6T SRAM bitcells, respectively. The mean value (μ) of read SNM of the proposed design is 23% higher than the standard 6T SRAM bitcell (i.e. 62.3mV against 50.6mV). The improvement in the read SNM at lower voltage is not as good as it was at higher V_{DD} , however, standard deviation in the read SNM of the both the design is of the same order.

Conclusion

- A differential read and write 9T SRAM bitcell is presented. The advantages of standard 6T such as differential read which provides lower read access time and lower power consumption during read operation are preserved.
- However, the conflicting read and write requirements with the increase in bitcell ratio increases the read SNM, while it deteriorates the write performance, is also addressed in this design. The conflicting read and write problem is addressed by providing a separate read wordline, however, proposed design departs from the read SNM free SRAM designs those employs the separate read and write ports.

THANK YOU

For any questions contact:
Jawar Singh (jawar@iiitdmj.ac.in)