Design and Modeling of a Continuous-Time Delta-Sigma Modulator for Biopotential Signal Acquisition: Simulink Vs Verilog-AMS Perspective

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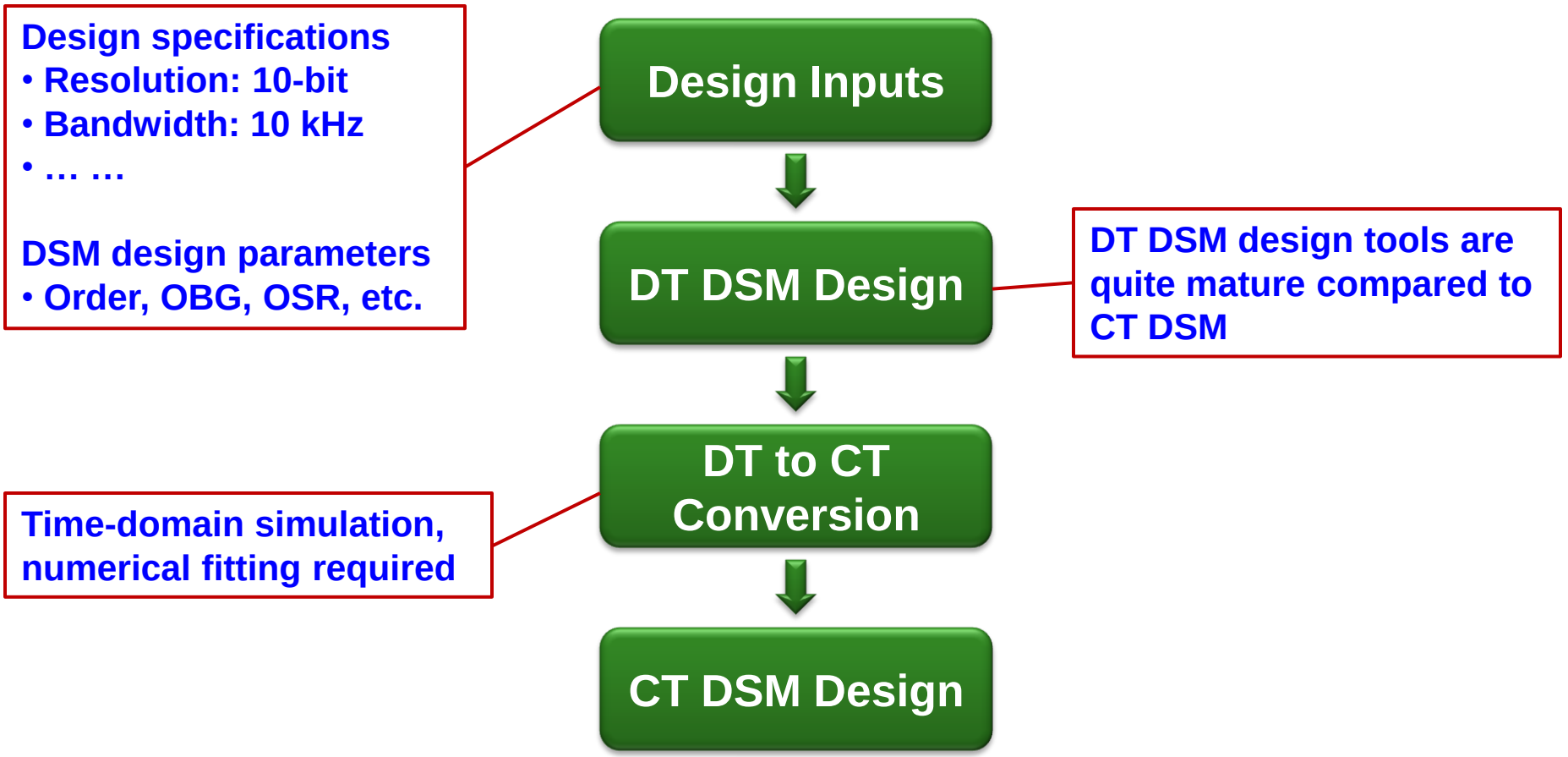
Agenda

- Motivation
- Continuous-time (CT) delta-sigma modulator (DSM) design overview
- Modeling tools and languages selection in each design step
- Conclusions

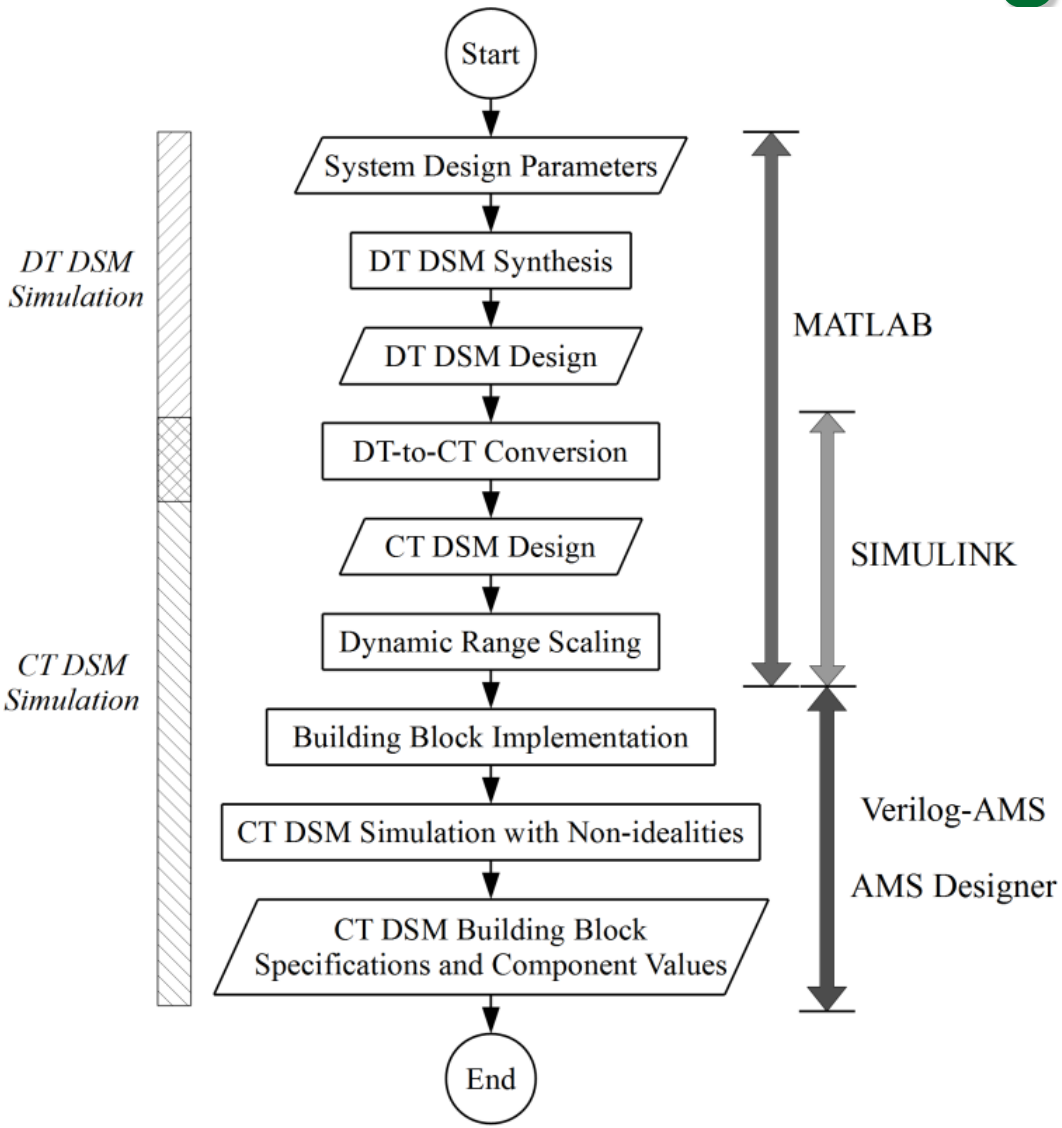
Motivation

- Analog and mixed-signal systems-on-a-Chip (AMS-SoC) are becoming more complex
- Simulating an entire AMS system with transistor-level netlists is infeasible
- Behavioral level simulations are crucial in AMS design and verification
- Simulink and Verilog-AMS are two well-known tools for behavioral modeling

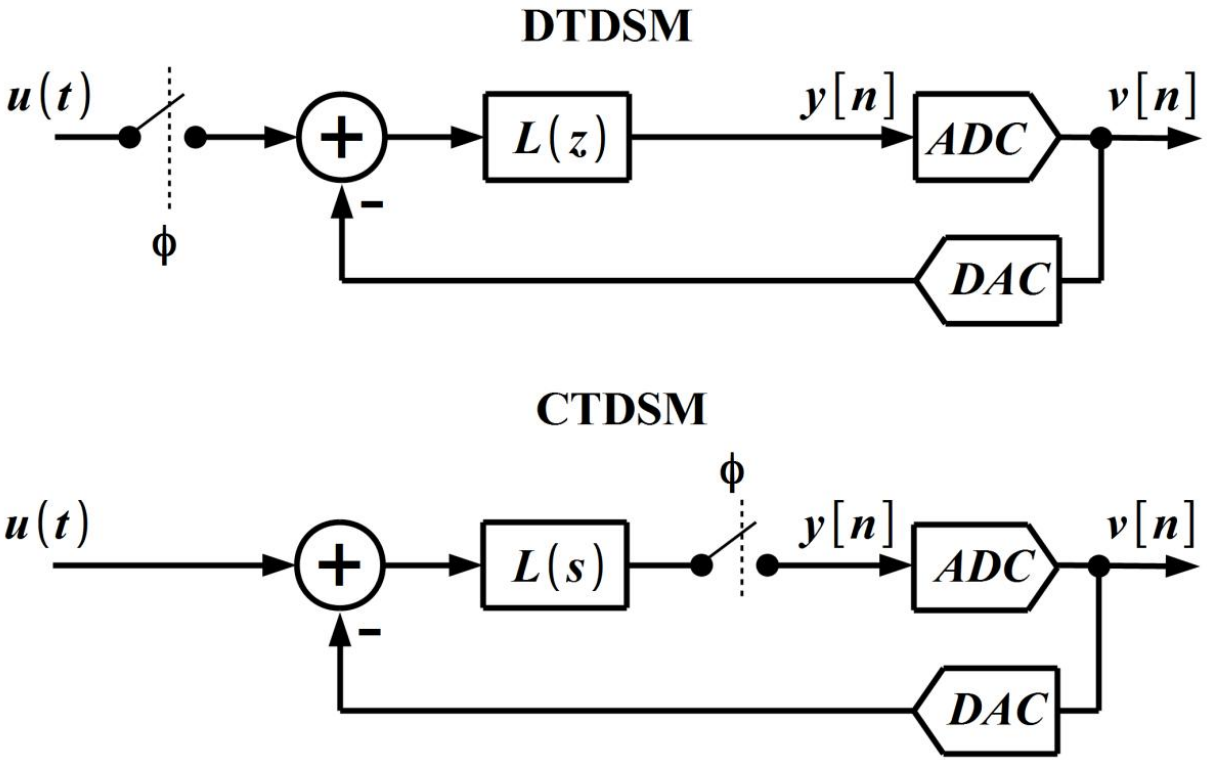
CT DSM Design Overview



System-Level CT DSM Design Flow



DSM Structures



Required components
- **Op amps**
- **Sampler/Quantizer**
- **… …**

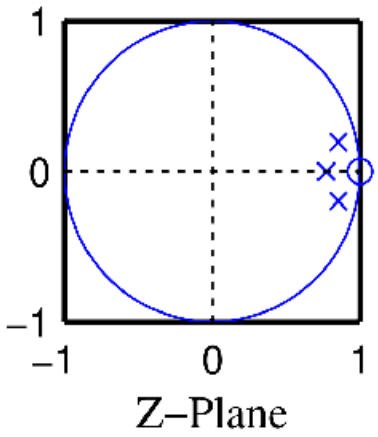
DT DSM Design Synthesis

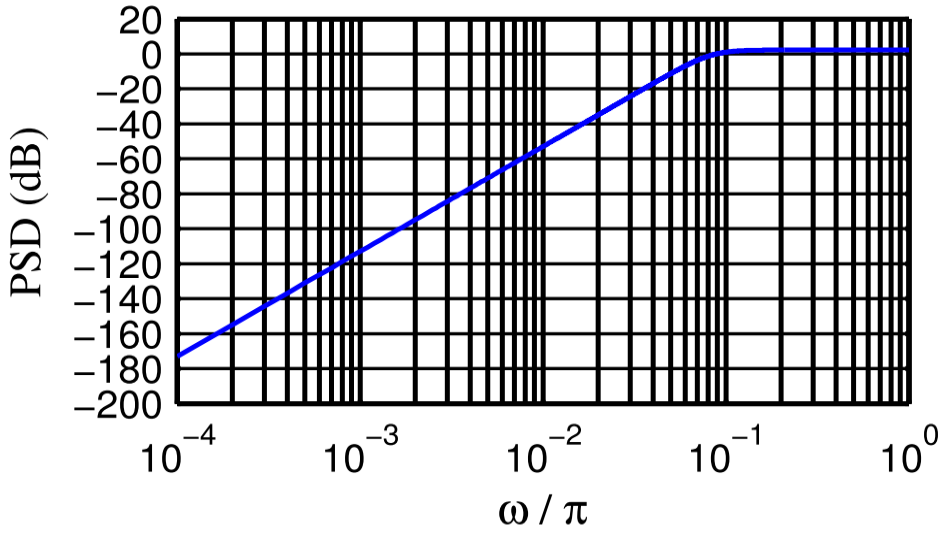
```
Order = 3;
OSR = 128;
nlev = 2;
OBG = 1.3;
f0 = 0;
opt = 0;
form = 'CIFF';
td = 0.2;
```

→ **MATLAB DSM Design Toolbox** →

$$L(z)=\frac{0.5217\left(z^2-1.756\,z+0.7826\right)}{(z-1)^3}$$

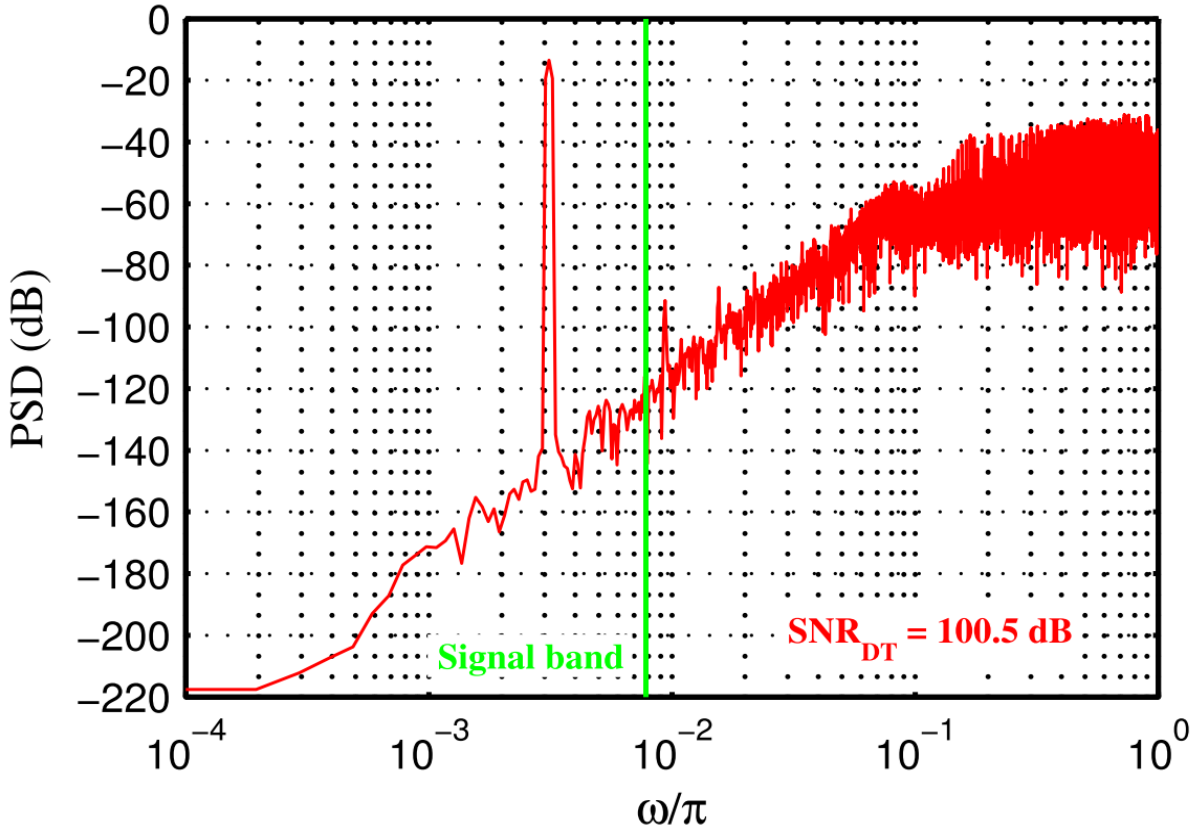
$$NTF(z)=\frac{1}{1+L(z)}$$



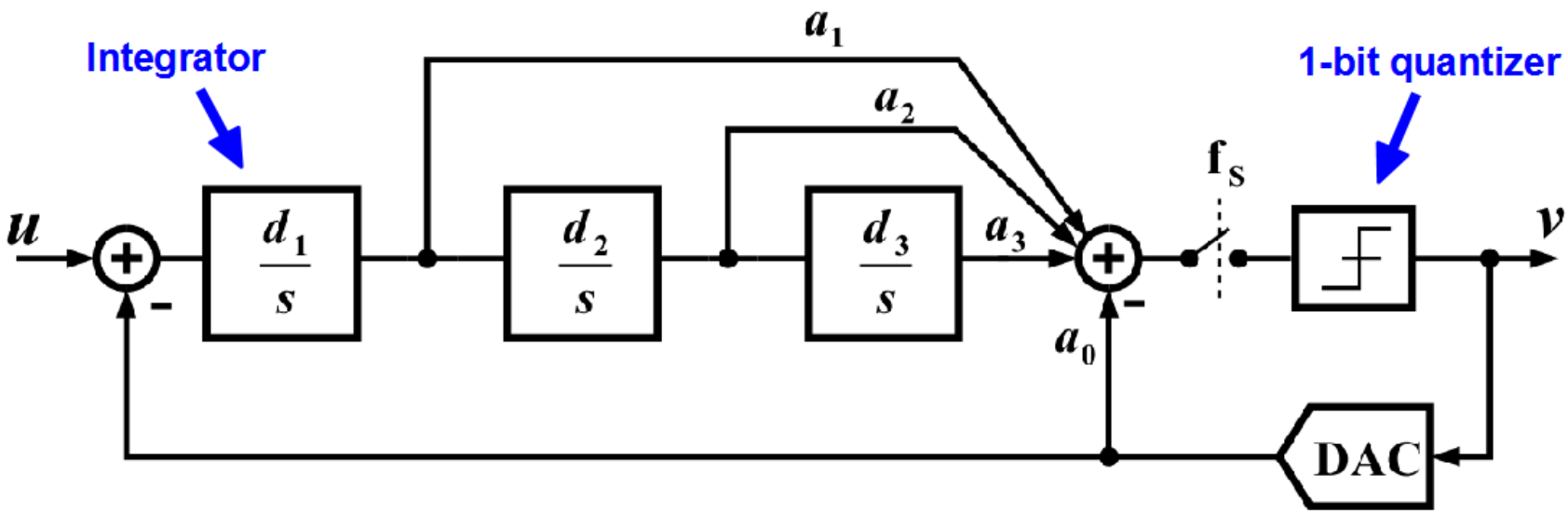


MATLAB DT DSM Simulation

- **MATLAB simulation shows that the DT DSM design satisfies the SNR requirement**



DT-to-CT Conversion

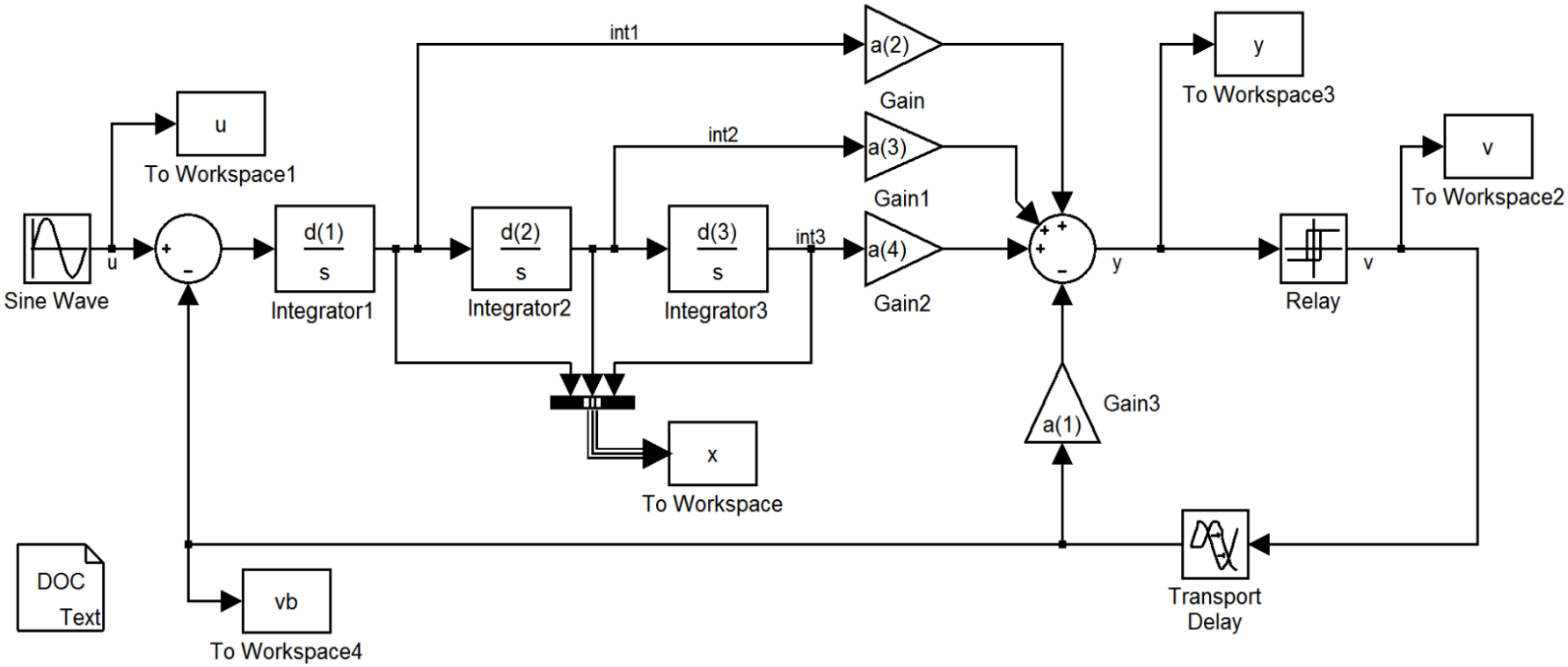


Find coefficients a0~a3 and d1~d3?

DT-to-CT Conversion

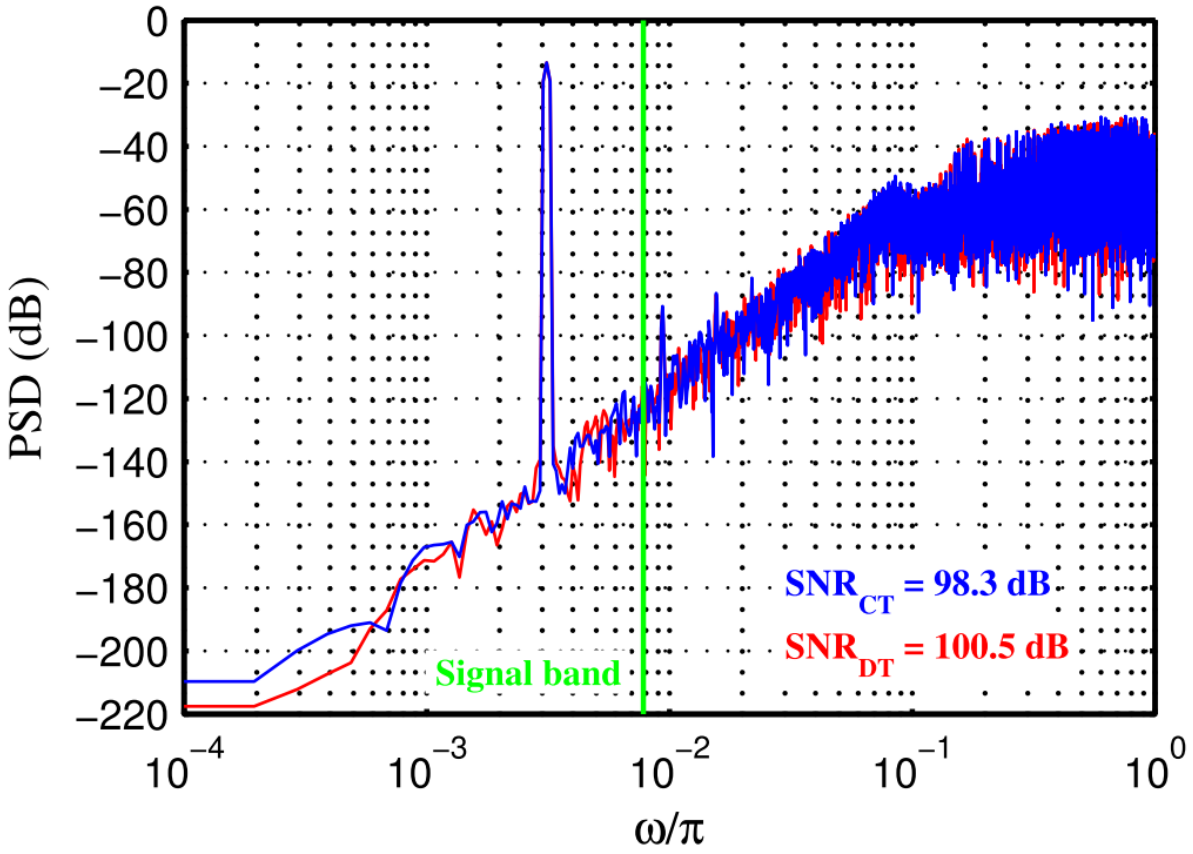
- **Finding the coefficients requires behavioral models, time-domain simulations, and numerical fitting**
- **Built-in libraries in SIMULINK provide a comprehensive collection of fundamental building blocks**
- **Writing codes and creating symbols for fundamental building blocks are necessary if Verilog-AMS is used**

SIMULINK CT DSM Model



SIMULINK CT DSM Simulation

- **The CT DSM simulation result is compared with the DT DSM result**



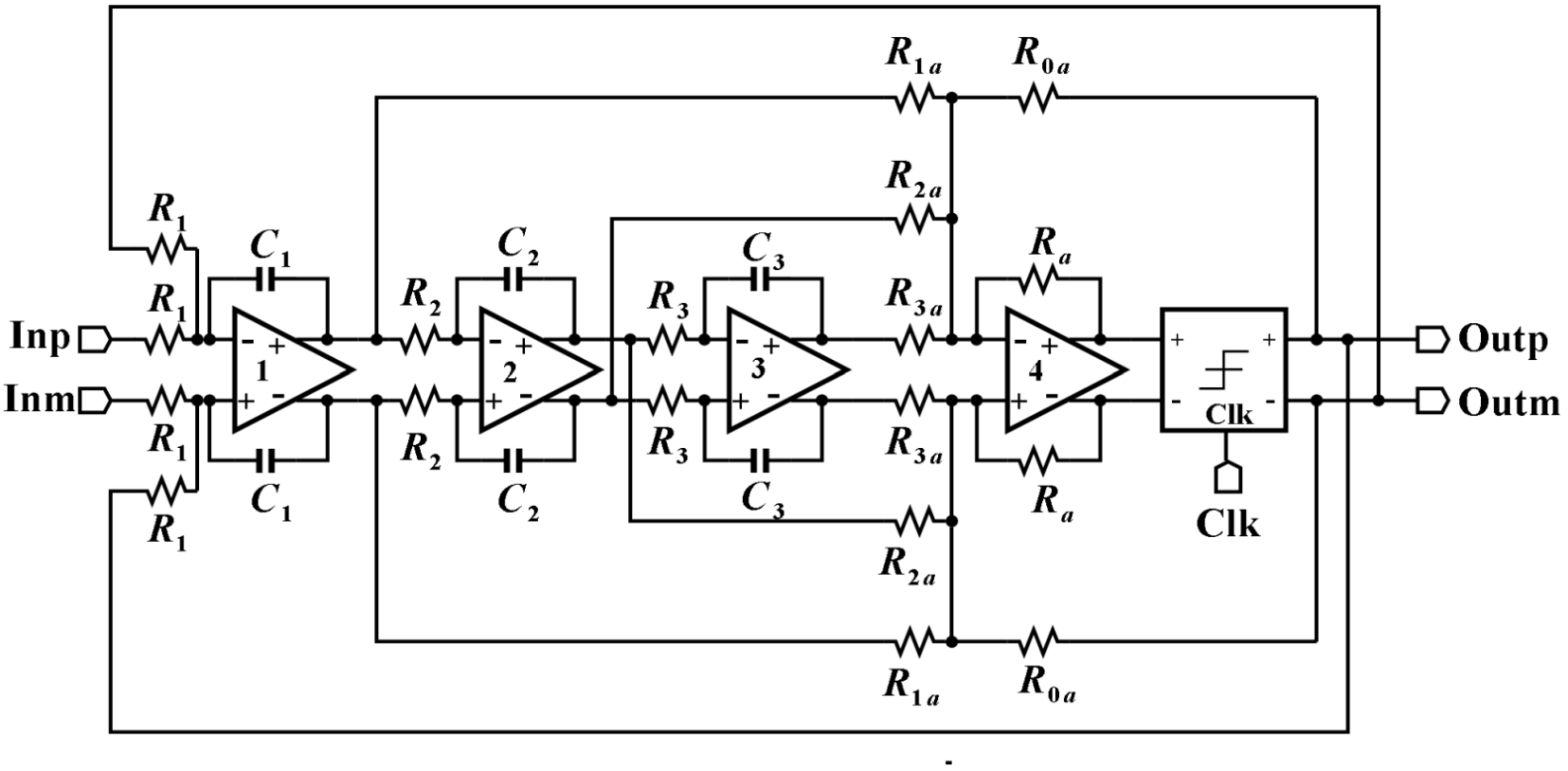
Building Block Implementation with Non-idealities

Two criteria when deciding the tool/language for this step:

- **The modeling language should be able to describe the non-idealities and allow them to be integrated into the ideal model without a great deal of time and effort**

- **The tool should allow the designer to switch each individual building block between ideal model, non-ideal model, and actual circuit implementation**

CT DSM Implementation



Two important non-idealities:

- **Finite Gain-Bandwidth Product (GBW)**
- **Clock Jitter**

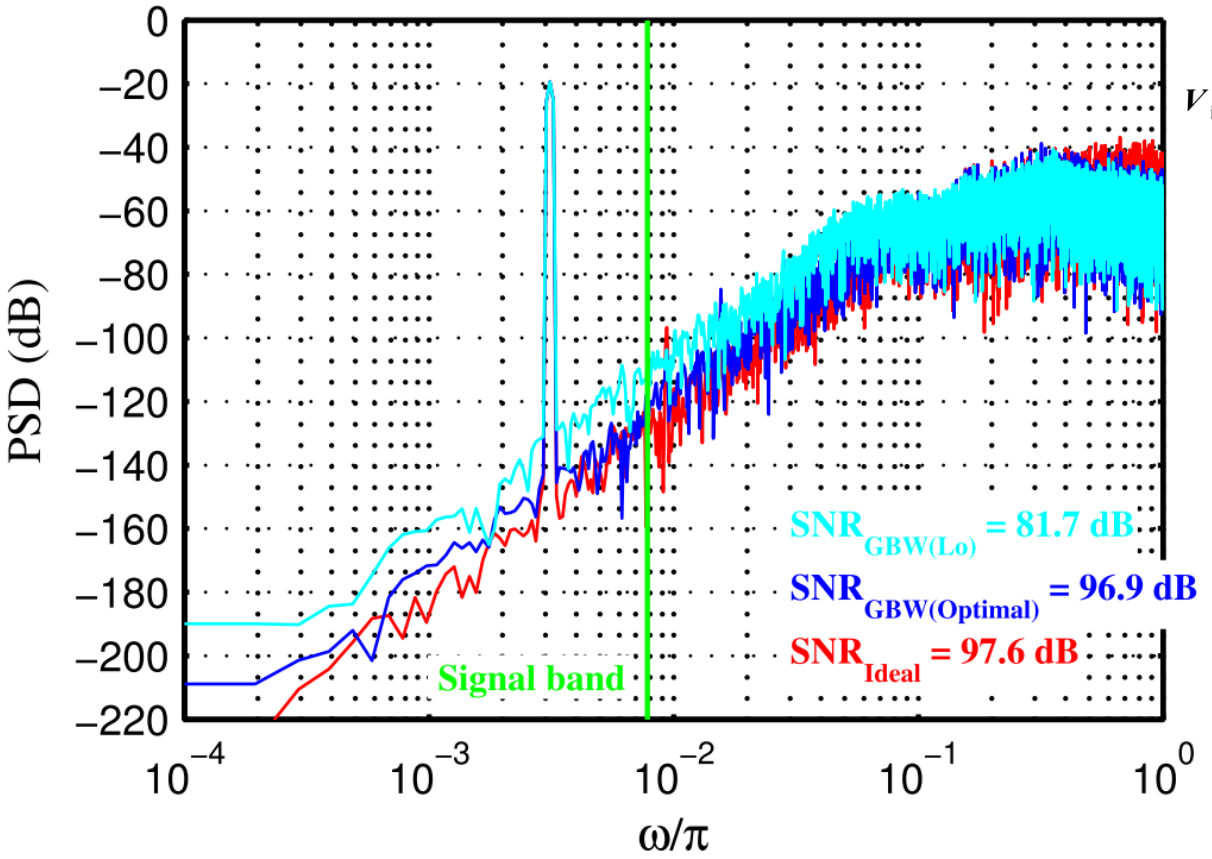
Modeling Non-idealities

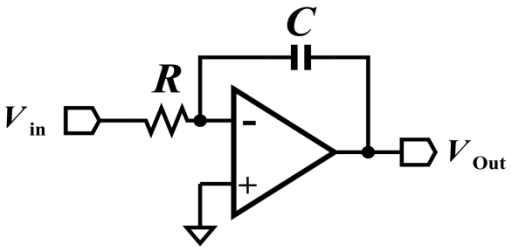
Verilog-AMS (AMS Designer) is chosen:

- **Actual circuit schematics and layouts are to be done in CADENCE**
- **SIMULINK requires extra effort for configuration on both sides, and the simulation procedure is not as convenient**
- **Modeling clock jitter in Verilog-AMS is relatively easier**

Finite GBW

V(outd) <+ laplace_nd((V(inp, inm) - V(fbp, fbm)), {-1}, d);

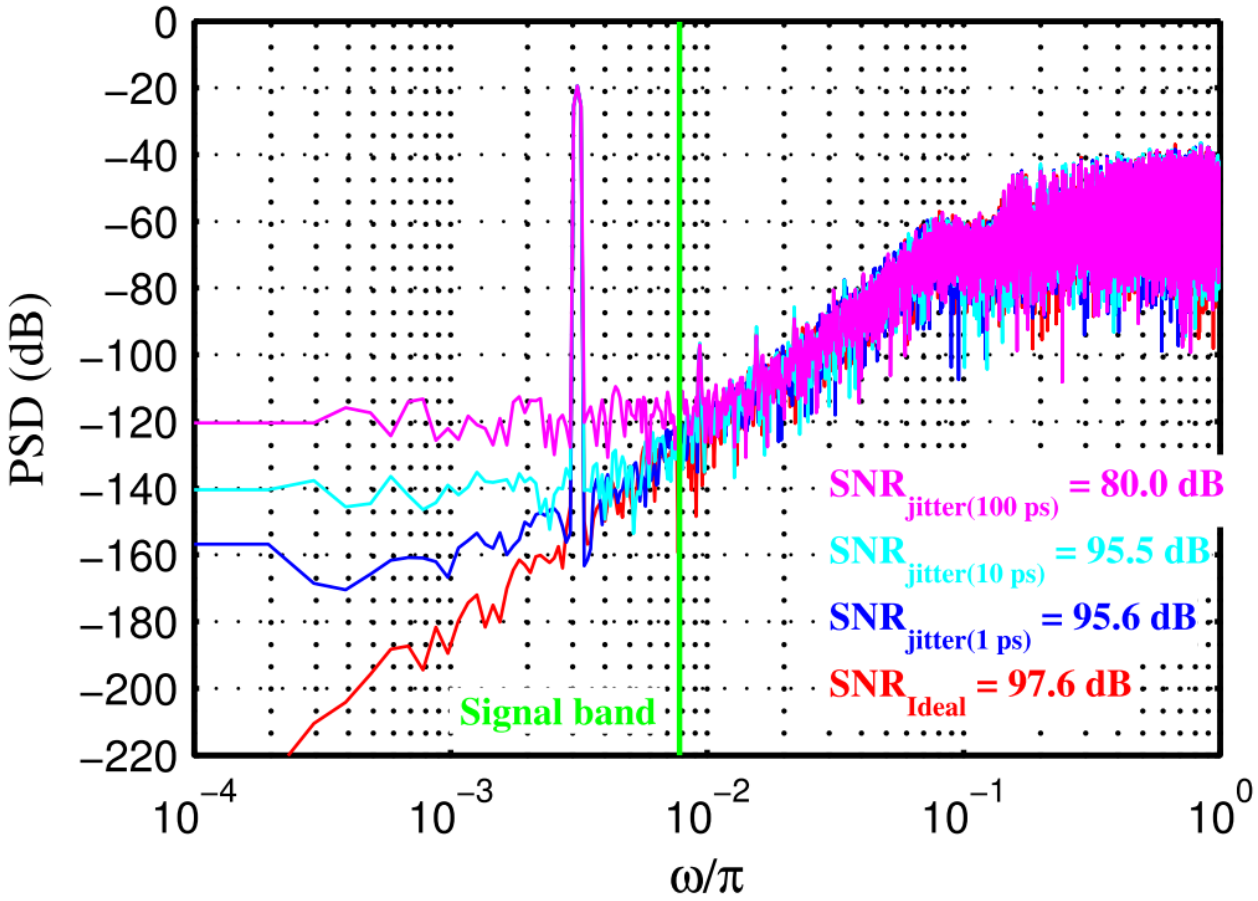




Clock Jitter

Function $rdist_normal for RMS jitter:

- **1 ps, 10 ps, and 100ps**



Simulator Settings

Accuracy vs Speed

- **Start with conservative settings to find out the theoretical limit and then gradually increase the tolerance to get a good tradeoff**

Simulator	Settings
Simulink	Analog Solver: ode23s Relative tolerance: 1×10^{-6} Absolute tolerance: 1×10^{-5} Max step size: 1×10^{-2}
AMS Designer	Analog Solver: Spectre Relative tolerance: 1×10^{-3} Voltage Absolute tolerance: 1×10^{-6} Current Absolute tolerance: 1×10^{-12}

Conclusions

- A CT DSM design flow along with modeling tools and languages for each step has been presented
- The choice of modeling tools and languauges depends on the objective, design cycle time, and budget

Questions?

Thank You!!!