A 2-Port 6T SRAM Bitcell Design with Multi-Port Capabilities at Reduced Area Overhead

Jawar Singh, Dilip S. Aswar[1], Saraju P. Mohanty[2] and Dhiraj K. Pradhan
Department of Computer Science, University of Bristol, UK.
Department of Telecommunication, Government of India, New Delhi.[1]
Dept. of Computer Science and Engineering, University of North Texas, USA.[2]
Email-ID: jawar@cs.bris.ac.uk, saraju.mohanty@unt.edu

Presented By:
Garima Thakral
University of North Texas

Acknowledgments: Jawar Singh acknowledges support from the Government of India, grant no. 11015/12/2005/SCD-V and Saraju P. Mohanty acknowledges partial support from NSF award CNS-0854182.

Outline of the Talk

- Introduction
- Comparison of dual-port bitcells
- The proposed dual-port bitcell
- Word array organization of the proposed bitcell
- Read/Write operation of proposed 2-port 6T SRAM
- Experimental Results
- Conclusions

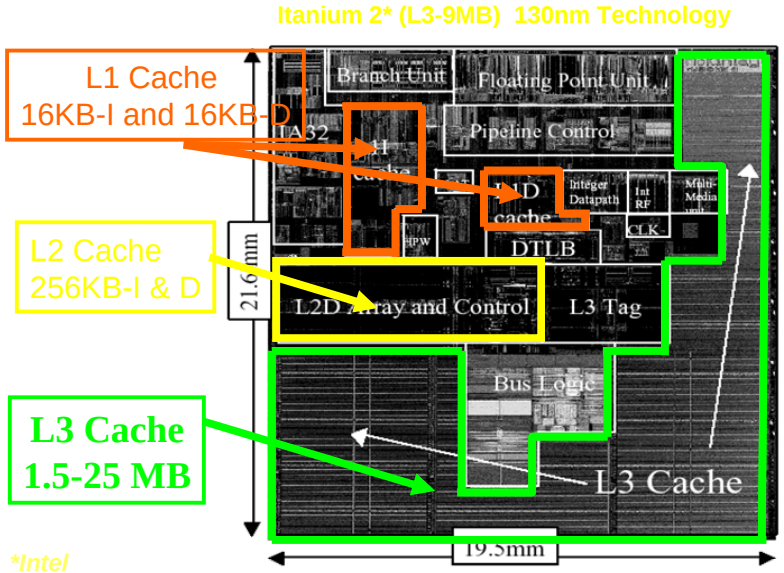
Introduction

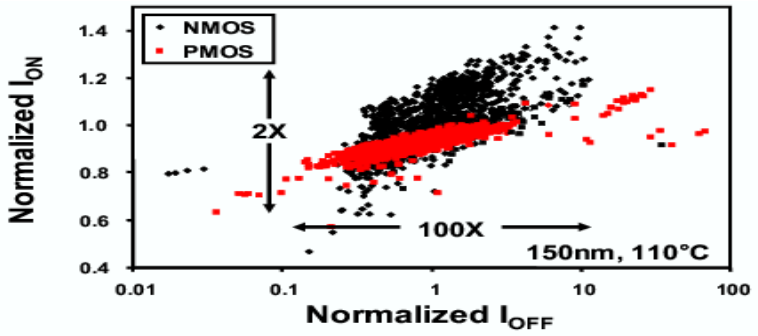
- The memory subsystem is a major part of any consumer electronic appliance designed as embedded system using system-on-a-chip (SoC) technology.
- In several applications, the embedded **Static Random Access Memory** (SRAMs) can occupy the majority of the chip area and contain hundreds of millions of transistors.

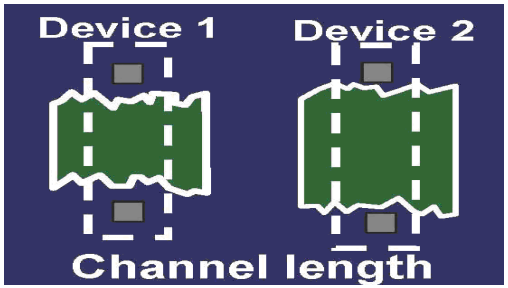
  In January 2010, a leading edge IC contained approximately 2 billion transistors.
- As the process technology continues to scale deeper into the nanometer region, the stability of embedded SRAM cells is a growing concern.
- Thus there is a popular demand for simultaneous or parallel read/write (R/W) access multi-port SRAM bitcells are widely employed in such embedded systems.

Motivation For SRAM Research

- Modern microprocessor and SoC products are memory intensive
  - Up 70% of die area is occupied by cache
  - To meet performance and throughput requirements
- Moore's Law driven CMOS scaling
  - Device variability
  - Reduced Ion/Ioff ratio
  - Exponential increase in leakage

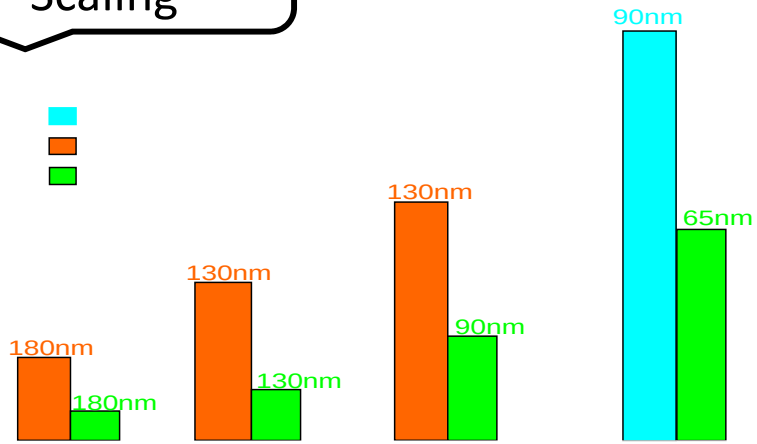


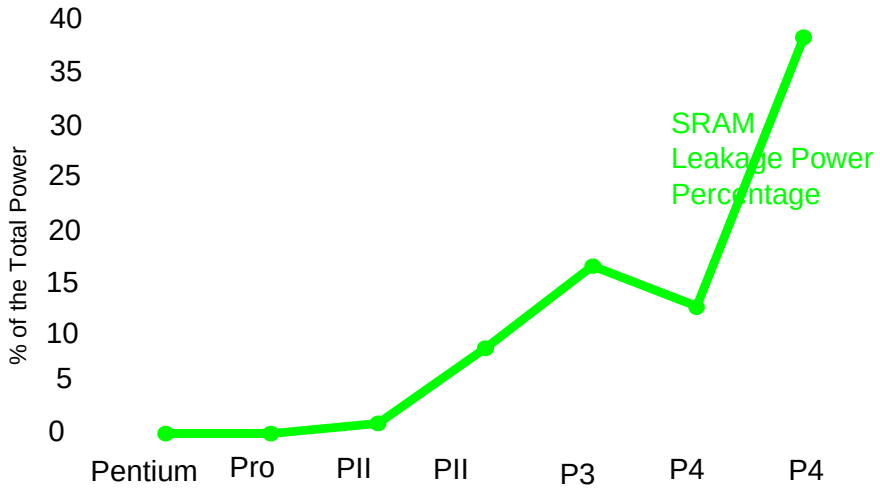




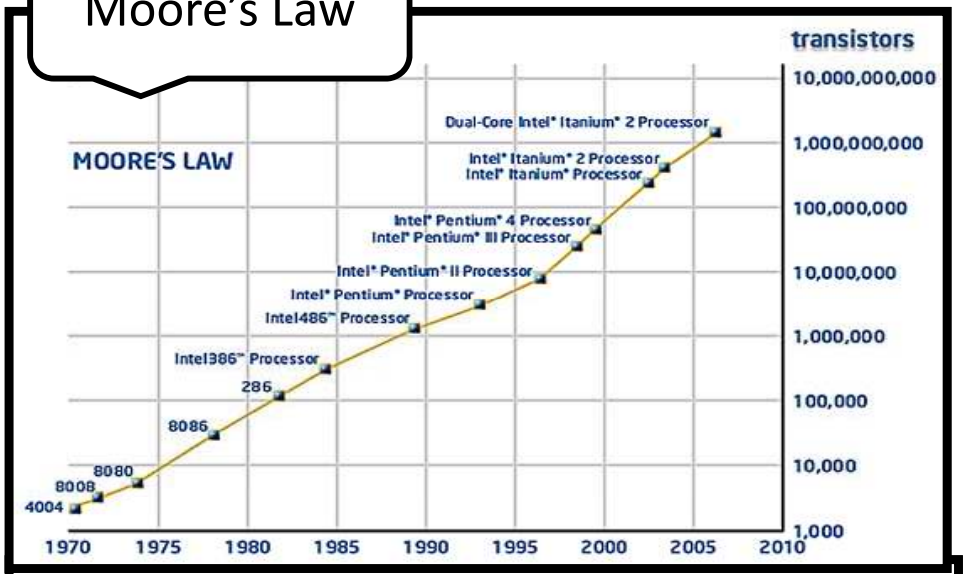
Scaling and Challenges: A Glimpse

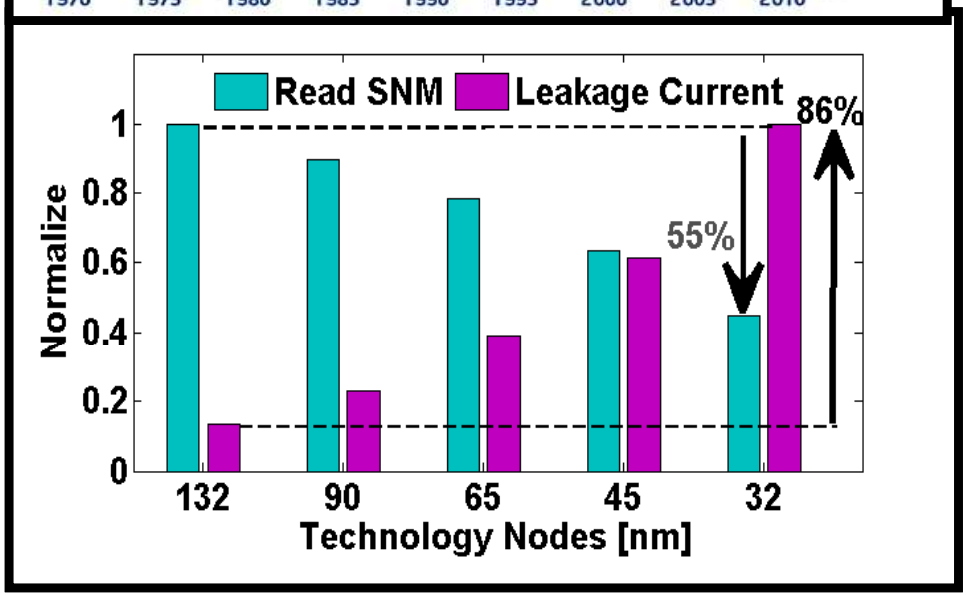
Technology Scaling





Moore's Law

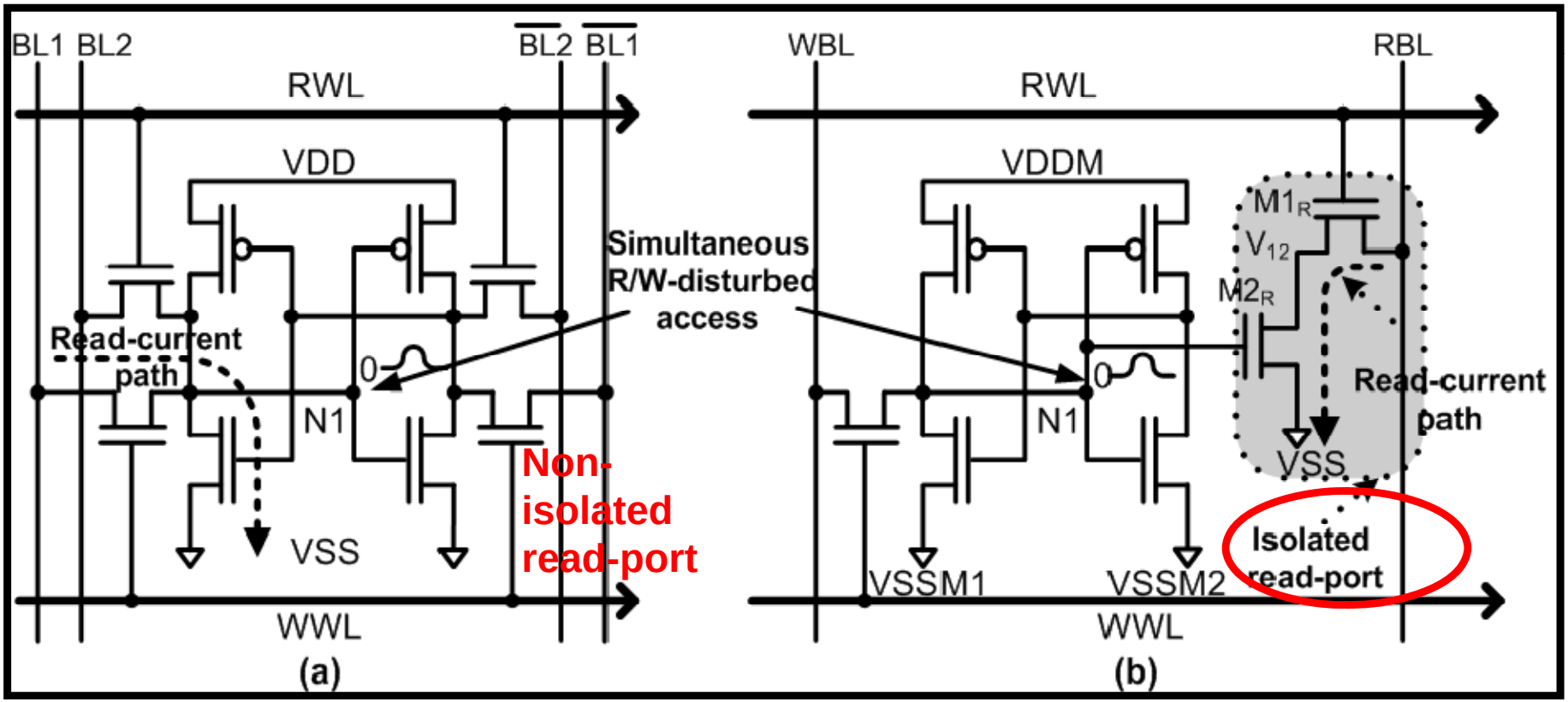




Contributions of This Paper

- A new 2-port 6T SRAM and its word-oriented array organization is proposed to eliminate read and write access disturbances due to column select functionality in neighboring cells or words.
- The poor read-noise margin and conflicting read-write problems are handled by isolating the read and write-ports to achieve higher stability.
- The proposed bitcell has a sufficiently large static noise margin (SNM), write ability margin (WAM) and read-current I_{read} which takes care of the tremendous parametric yield loss.
- The process variation sensitivity analysis shows that the proposed design has significantly low process variation sensitivity as compared to existing ones, hence a better parametric yield.

Dual-Port SRAM Bitcells



(a) Standard 8T SRAM

-non-isolated read port

-simultaneous read and write disturbance

-poor read SNM

- conflicting read and write requirements

(b) Single-ended 7T SRAM

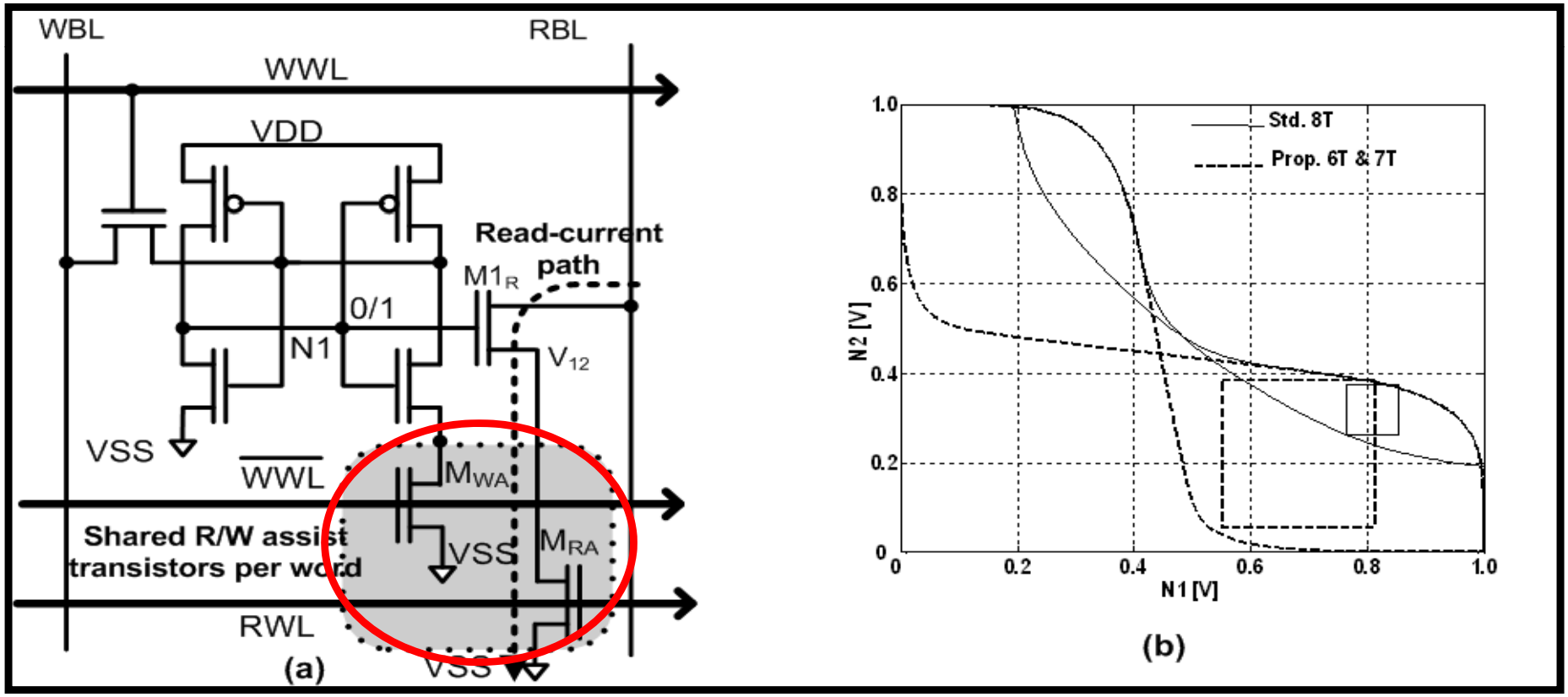
-isolated read port

-simultaneous read and write disturbance

-good read SNM

-differential biasing rail requirements

The Proposed Dual-Port Bitcell



Single-ended 6T SRAM: Advantages

-isolated read port

-good read SNM

-less number of devices with minimum size

-differential biasing rail requirements

-no simultaneous read/write disturbance

-no-conflicting read/write requirements

-no differential biasing rail requirements

-only shared read and write transistors per word needed

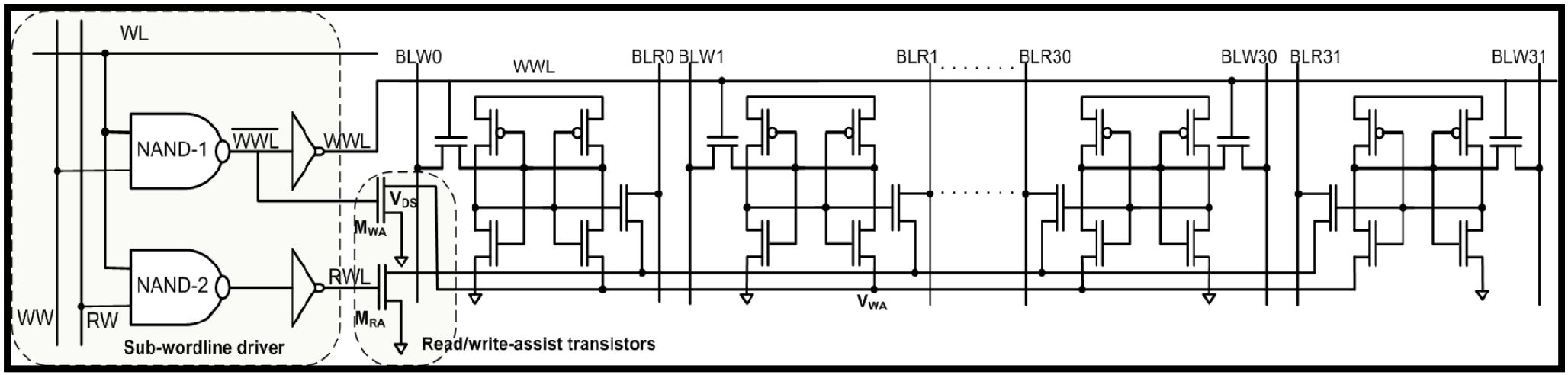
Unique Features of Proposed Bitcell

• The read bitline (RBL) is isolated with a single transistor while another (read-assist, MRA) transistor is shared among all the bitcells in a word. This arrangement provides a SNM-free read operation and a more area efficient bitcell.

• A write assist transistor (MWA) is used, shared per word, to advance the WAM or to achieve a strong write-ability margin.

• A non-interleaved array organization to facilitate the sharing of MRA, MWA and sub-wordline drivers, for eliminating the column select functionality within the array. This helps in achieving both the SNM-free read operation and strong write-ability margin simultaneously, while eliminating the simultaneous read/write disturbance problems.

Word-Organization of Proposed SRAM



A non-interleaved array organization:

- in order to share read and write assist transistors
- reduced array area overhead
- read and write assist transistors are shared per word to eliminate simultaneous read/write disturbance
- sizing of read assist transistor has direct impact of the array performance
- while a minimum sized write assist transistor to provide good write-ability and less leakage current

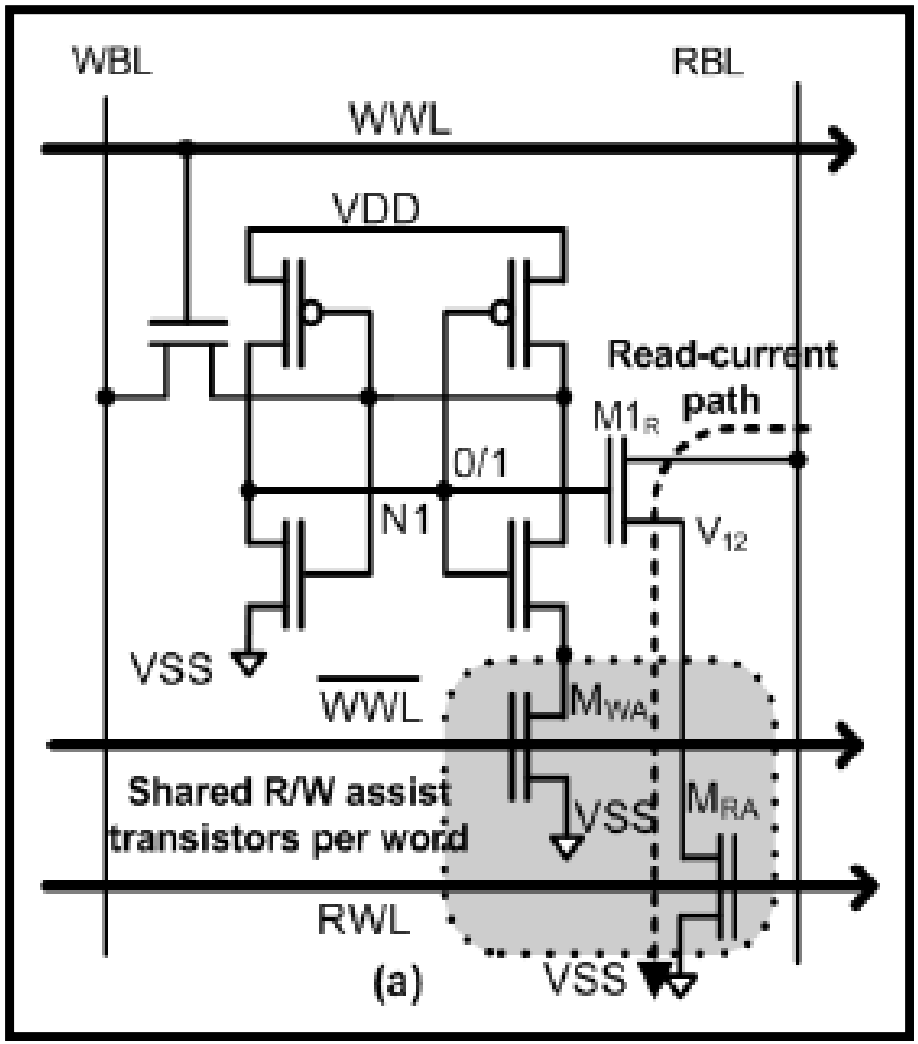
Read/Write Operations of Proposed SRAM

Read 0/1

- Carried out via a single ended bitline (data-line).
- reading '1' or '0', storage nodes are isolated from the read current path, hence, it significantly enhances the data stability during read cycle.

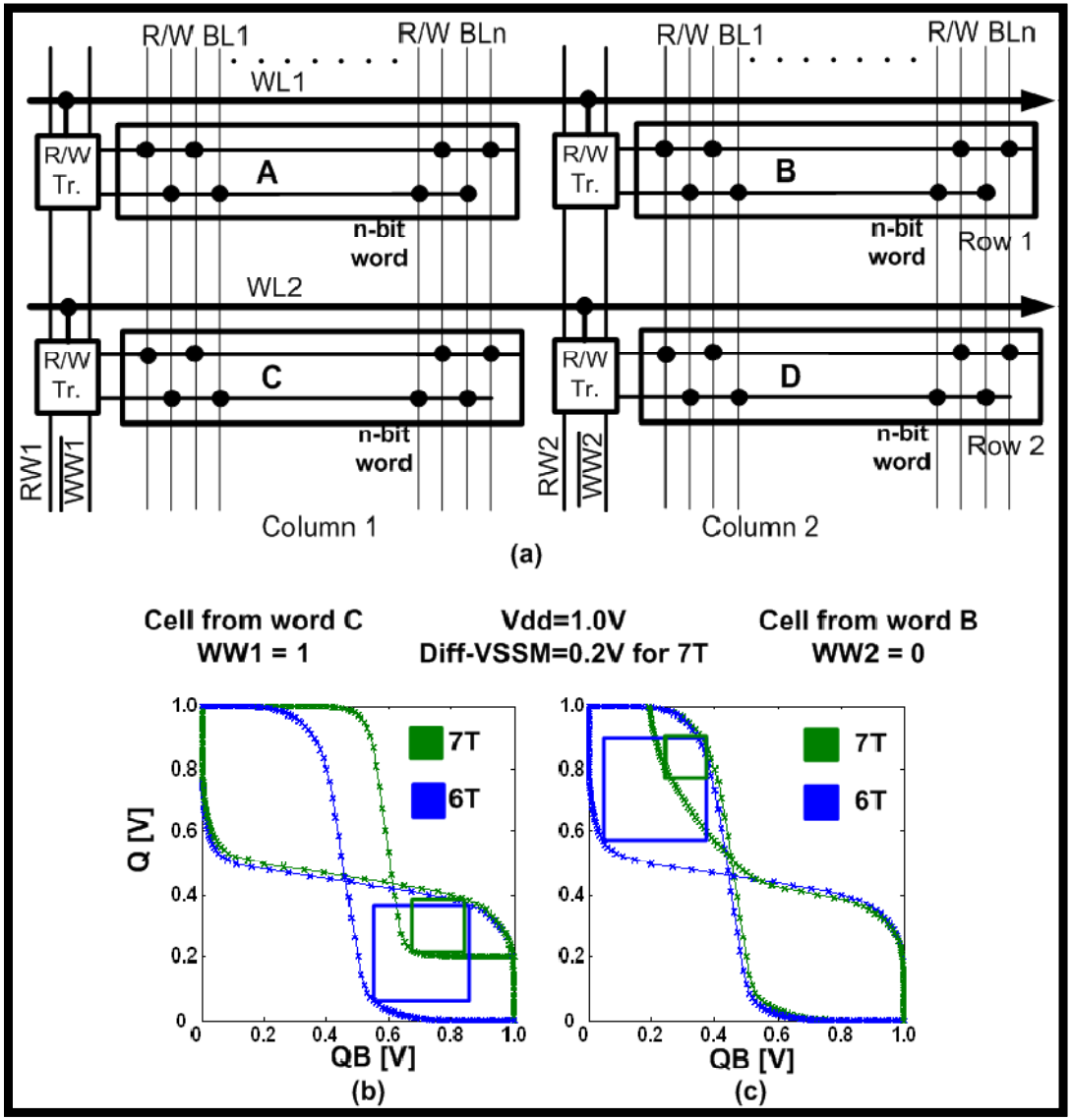
Write 0/1

- MWA is used to weaken the strongly cross coupled inverters. Hence, it enhances the write-ability, even at lower operating voltages effectively.



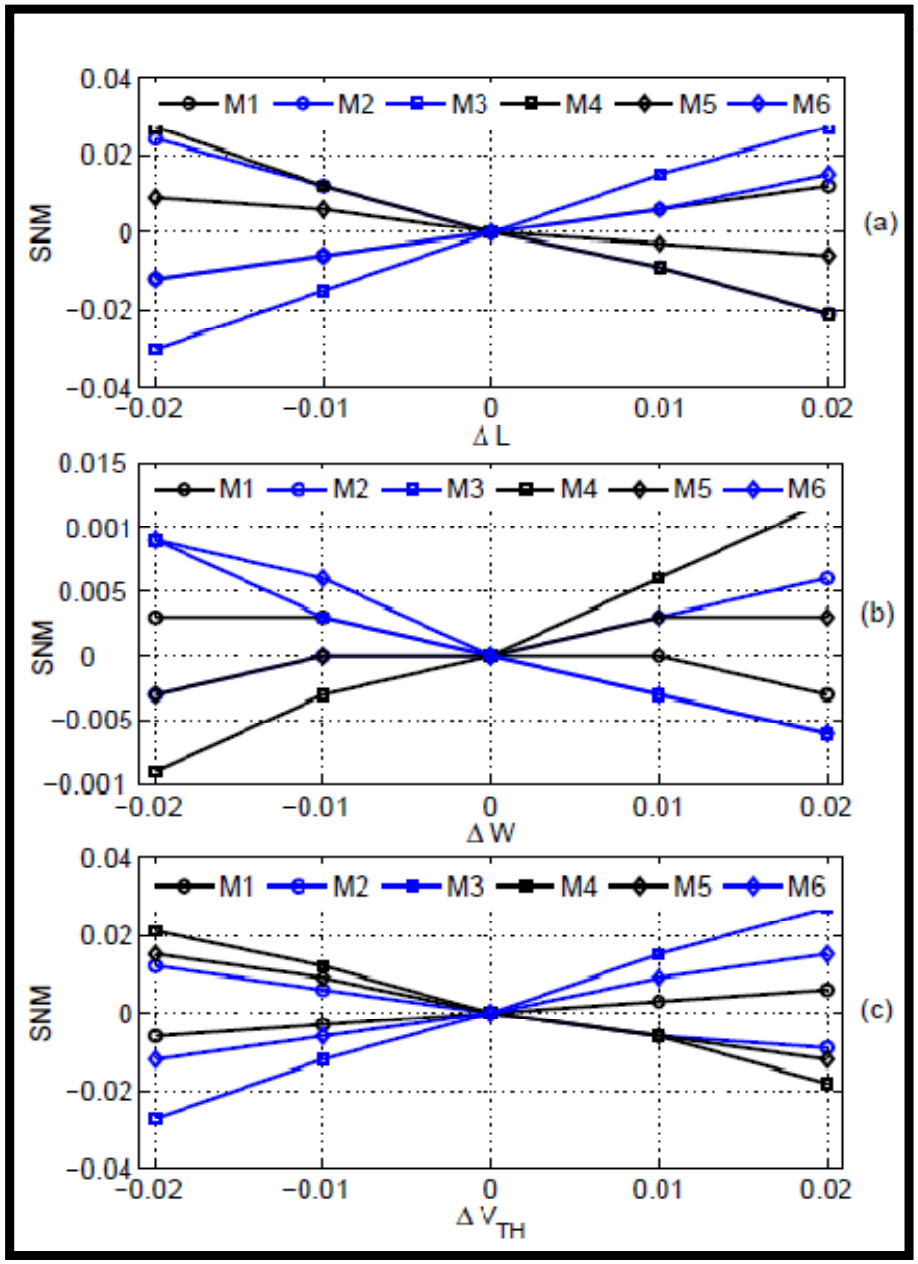
Simultaneous Read and Write Access

- Four 32-bit words to illustrate simultaneous read / write disturbance
  - read static noise margins are used as a metric
  - to read and write word A: bitcells in word C and B will get disturb
  - since word B and C share the same bit and word lines
  - while the use of separate read and write drivers avoid this disturbance, hence, proposed design has intact read SNM
  - while in 7T bitcell the read SNM is worst due to differential biasing.



Process Variation: Standard SRAM

- PV sensitivity is defined as a change in SNM with respect to change in device parameters.
- Read SNM of standard bitcell with variation in device parameters.
- Change in length and threshold voltage has huge impact on the read SNM as compared to change in width.
- Also the variation in pull down devices (M3 and M4) has sever impact on the SNM followed by the access devices (M5 and M6).



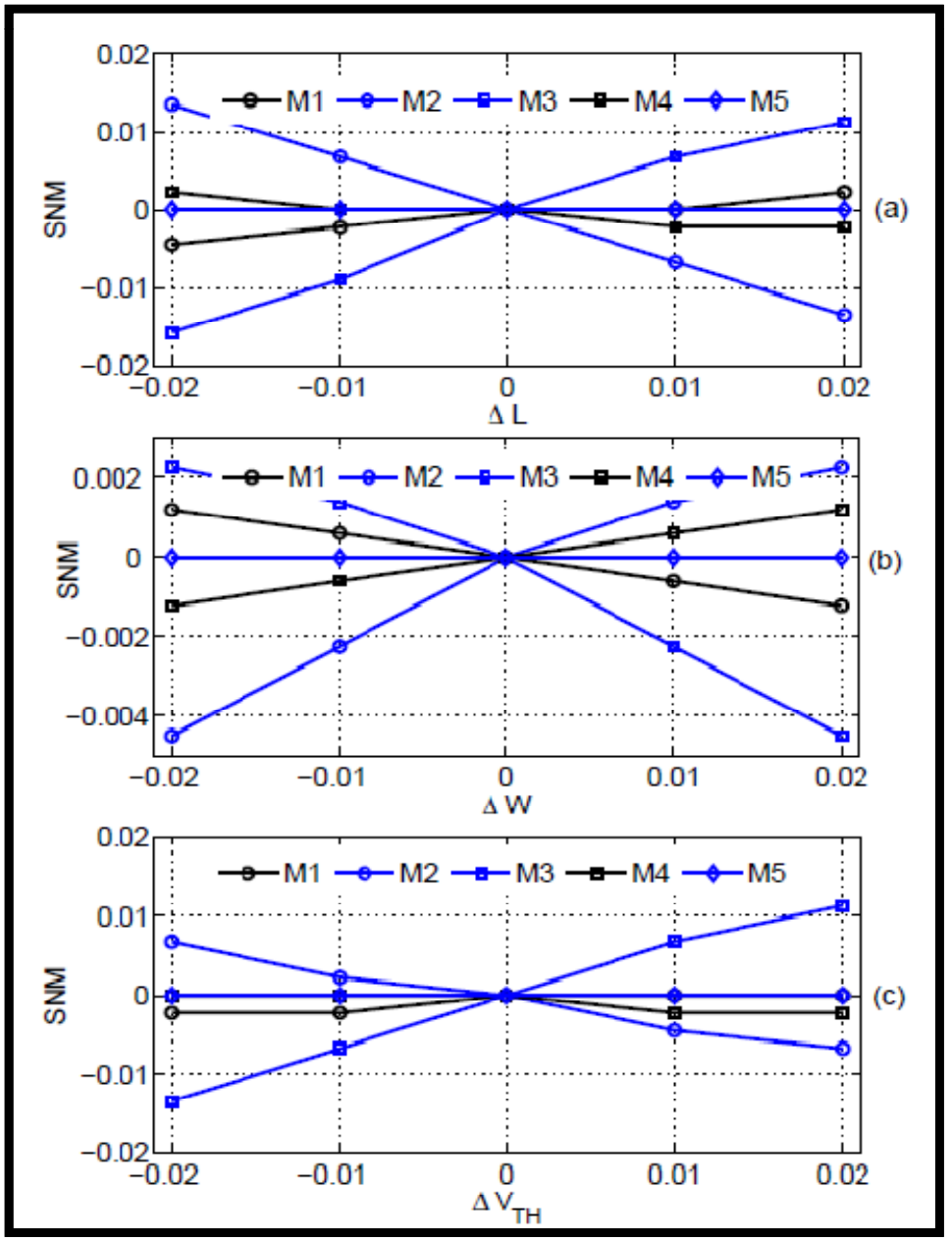
Process Variation : Proposed SRAM

- Read SNM of the proposed bitcell with variation in device parameters.

- Trends in variation in SNM is remain same such as length and threshold voltage degrades higher than the width.

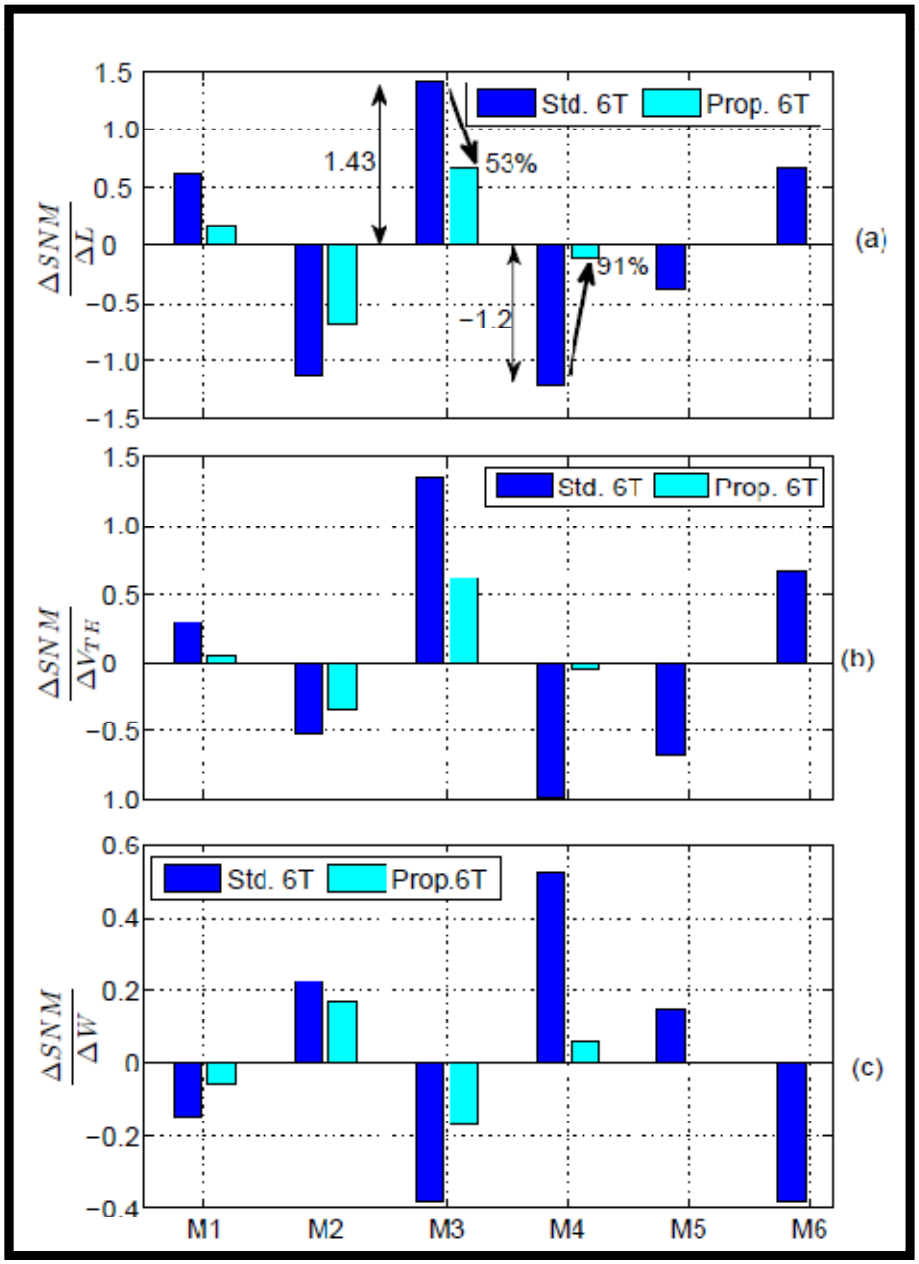
- While the overall variation in SNM is significantly less in all the cases as compared to standard bitcell.

- That is mainly due to isolation of read port.

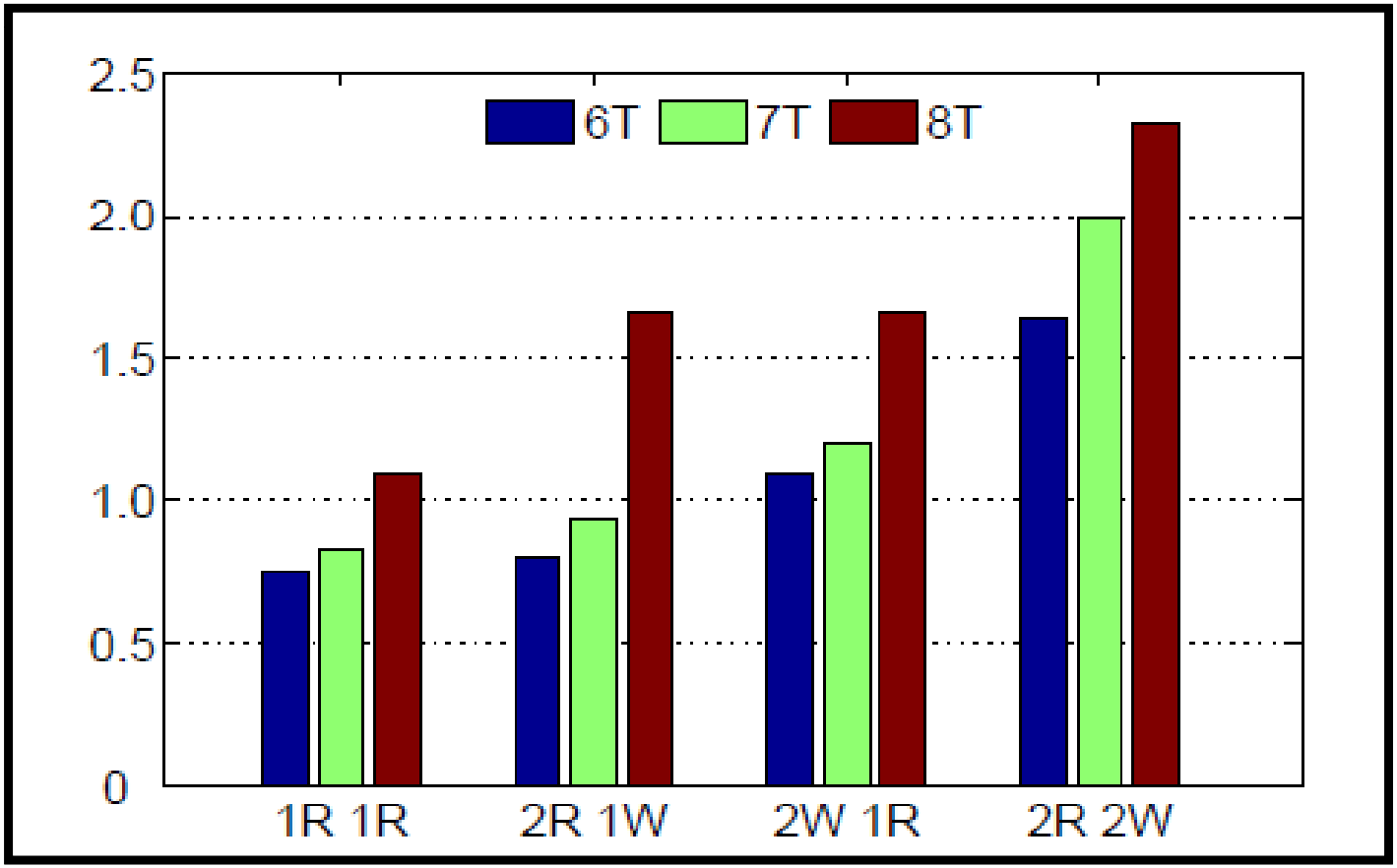


Process Variation : Comparison

- Bitcells' SNM is more sensitive to length and threshold voltage as compared to width.
- Bitcells' SNM is more sensitive pull down and access devices.
- The proposed bitcell SNM is less sensitivity as compared to standard bitcell.
- That is mainly due to pull down and access devices are not in read current path.



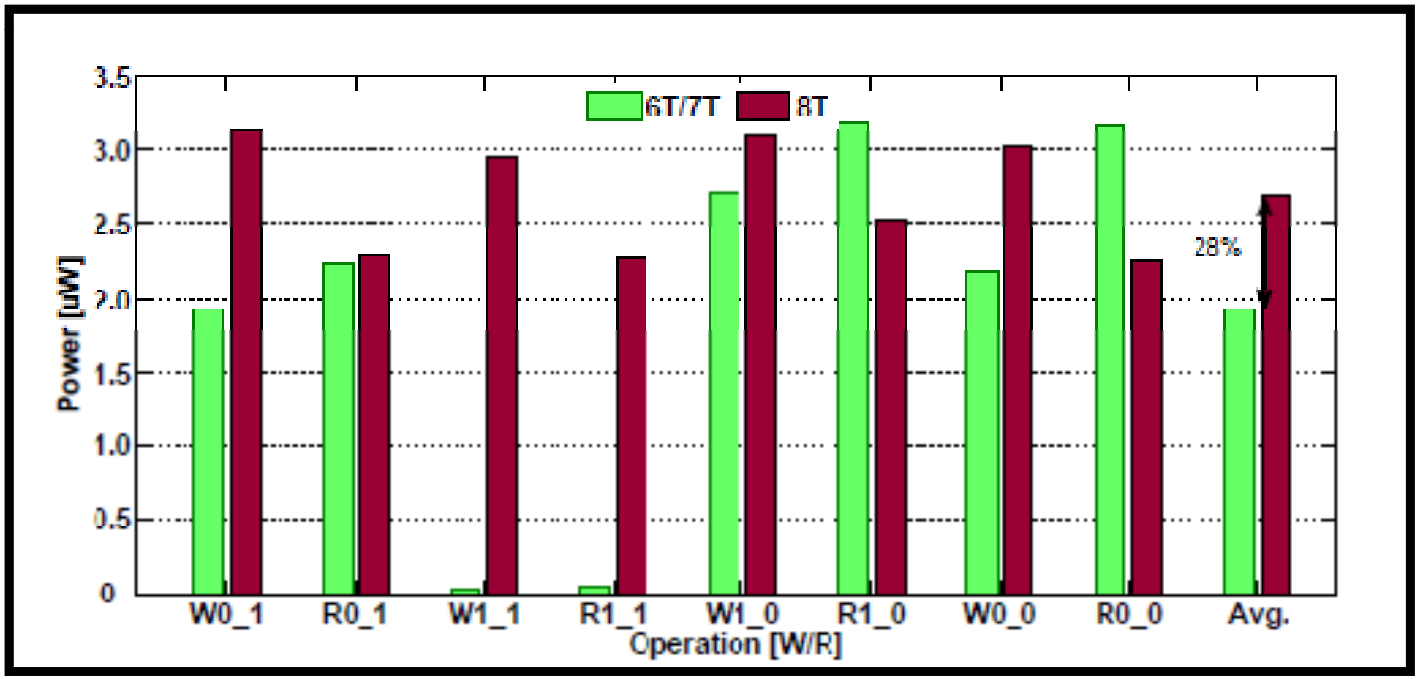
Area Comparison: 6T, 7T, and 8T



- Proposed bitcell has less area over head in order to have additional ports.

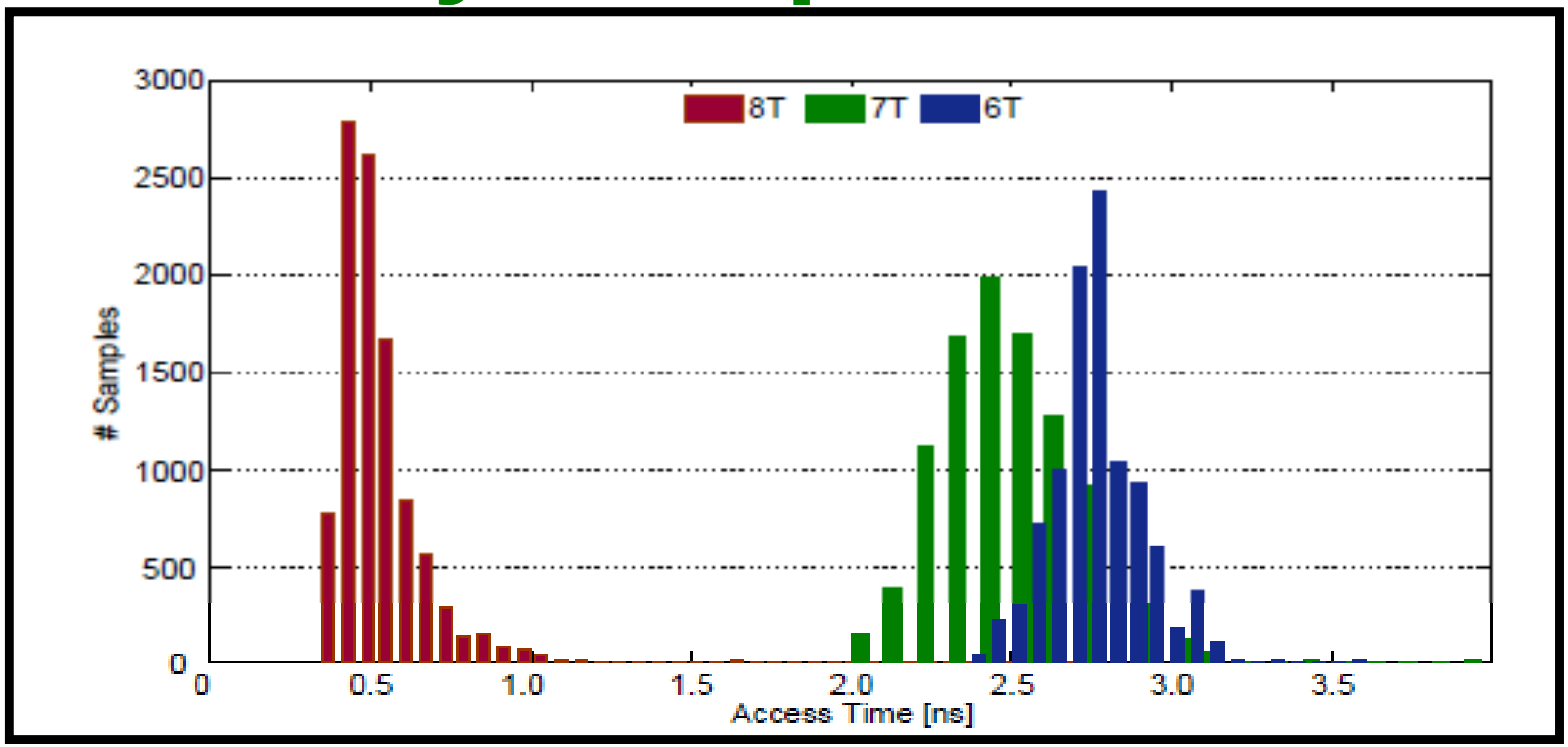
- While in the standard bitcell area overhead increases significantly in order to provide additional ports.

Active Power Comparison: 6T/7T/8T



- Average active power dissipation for different read and write operation in the proposed bitcell is 28% less as compared to standard bitcell.
- It is mainly due to single ended read or directly sensing the data without discharging the bitline.
- While 7T has almost equal power dissipation.

Read Delay Comparison: 6T/7T/8T



• Read delay of proposed bitcell in worst case is 3X higher as compared to standard bitcell while similar to 7T bitcell.

•It is mainly due to single ended read or directly sensing the data while in standard bitcell sense amplifier is used to sense the data.

Performance Comparison: 6T/7T/8T

- For the target applications such as video-processing, high read access multi-port SRAM is strongly recommended since the read operation occurs more repeatedly than the write operation in video codec.

- Read access time of the proposed 6T bitcell is 10% higher than that of the 7T bitcell because of the modified read-port or in other words, stacking phenomena in the read-port slow down the read performance of the 6T bitcell.

- Performance of the proposed 6T can be achieved equivalent to an 8T by optimizing the size of read-assist transistor, however, it may lead to an increase in area overhead.

Conclusions

- The major challenges of 2-port SRAM bitcells, such as poor data stability, read and write disturbances and simultaneous read and write conflicts have been addressed.
- The robustness, process sensitivity, area overhead, power and performance of the proposed bitcell are compared with existing 7T and 8T bitcells.
- The area overhead in the proposed bitcell for providing the multi-port capabilities such as additional read and write ports is lower than the 7T and 8T bitcells.
- Hence, the proposed design has significant potential for the multimedia and communication applications for nanoscale and other SoCs in terms of area and power dissipation.
- Furthermore, sensitivity to process variations and high stability margins make the proposed design more attractive in nano-regime.


Thank you !!!