

Layout-Aware Illinois Scan Design for High Fault Coverage

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Acknowledgment: This research is supported in part by EPSRC grant EP/G032904/1.

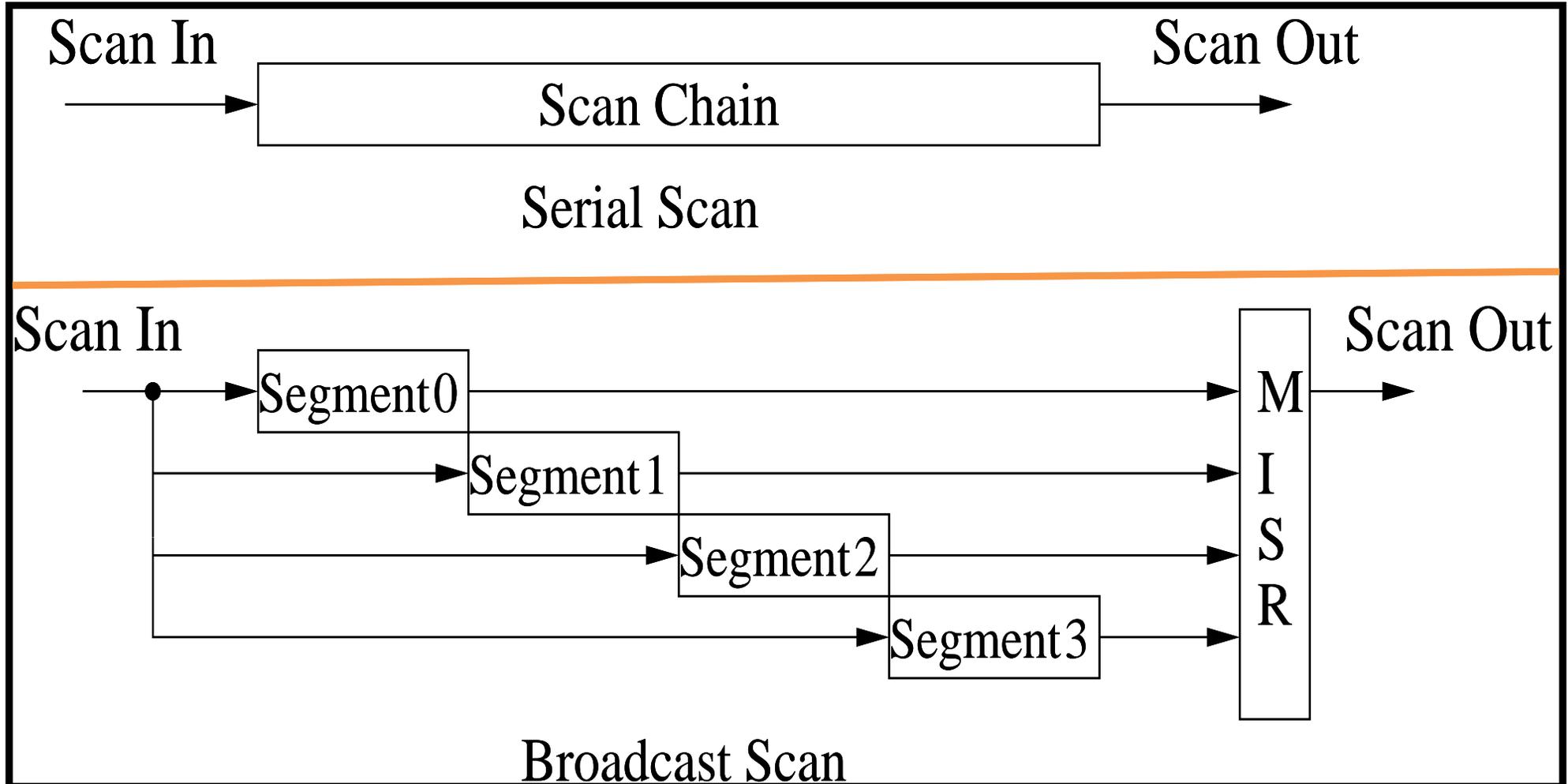
Outline of the Presentation

- Introduction of Illinois Scan Architecture (*ILS*)
- Layout aware *ILS* Design style
- Scan cell reordering procedure in order to reduce the power consumption
- Hybrid structure of *ILS* for reducing test time
- Experimental results
- Conclusions

Illinois Scan Architecture (ILS)

- Serial full scan technique is widely acceptable because of its high fault coverage and low cost of test generation.
- However, test application time and power dissipation increase significantly.
- Different methods are proposed to tackle the problem.
- Among them ILS is introduced recently to reduce the test application time.

Scan Architecture : Two Basic Modes



The ILS Architecture : Features

- In the *ILS* structure, a long scan chain is divided into many short segments that are loaded in parallel with the same test vector (called broadcast mode).
- The outputs of the different scan segments are fed to a multiple input signature register (*MISR*) to compress the responses.
- However, the constraints on the test bits often reduce the fault coverage of the circuit.
- To overcome this problem, a few additional test patterns are applied in serial full scan mode to detect the uncovered faults.

The ILS Architecture : Problems

- The main problem of *ILS* design is to select segments properly so that the objectives of reducing test time/data and that of achieving high fault coverage are satisfied concurrently.
- This may increase wiring cost significantly and introduces routing overhead
- None of the earlier works on the *ILS* structure considered the impact of physical design while determining the segments.

Contributions of This Paper

- A layout-aware design of *ILS* architecture which takes care of the physical locations of the flip-flops and considers tradeoffs.
- A three step algorithm for the generation of layout-aware *ILS* architecture.

Proposed ILS Architecture : Highlights

- It is a layout-aware design of *ILS* architecture.
- It takes care of the physical locations of the flip-flops.
- It provides a compromise among fault coverage, test application time, test data volume, and wiring cost.

The Proposed Algorithm for the ILS Architecture Generation: Inputs

The inputs to the algorithm are as follows:

- A given set of *FFs* and their corresponding coordinates in the layout area.
- A given set of deterministic test vectors.

The Proposed Algorithm for the ILS Architecture Generation: 3 Steps

The proposed algorithm consists of three steps:

Step-1: scan cells are grouped based on their geometric proximity to form the different segments of the *ILS*; this reduces wiring cost

Step-2: the flip-flops in different segments are aligned based on some incompatibility information; this reduces test application time

Step-3: ordering of the scan cells based on their coordinates

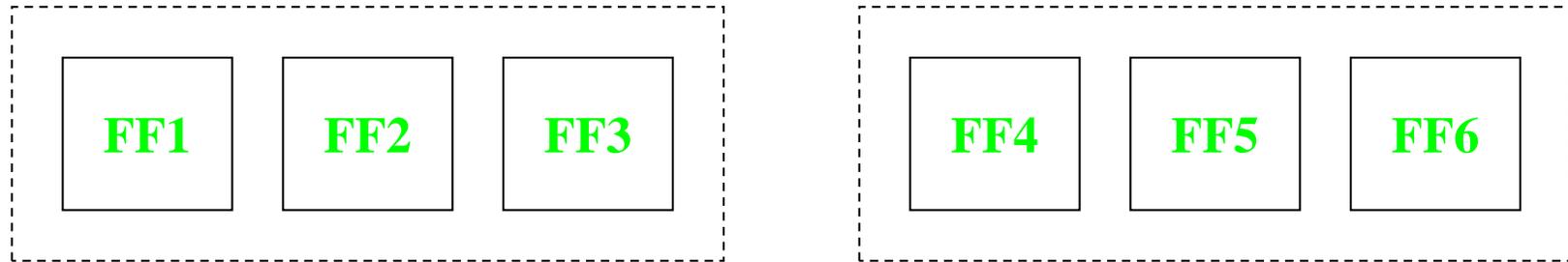
Proposed Algorithm Step-1 : Partitioning of Flip-Flops into *ILS* Segments

- In this step, the algorithm partitions the flip-flops into different groups based on their geometric neighborhood.
- In other words, the flip-flops nearest to each other are grouped, so that scan path length is minimized.
- Each group will form a segment of *ILS*, and the number of groups will be equal to the number of required segments in the *ILS* structure.
- In the present paper Integer Linear Programming is used to solve the problem.

Proposed Algorithm Step-2 : Determining the flip-flops to be placed in across segments

- The proposed algorithm will select one flip-flop from each segment, such that they have minimal incompatibility relationship.
- All such flip-flops will be placed in parallel (at the same depth) in the *ILS* structure.
- This will give rise to high fault coverage in broadcast mode.

Proposed Algorithm Step-2 (contd.)



Segment 1

Segment 2

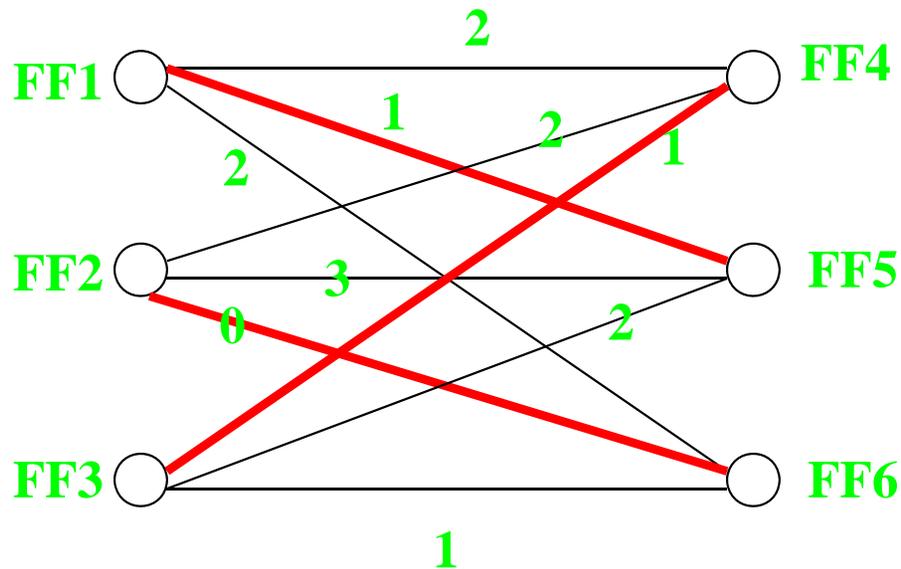
t1	1	0	0	0	1	0
t2	0	1	0	0	0	1
t3	1	1	1	0	0	1

- Consider the circuit of 6 flip-flops and corresponding test set.
- ILS structure consists of two segments as obtained from step-1.
- The next task is to find out three groups of two flip-flops each, by selecting one flip-flop from each segment.
- This selection problem can be solved by finding a perfect matching of a bipartite graph with minimum weight.

Proposed Algorithm Step-2 (contd.)

- Determine the incompatibility distance (d) of two flip-flops belonging to two segments.
- The incompatibility distance is defined as the number of conflicting bits in two corresponding column vectors of the test matrix.
- For the example, in the previous *Figure*, the following are distance values: $d(FF1,FF4)= 2$, $d(FF1,FF5)=1$.
- Then construct a graph $G(X, Y)$, called weighted incompatibility bipartite graph (*WIBG*).
- In G , left set of vertices represents the flip-flops in one segment, and right set of vertices represents the flip-flops in the other segment.

Proposed Algorithm Step-2 (contd.)

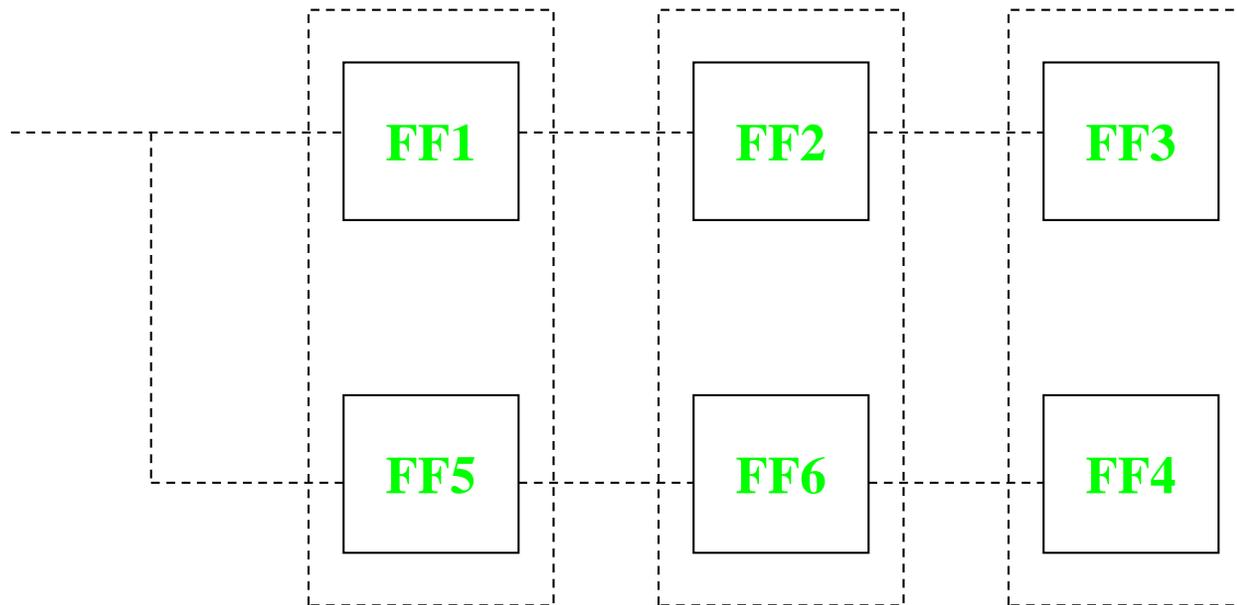


Nodes: Flip Flops
Weights: Incompatible Distance

- The weight on an edge represents the incompatibility distance between the two vertices connected by the edge.
- We seek a perfect matching M of graph G that minimizes the total weight.
- In the Figure, the minimum matching consists of three edges i.e. $M = \{FF1 FF5, FF2 FF6, FF3 FF4\}$, and the weight of M is 2.
- Two vertices or flip-flops connected by an edge of M can be grouped.

Proposed Algorithm Step-2 (contd.)

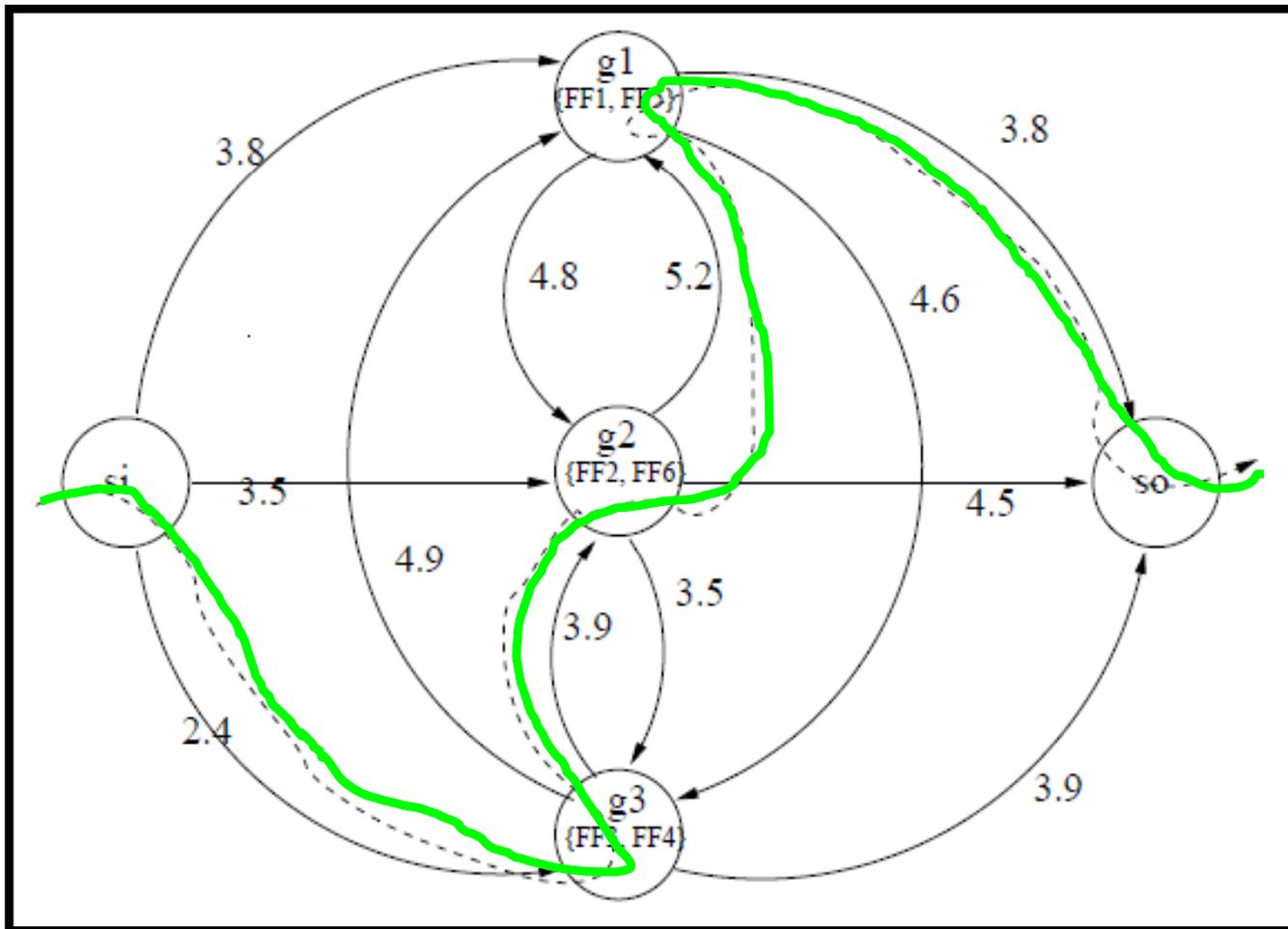
The resultant *ILS* structure is shown as follows:



Proposed Algorithm Step-3 : Ordering of the scan cells

- Scan cell ordering within a branch or partition is done by using a weighted distance graph (*WDG*).
- After creating *WDG*, the order of the scan cells can be determined by finding a shortest path from Scan Input to Scan Output.
- We have used Dijkstra's algorithm whose runtime is linear to find out the shortest path.

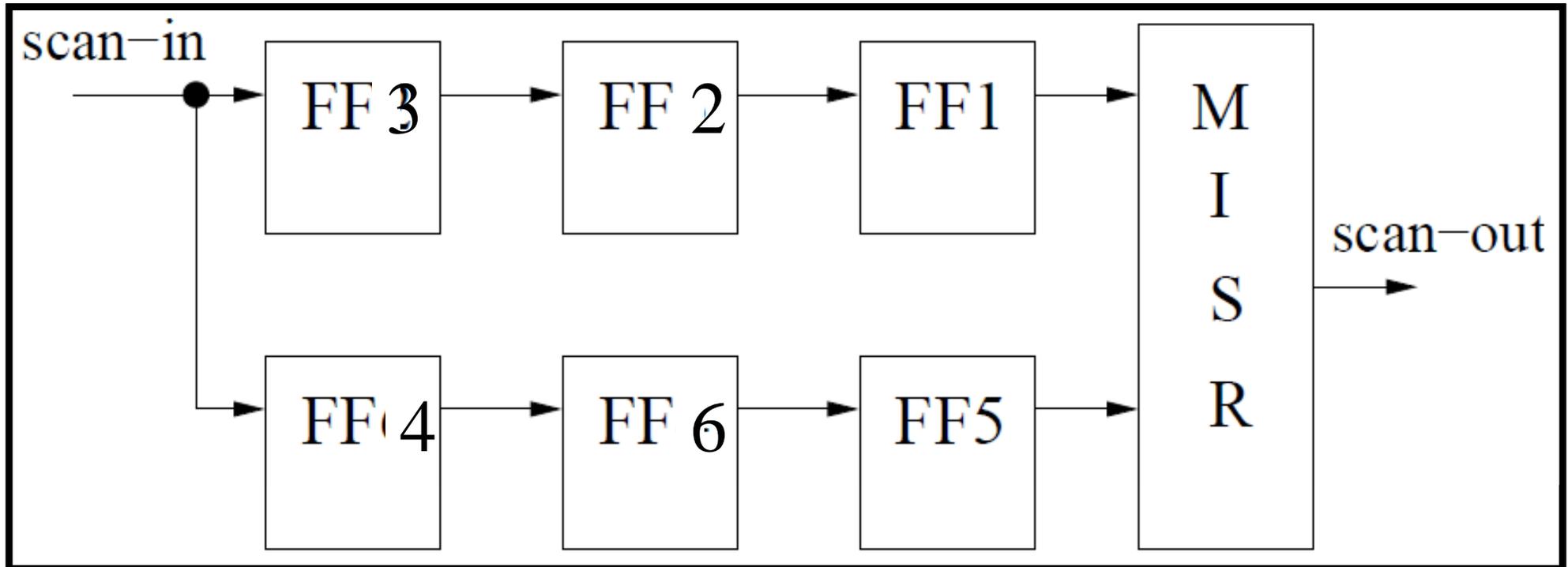
Proposed Algorithm Step-3 (contd.)



Nodes: FF Groups
Weights: Avg. Routing Length

- The WDG for ordering of the scan cells.
- The best path, shown dotted, is: s_i, g_3, g_2, g_1, s_o .

Proposed Algorithm Step-3 (contd.)

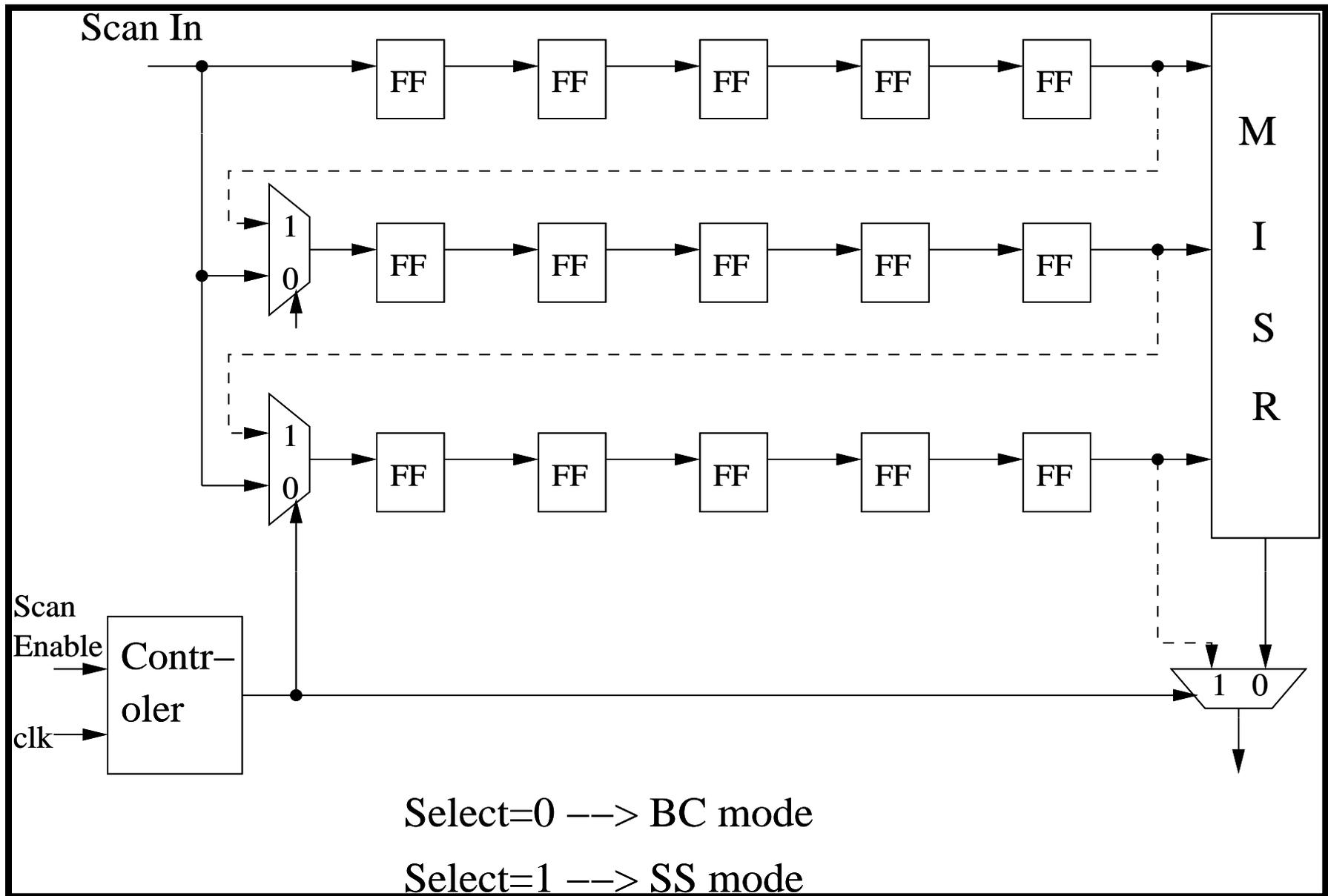


- Final ILS structure.

Serial Mode of ILS Architecture

- Once we obtain an *ILS* structure, find out the undetected fault in the broadcast mode.
- Apply the test vectors corresponding to these undetectable fault in serial mode.
- In this way a high fault coverage can be obtained.

Serial Mode of ILS Architecture (contd.)



Experimental Results

- The proposed algorithms are implemented in *C* on a *SUN SPARC ULTRA-60* workstation in *SOLARIS 5.8* environment and run on several *ISCAS'89* benchmark circuits.
- Experiments were performed on each circuit with *0.18 μm* digital *CMOS-9* standard cell library provided by the National Semiconductor.
- Each circuit is first synthesized by using the *Design Analyzer* tool of Synopsys.
- The test patterns are generated by the *TetraMax* tool from Synopsys.
- The goal of the experiments is to demonstrate: (i) the reduction of the scan path length in the ILS structure compared to full scan circuits, (ii) achieving high fault coverage in broadcast mode.

Experimental Results (contd.)

Table 1: Total wire length of the scan path w.r.t. number of segments

Number of segments in ILS	s1423 (μm)	s5378 (μm)	s9234 (μm)	s13207 (μm)	s15850 (μm)
1	9.2E + 3	5.1E + 4	7.5E + 4	2.3E + 5	1.2E + 5
2	8.5E + 3	4.1E + 4	6.1E + 4	1.4E + 5	0.9E + 5
4	7.5E + 3	3.6E + 4	5.1E + 4	0.8E + 5	0.3E + 5
6	7.1E + 3	2.9E + 4	4.8E + 4	9.6 + 4	8.8E + 4

Experimental Results (contd.)

Table 2: Results on test cycle reduction using proposed algorithms for *s1423* and *s5378*

#seg- ments in ILS	s1423					s5378				
	Broadcast Mode		Serial mode	Total test cycles	Total cove- rage (%)	Broadcast Mode		Serial mode	Total test cycles	Total cove- rage (%)
	#Test patte- rns	Fault cove- rage	#Test patte- rns			#Test patte- rns	Fault cove- rage	#Test patte- rns		
1	-	-	78	5924	99.3	-	-	192	34739	99.1
2	69	81.70	12	3633	98.6	210	78.5	37	25734	98.5
4	58	75.65	23	2920	98.1	197	61.2	62	20249	98.2
6	55	68.64	21	2377	96.7	189	57.9	59	16499	97.1

Conclusions

- In this paper, a layout-aware and coverage-driven design methodology for *ILS* architecture is proposed.
- The technique achieves significant improvements in fault coverage while at same time reduces the scan wire length to a great extent.
- The proposed design methodology is also suitable for a highly compact test set, i.e., when the flip-flops have very weak or no compatibility under a test set.

References

- [1] Y. Bonhomme, P. Girard, C. Landrault, and S. Pravossoudovitch, “Power driven chaining of flip-flops in scan architectures,” Proc. International Test Conference, 7-10 Oct. 2002, pp. 796 – 803.
- [2] A.R. Pandey and J.H. Patel, “An incremental algorithm for test generation in Illinois scan architecture based designs,” Proc. Design, Automation and Test in Europe Conference and Exhibition, 4-8 March 2002, pp. 368 – 375.
- [3] F.F. Hsu, K.M. Butler, and J.H. Patel, “A case study on the implementation of the Illinois Scan Architecture,” Proc. International Test Conference, 30 Oct.-1 Nov. 2001, pp. 538 – 547.
- [4] P. Gupta, A.B. Kahng, and S. Mantik, “Routing-aware scan chain ordering,” Proc. Asia and South Pacific Design Automation Conference, 21-24 Jan. 2003, pp. 857 – 862.
- [5] M.A. Shah and J.H. Patel, “Enhancement of the Illinois scan architecture for use with multiple scan inputs,” Proc. DATE, 4-8 March 2002, pp. 368 – 375.
- [6] D. Berthelot, S. Chaudhuri, and H. Savoj, “An efficient linear time algorithm for scan chain optimization and repartitioning,” Proc. International Test Conference, 7- 10 Oct. 2002, pp. 781 – 787.

THANK YOU