Nano-CMOS Mixed-Signal Circuit Metamodeling Techniques: A Comparative Study

O. Garitselov[1], S. P. Mohanty[2], E. Kougianos[3], P. Patra[4]

NanoSystem Design Laboratory (NSDL, http://nsdl.cse.unt.edu), University of North Texas, Denton, TX 76203, USA.[1,2,3]

Intel Architecture Group, Intel Corporation, USA.[4]

E-mail: saraju.mohanty@unt.edu

Presented By:
Garima Thakral
University of North Texas

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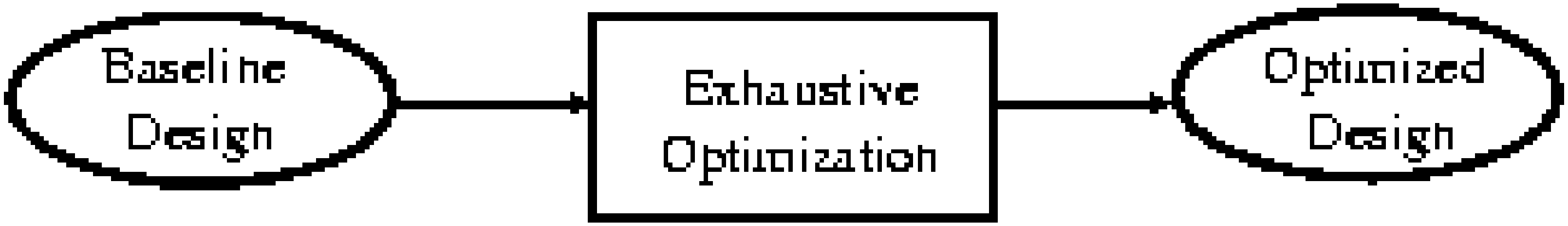
Outline of the talk

- Introduction
- Fast Design Exploration through Metamodeling
- Metamodeling vs. Macromodeling
- Metamodeling based Design Flow
- Sampling Techniques
- Ring Oscillator Example Circuit
- “Golden” Surface
- Experimental Results
- Conclusions and Future Research

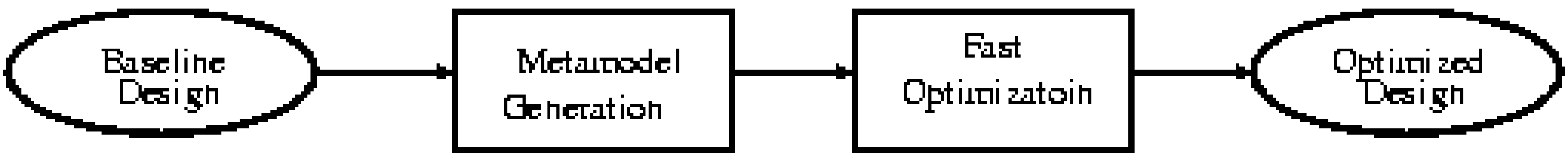
Introduction

- Complex computations for analog circuits to include parasitics
- Physical layout and simulation analysis is very costly processes in design flow
- Metamodeling is mathematical formula that represents circuit's behavior within a given range using sampling points
- This paper targets sampling techniques which are technology independent and the amount that is needed to create an accurate metamodel

Fast Design Exploration Through Metamodeling



a. Traditional Slow Approach

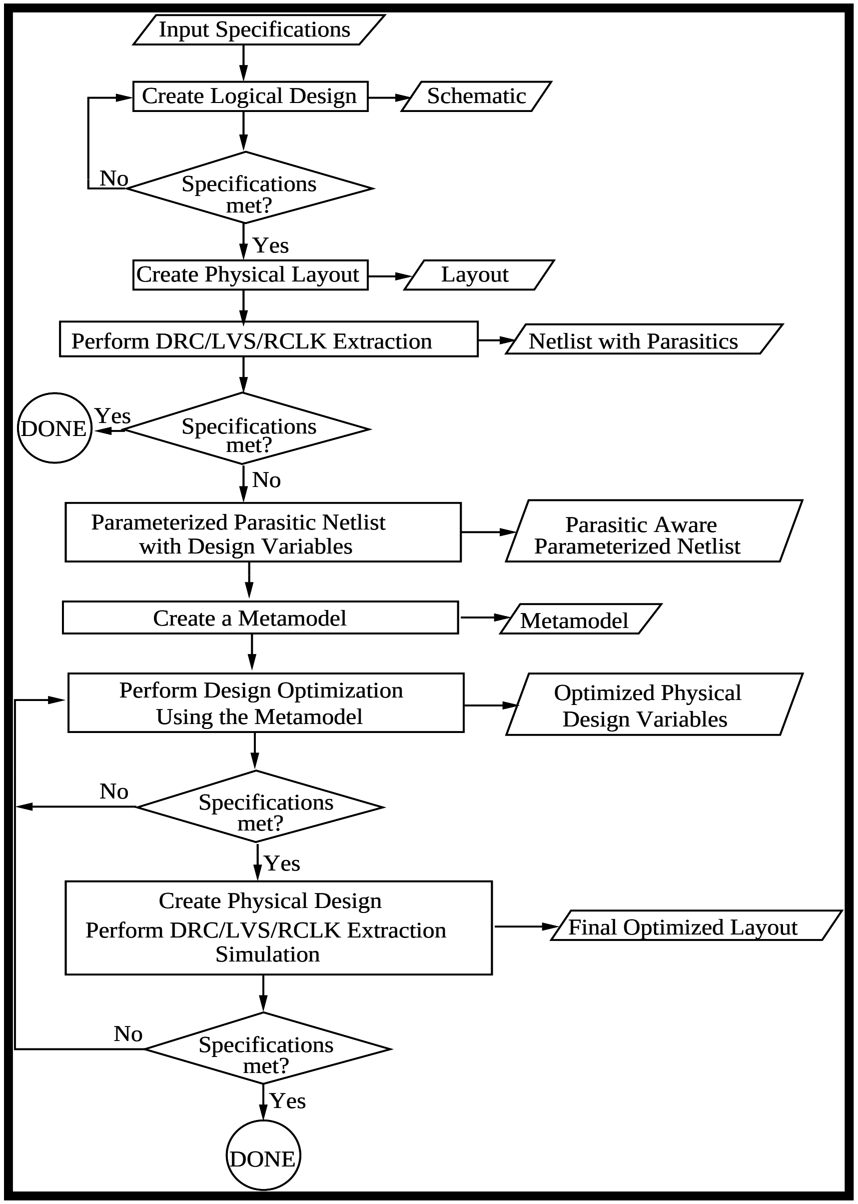


b. Metamodeling-Based Fast Approach

Metamodeling vs. Macromodeling

- **Metamodeling**
  - mathematical representation of output
  - prediction equation
  - can be used in different tool like MATLAB
- **Macromodeling**
  - simplified version of the circuit
  - used in same simulation tool
  - hard to create

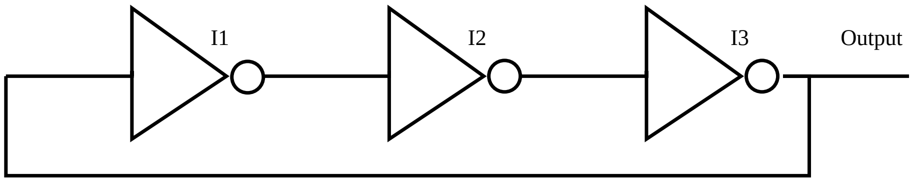
Metamodeling Design Flow

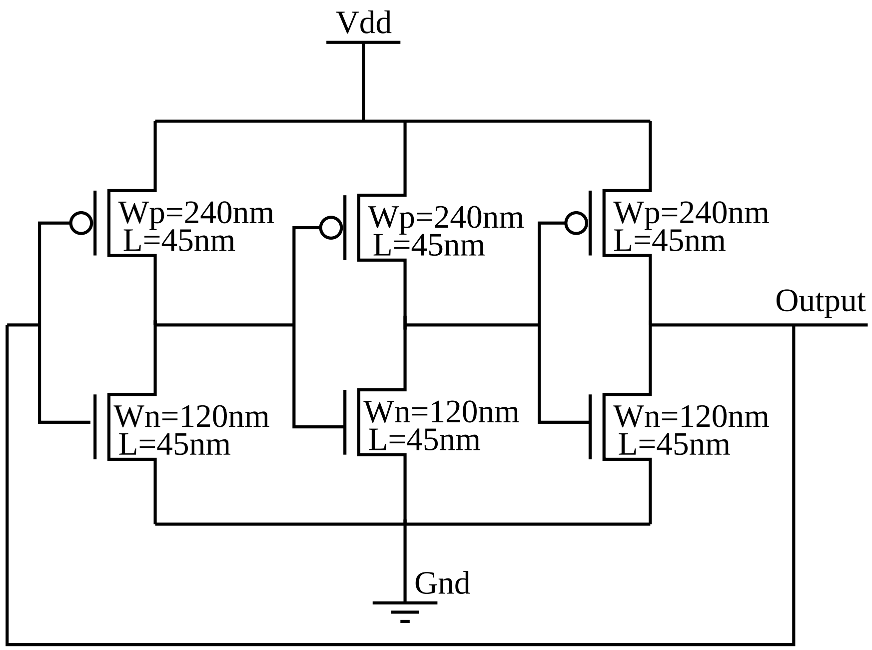


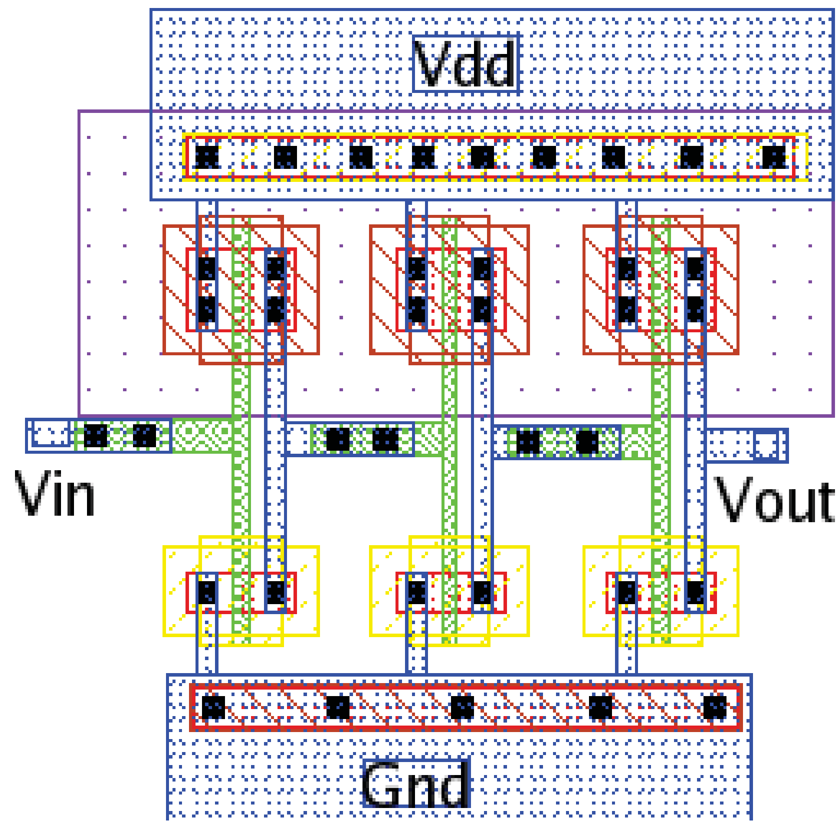
- Regular design flow is altered for using metamodels.
- Advantages for using metamodels:
  - Reusability
  - Speed
  - Accuracy
- Physical design is done only 2 times in the proposed design flow.

Ring Oscillator: 45nm CMOS Design

$f = \dfrac{1}{2Nt_p}$ Where f - frequency of oscillations, N - number of inverters, t_p - delay of each inverter







Ring Oscillator: Characterization

Eye Diagram for Parasitic Aware Netlist Simulation

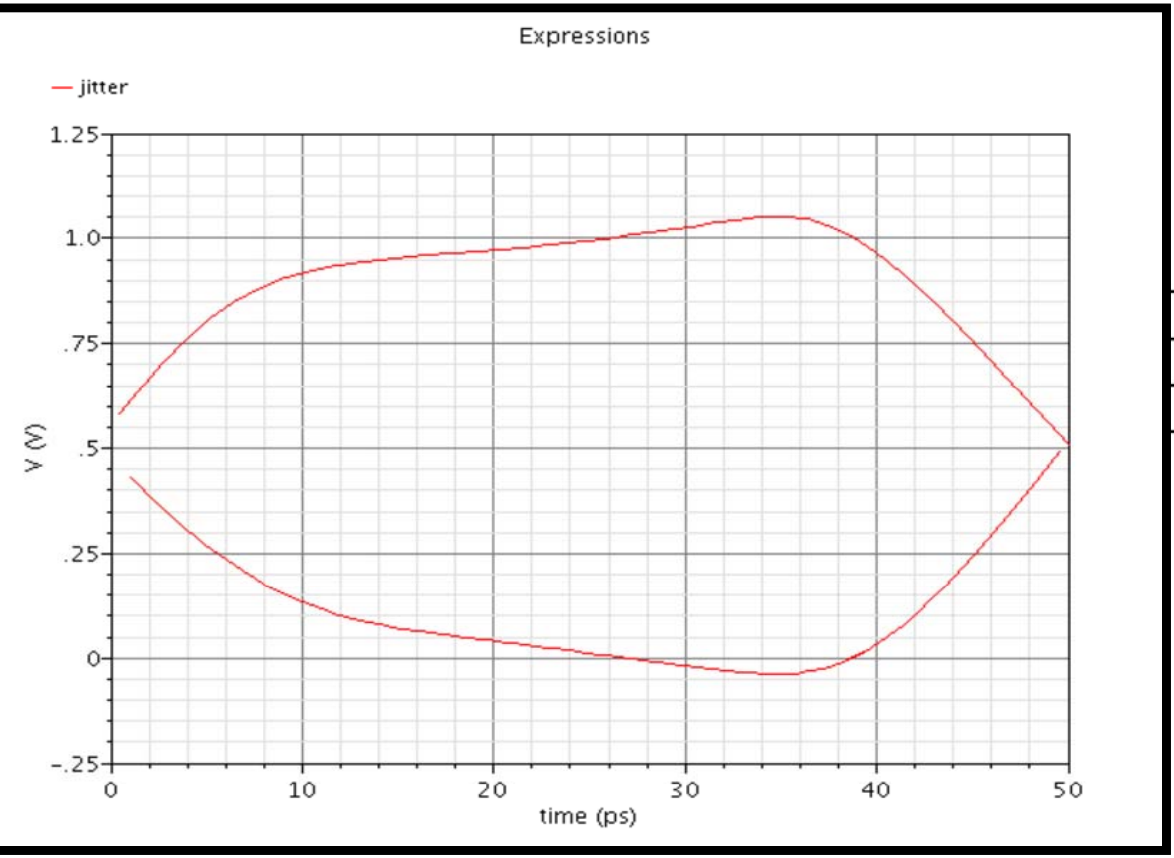


TABLE II
SIMULATION COMPARISON

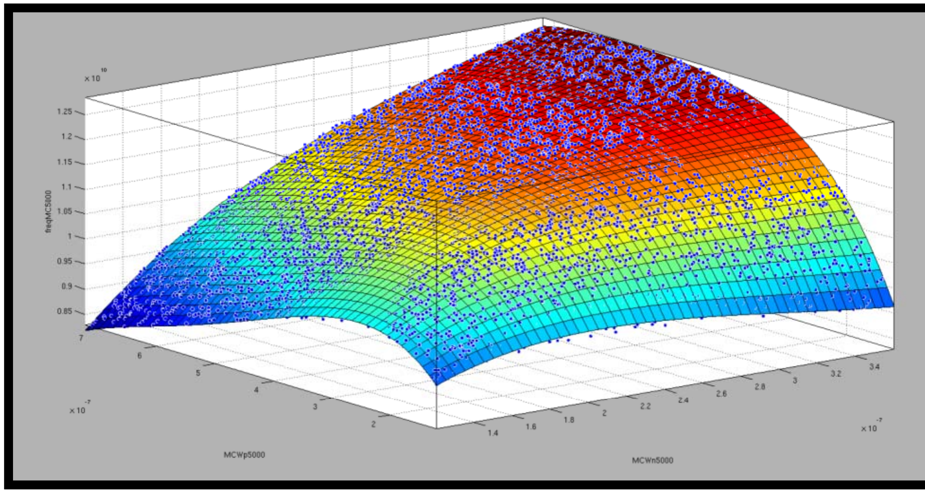
Extraction	Power	Frequency
Schematic	27.17 μW	16.21 GHz
120nm-240nm Parasitic	26.96 μW	9.88 GHz

Sampling Techniques Explored

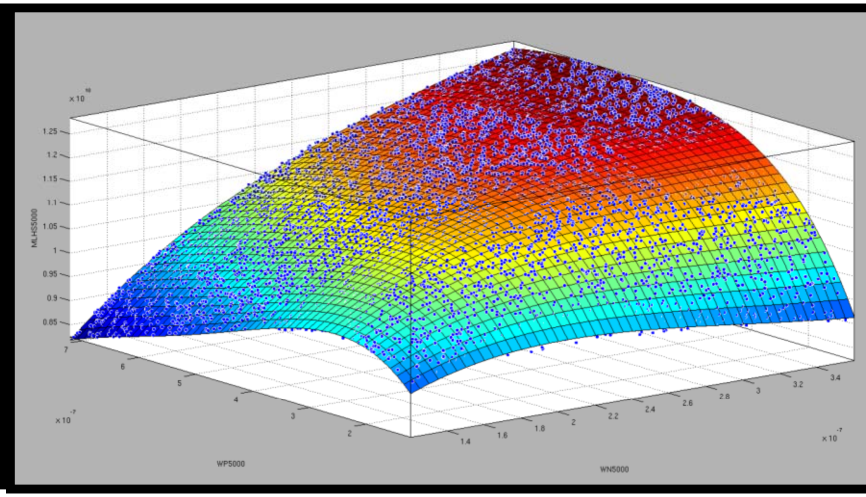
- Exhaustive – evenly distributed large amount of samples
- Monte Carlo – random sampling
- Latin Hypercube – random sampling within each Latin square
- Middle Latin Hypercube – middle point sampling within each Latin square
- Design of Experiments – min, mid, max sampling for each parameter

Sampling Techniques: Applied to Ring Oscillator Circuit

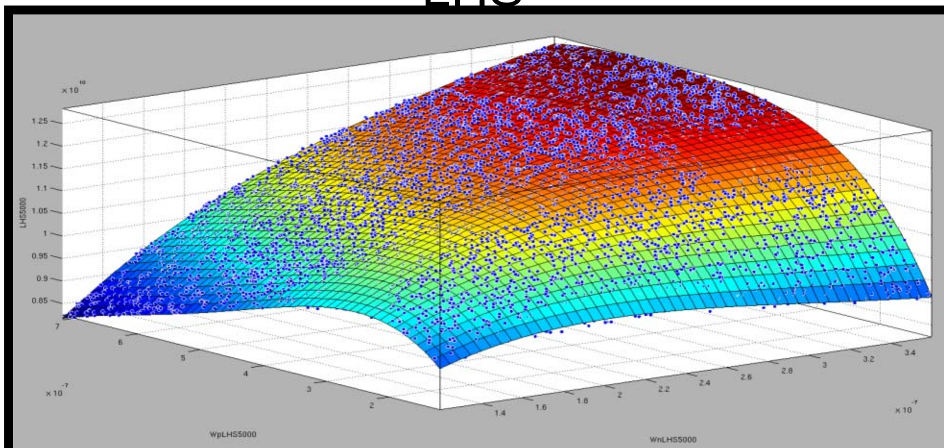
Monte Carlo



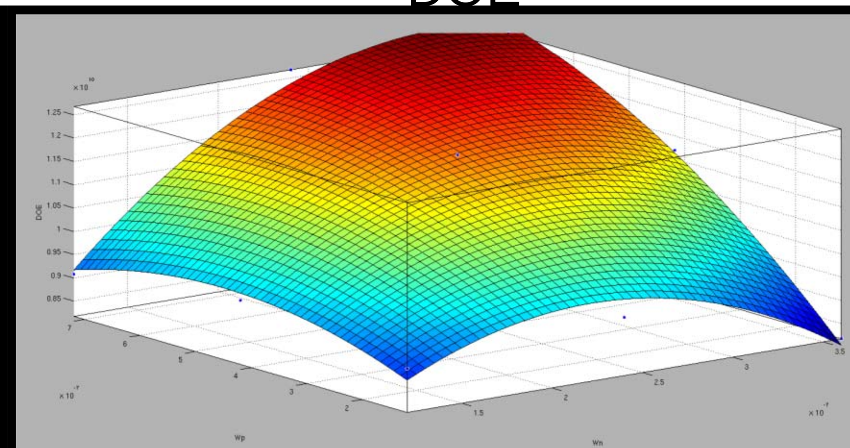
MLHS



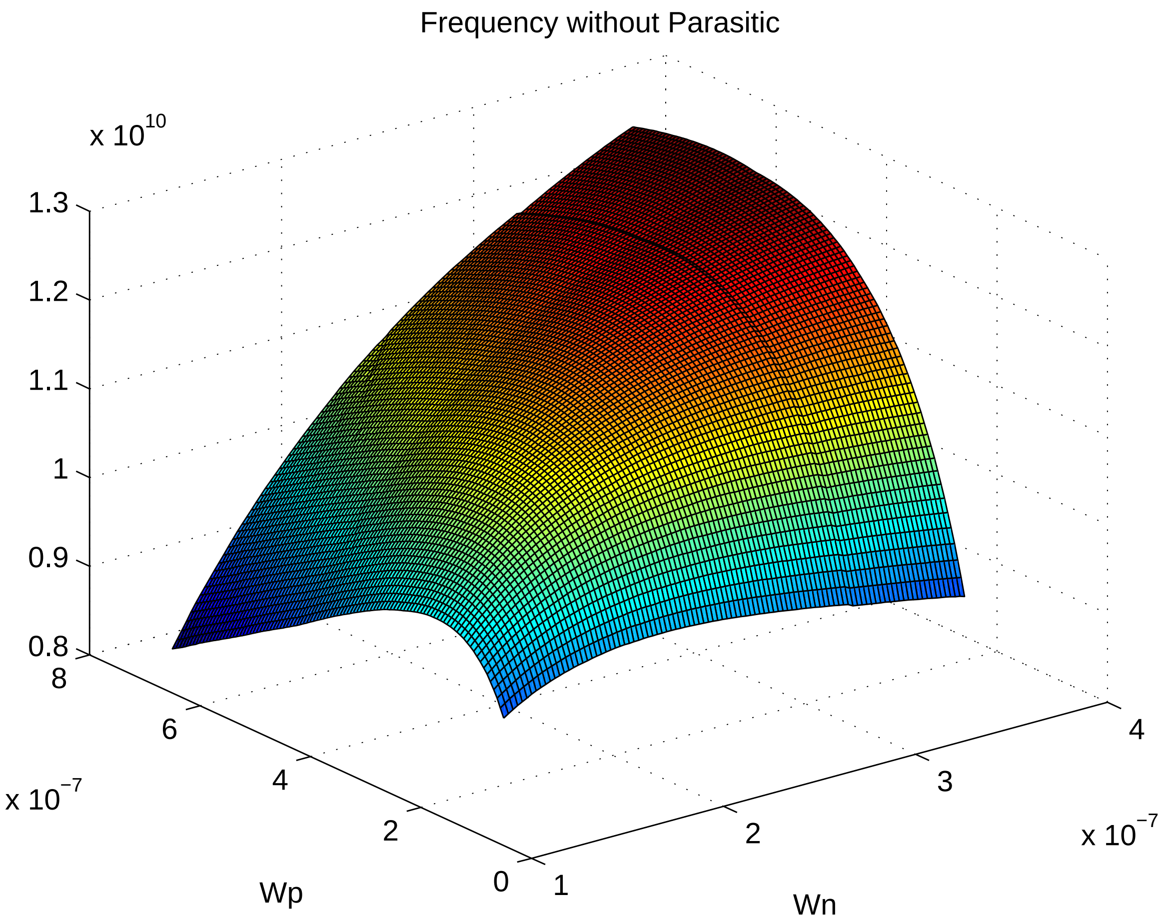
LHS



DOE



“Golden” Surface



10,000 sampling surface was created for exhaustive analysis.

-RMSE < 0.01%

“Golden” Surface is used as actual results to compare to the sampling techniques.

The Metamodels

- The generated sample data can be fitted in many ways to generate a metamodel.
- The choice of fitting algorithm can affect the accuracy of the metamodel.
- Metamodel has the form: $$y = \sum_{i,j=0}^{k} \left(\alpha_{ij} \times x_1^i \times x_2^j \right)$$
- Where y is the response being modeled (e.g. frequency), $x = [W_n, W_p]$ is the vector of variables and α_{ij} are the coefficients.
- The polynomial regression determined k = 2 for DOE and k = 4 for other cases.

Error Analysis

$$RMSE = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(y(x_k) - \hat{y}(x_k)\right)^2},$$

$$\sigma = \sqrt{\frac{1}{N}\sum_{k=1}^{N}\left(\left|y(x_k) - \hat{y}(x_k)\right| - RMSE\right)^2},$$

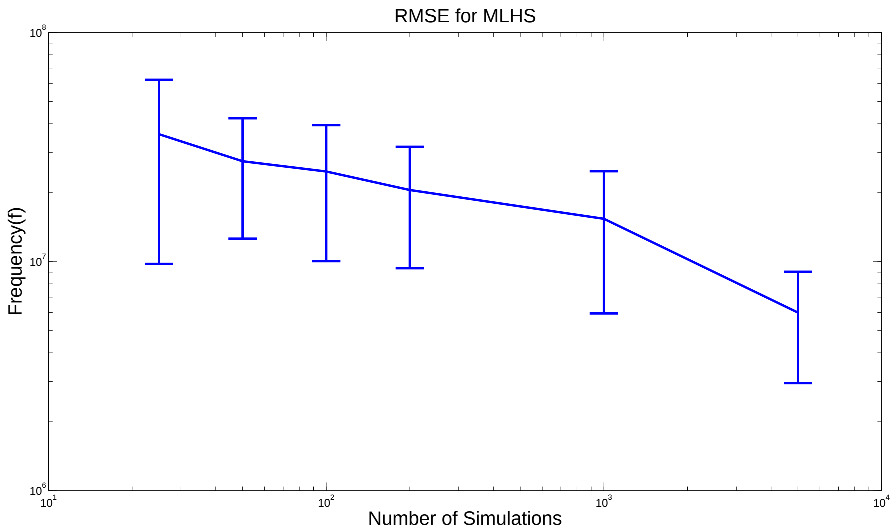
Where:

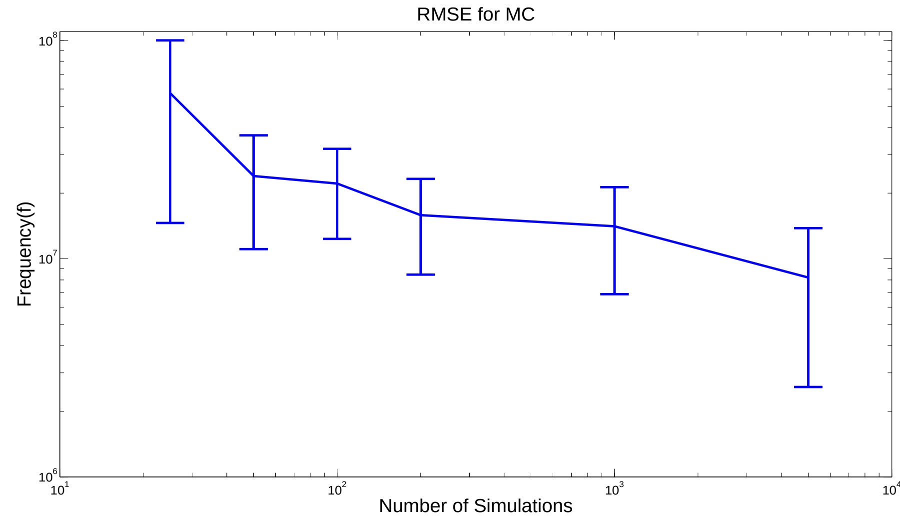
x_k is the set of parameters

$\hat{y}$ is the predicted equation

N is the number of sampling points

Experimental Results





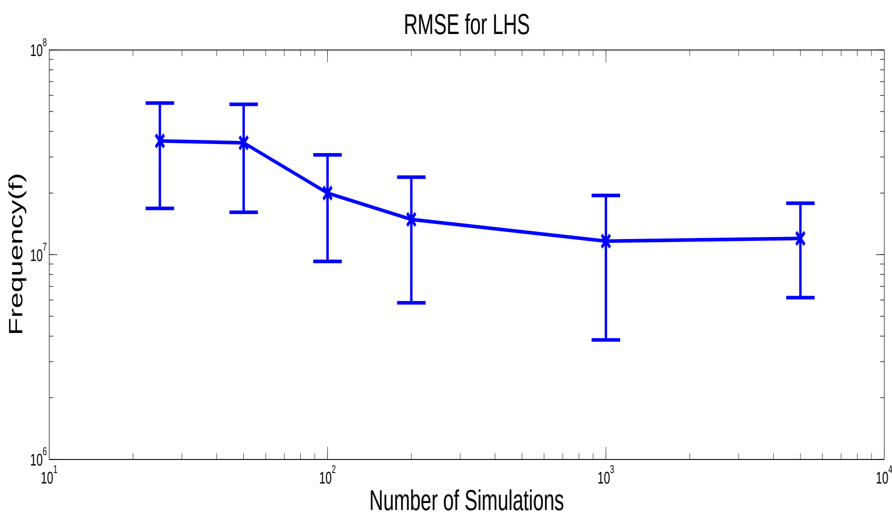


TABLE III
RMSE COMPARISON FOR DIFFERENT SAMPLING TECHNIQUES (IN MHZ)

Samples	MC		LHS		MLHS	
N	μ	σ	μ	σ	μ	σ
25	57.5	42.9	35.6	19.1	36.0	26.2
50	24.0	12.9	35.2	19.1	27.4	14.8
100	22.1	9.79	20.0	10.7	24.8	14.7
200	15.9	7.39	14.9	9.04	20.5	11.2
1000	14.1	7.21	11.7	7.81	15.4	9.44
5000	8.20	5.62	12.0	5.84	5.99	3.04

Conclusions

- A design flow for metamodeling is proposed
- A 45nm ring oscillator was subjected to the proposed design flow
- Uniform sampling techniques has better performance than DoE or than randomized.
- Designers should choose LHS or MLHS over MC but the trend in typical design environments is the opposite.

Future Research

- Our future research will include the optimization techniques part of the proposed design flow. We will conduct thorough study by using metamodel optimization for higher amount of variables by the example of a more complex nano-CMOS circuit.


Thank you !!!