A P4VT (Power-Performance-Process - Parasitic-Voltage-Temperature) Aware Dual-V_{Th} Nano-CMOS VCO

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Outline of the Talk

- Introduction
- Novel Contributions of this paper
- Related Prior Research
- Proposed Novel P4VT Aware Design Flow
- Logical Design of VCO
- PVT Variation Analysis of VCO
- P4VT Optimization of VCO
- Conclusions and Future Research

Introduction …

- **Power-Performance:** Radio Frequency Integrated Circuits (RFICs) must be simultaneously:
  - Low power consuming
  - High performance
- **Process-Voltage:** Impact of process and supply voltage variations on the performance factors of a design is much higher for nanometer technologies.

Introduction

- **Parasitics:** In high frequency application circuits, the exact performance prediction is challenging due to many parasitic effects. It is crucial to be able to account parasitic effects for accurate performance.
- **Temperature:** There is a need for temperature-aware design methodologies in order to produce properly functioning and reliable silicon.

Novel Contributions of This Paper

- A Power-Performance-Parasitic-Process-Voltage-Temperature (called P4VT) aware optimization flow for nanoscale CMOS analog circuits is introduced.
- The design of a P4VT-aware RF nano-CMOS circuit, VCO is discussed.
- For power optimization of the VCO, a dual-threshold process level technique is discussed.
- A dual-threshold physical design of the optimized VCO is presented.

Prior Research: VCO Design

Research	Tech. Node	Performance	Power	Area
Tiebout et al.	250nm	1.8GHz	20mW	1.1mm^2
Troedsson et al.	250nm	2.4GHz	5.5mW	0.874µm^2
Long et al.	180nm	2.4GHz	1.8mW	--
Kwok et al.	180nm	1.4GHz	1.46mW	0.76mm^2
This Paper	90nm Dual-V_{Th}	2.4GHz	137.5µW	547.7µm^2

Prior Research: PVT Tolerance

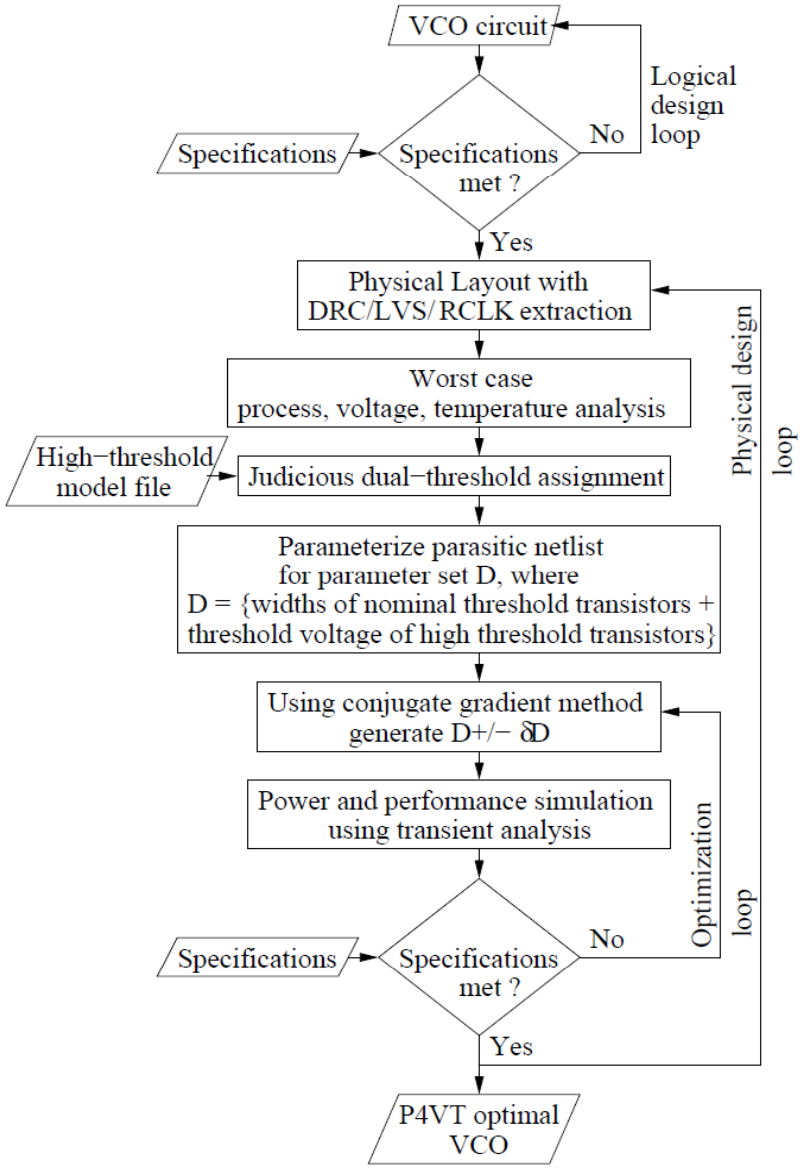
- **Kim 2009**: PVT-tolerance using supply/body-bias voltage generation.
- **Charan 2008**: Corner analysis used for PVT-tolerant humidity sensor.
- **Miyashita 2005**: Automatic amplitude control is used to reduce PVT variation in LC-VCO.
- **Kondou 2007**: Two on-chip digital calibration circuits are used for PVT-tolerant PLL.

Prior Research: Parasitic Tolerance

- **Park 2003**: Parasitic-Aware optimization of CMOS wideband amplifier.
- **Choi 2006**: Simulated annealing optimization for parasitic-aware RF power amplifier.
- **Choi 2003**: Particle swarm optimization techniques for parasitic-aware CMOS RF circuits.

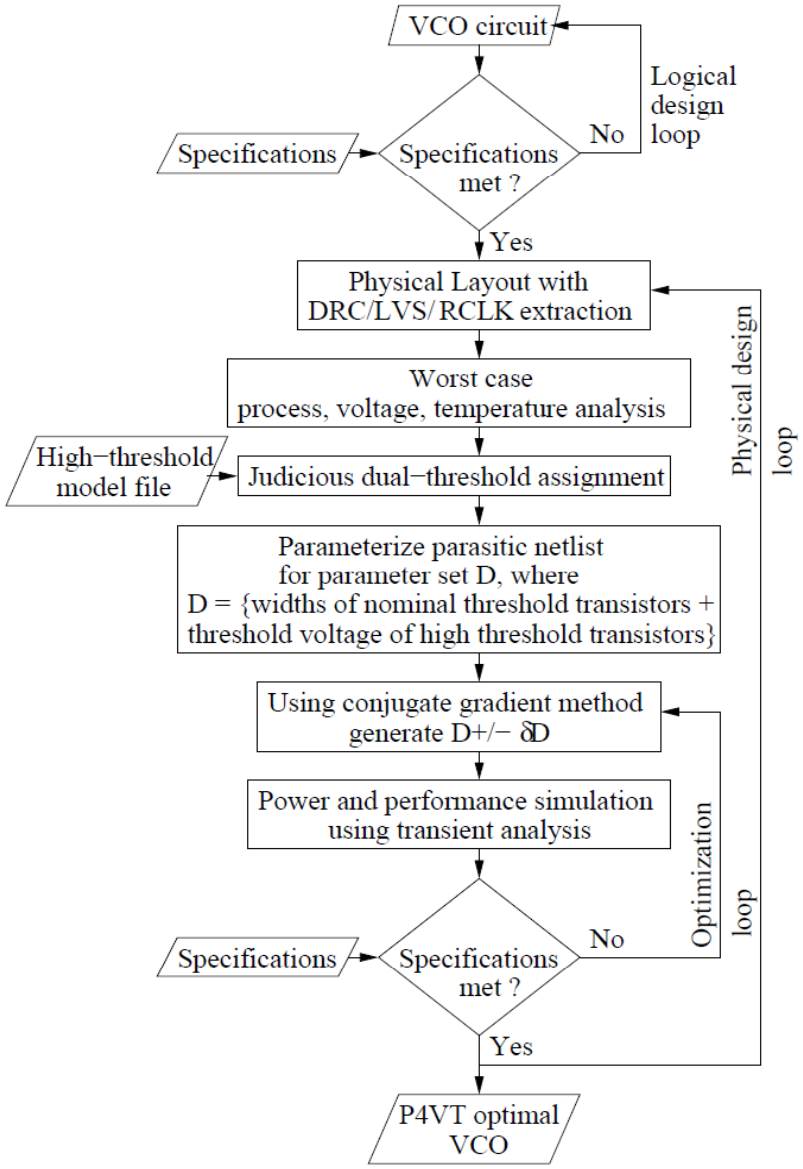
Proposed Novel P4VT Aware Design Flow …

- Logical design performed to meet the specifications.
- Preliminary physical layout subjected to DRC/LVS/RCLK.
- RCLK extracted physical design is subjected to process, voltage and temperature variation analysis.
- Dual-threshold assignment (HV_{Thn} , HV_{Thp}) to the power-hungry transistors of the VCO.

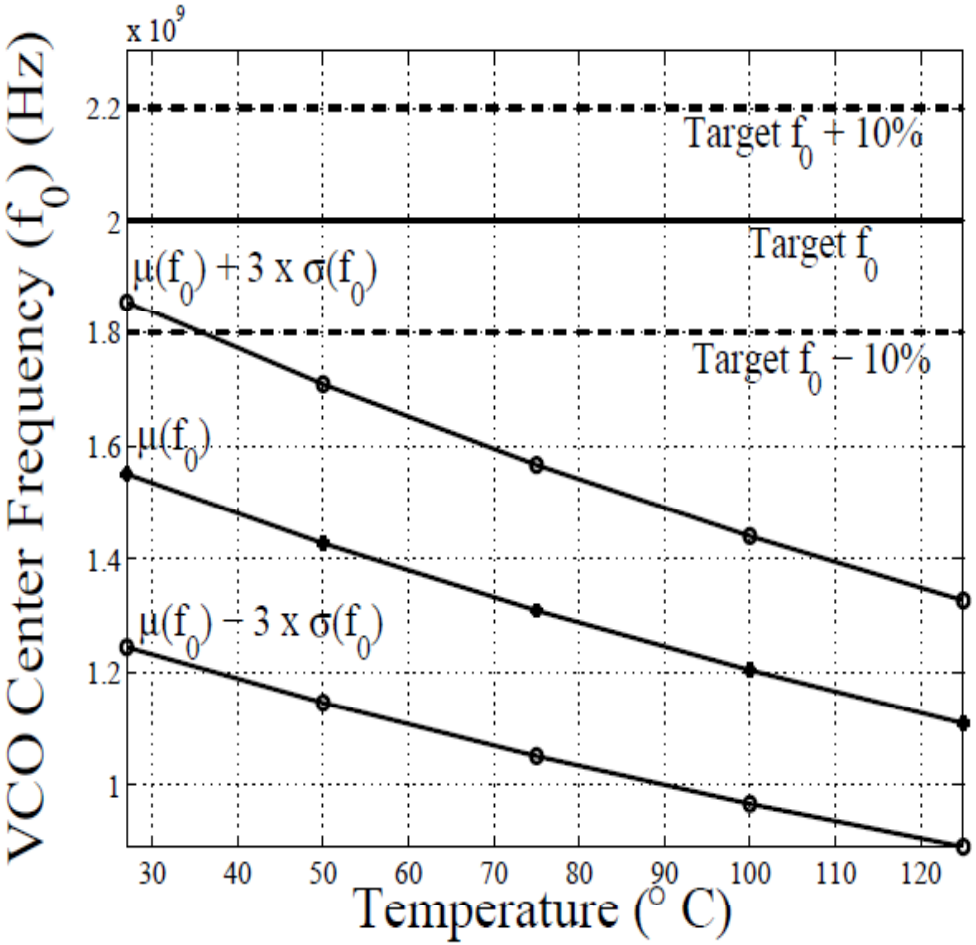


Proposed Novel P4VT Aware Design Flow

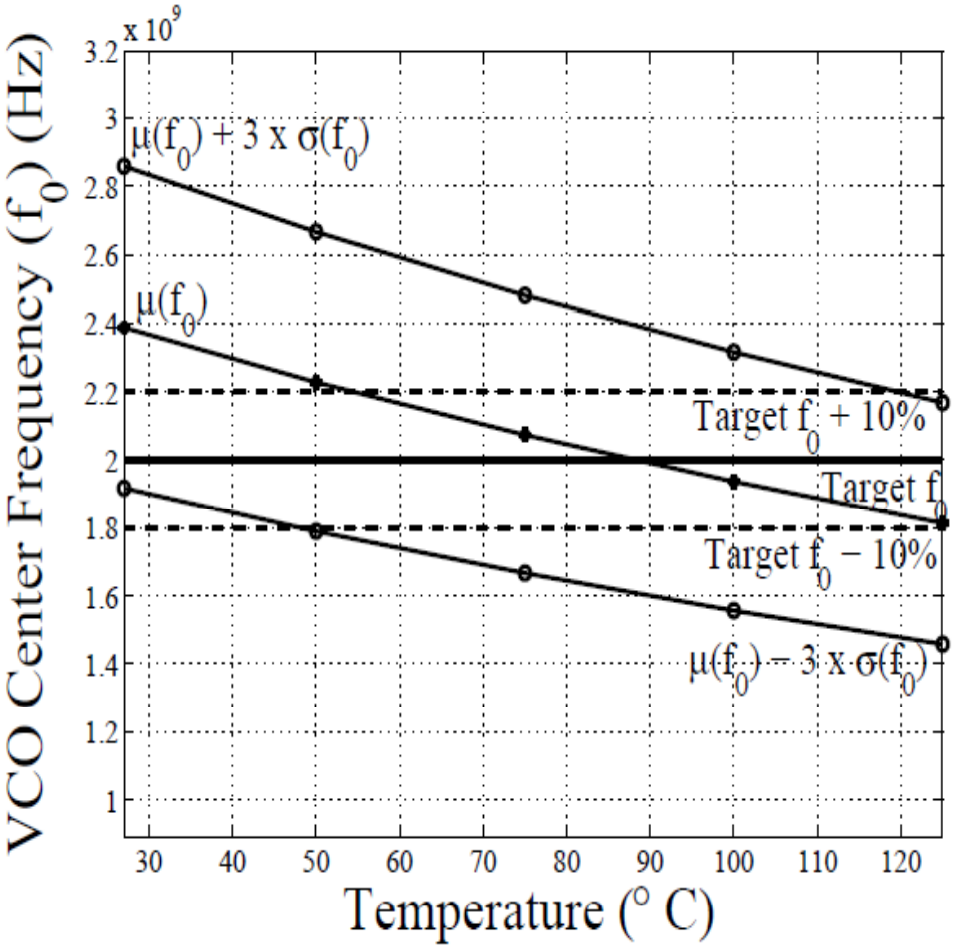
- Parasitic netlist is parameterized for parameter set D (widths of transistors and HV_{Thn}, HV_{Thp}).
- Parameterized netlist is subjected to optimization for *worst case PVT* variations.
- Parameter values for which the specifications are met are determined.
- Final physical design of the VCO is performed using these parameter values.



Center Frequency (f_0) vs. Temperature



- Non-Optimized VCO



- P4VT Optimized VCO

Logical Design of 90nm CMOS VCO

- Current starved VCO design performed using 90nm process. Following equations are used:

$$f_0 = \frac{I_D}{N * C_{tot} * V_{DD}}$$

$$C_{tot} = \frac{5}{2} C_{ox}(W_p L_p + W_n L_n)$$

$$C_{ox} = \frac{\varepsilon_{r_{ox}} \varepsilon_0}{T_{ox}}$$

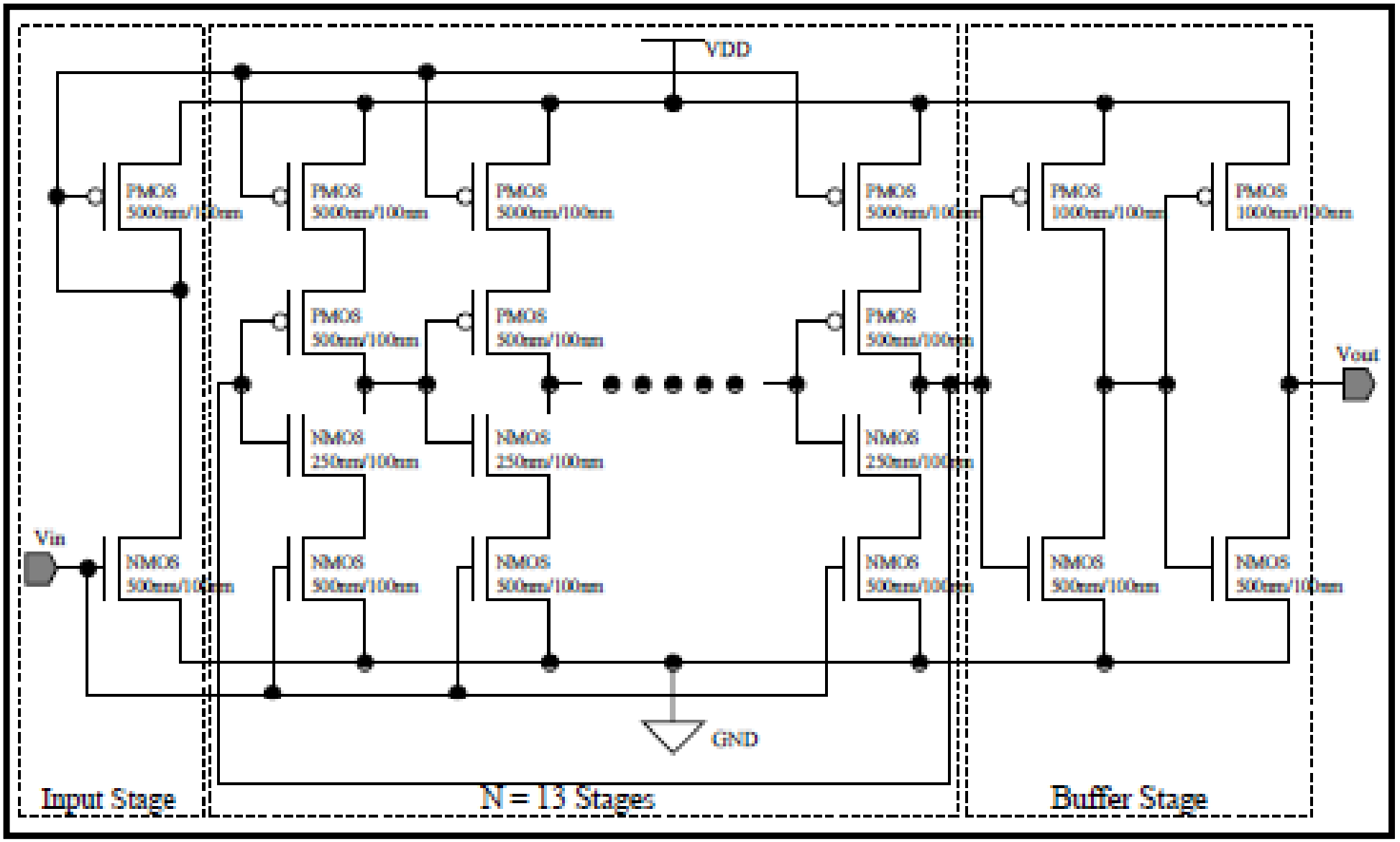
  - V_{DD} : supply voltage, I_D: current flowing through inverter, N: odd number of inverters, C_{tot}: total capacitance of each inverter stage, C_{ox}: gate oxide capacitance per unit area.

Logical Design of 90nm CMOS VCO

- For a target oscillation frequency $(f_0) \geq 2GHz$ for 90nm node:

- {Wp, Lp}: inverter PMOS width (500nm) and length (100nm).
- {Wn, Ln}: inverter NMOS width (250nm) and length (100nm)
- {Wpcs, Lpcs}: current starved PMOS width (5um) and length (100nm)
- {Wncs, Lncs}: current starved NMOS width (500nm) and length (100nm).

Logical Design of 90nm CMOS VCO



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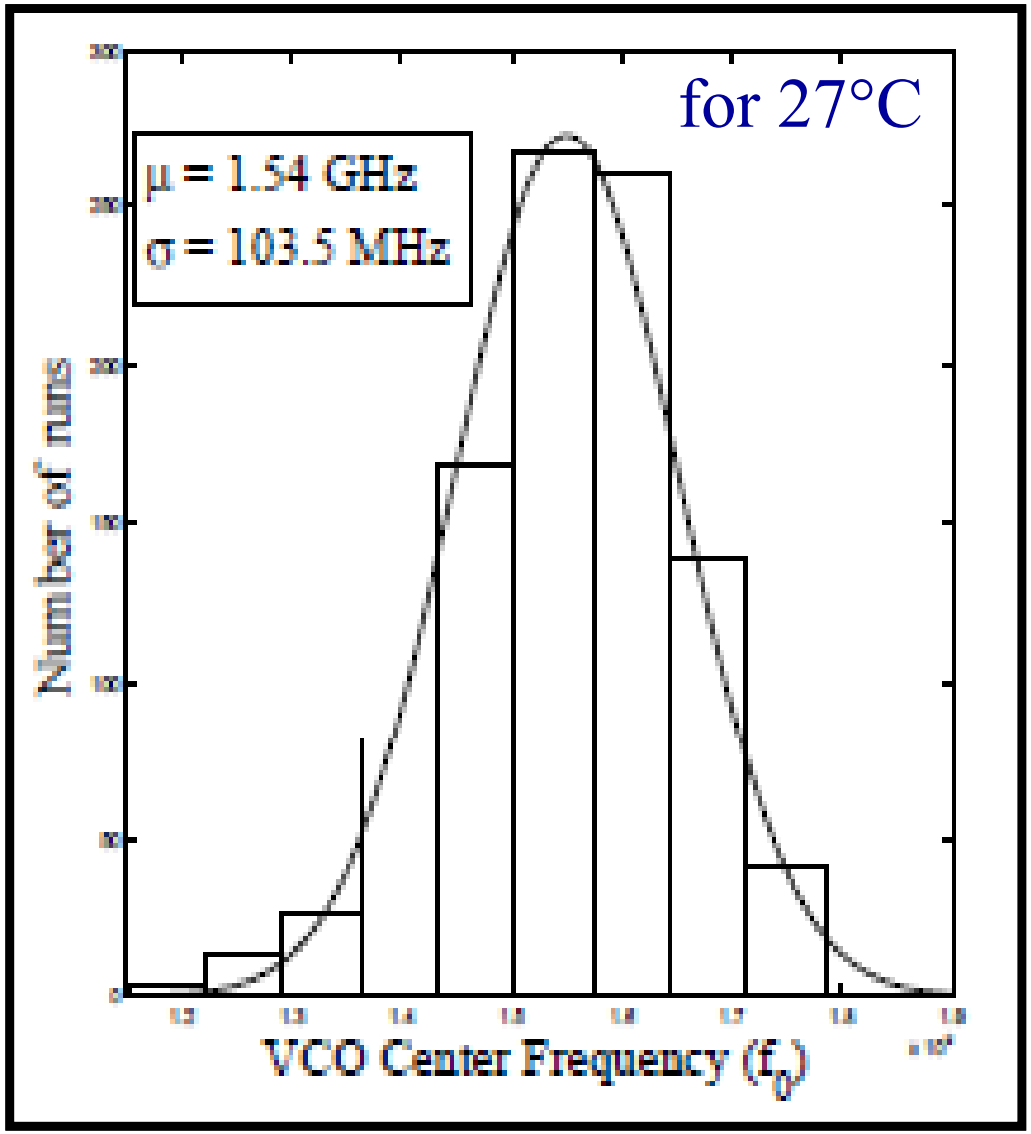
PVT Variation Analysis of VCO

- Process-voltage variation analysis has been carried out on the initial physical design with parasitics (RLCK) extracted netlist.
- Monte Carlo simulation for 1000 runs performed for variation in 5 parameters:
  - V_{DD}: Supply voltage
  - V_{Thn}: NMOS threshold voltage
  - V_{Thp}: PMOS threshold voltage
  - Toxn: NMOS gate oxide thickness
  - Toxp: PMOS gate oxide thickness.
- for temperatures = 27°C, 50°C, 75°C, 100°C, 125°C.



PVT Variation Analysis of VCO

- The worst-case process variation is where V_{Thn}, V_{Thp}, Toxn, Toxp) are increased by 10%.
- The worst-case voltage variation is where VDD is reduced by 10%.
- The worst-case temperature variation is 125°C.

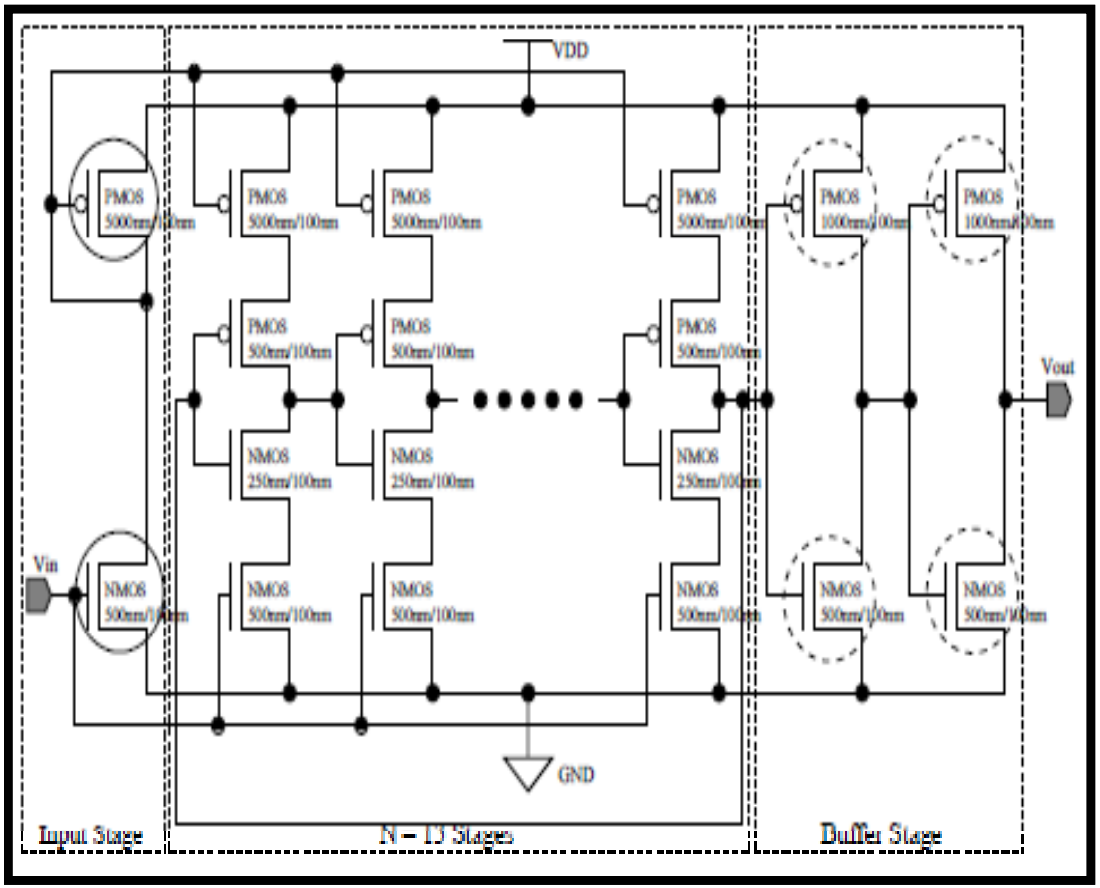
P4VT Optimization of VCO

- Logical design center frequency $f_0 \geq 2$ GHz.
- Preliminary physical design center frequency $f_{0p} = 1.56$ GHz (25% degradation).
- Preliminary physical design center frequency in *worst case PVT* conditions $f_{0pvt} = 1$ GHz (50% degradation).
- Initial average power consumption (including leakage) (P_{VCO}) = 164.5µW.

Parameter	Initial Physical Design	Initial Physical Design + Process Variation	Final Physical Design + Process Variation
f_0	$1.56GHz$	$1.13GHz$	$1.98GHz$
discrepancy	25%	43.5%	1%
V_{DD}	$1.2V$ (nominal)	$1.08V$ (-10%)	$1.08V$
V_{tn}	$0.1692662V$ (nominal)	$0.186193V$ ($+10\%$)	$0.186193V$
V_{tp}	$-0.1359511V$ (nominal)	$-0.149546V$ ($+10\%$)	$-0.149546V$
T_{oxn}	$2.33nm$ (nominal)	$2.563nm$ ($+10\%$)	$2.563nm$
T_{oxp}	$2.48nm$ (nominal)	$2.728nm$ ($+10\%$)	$2.728nm$

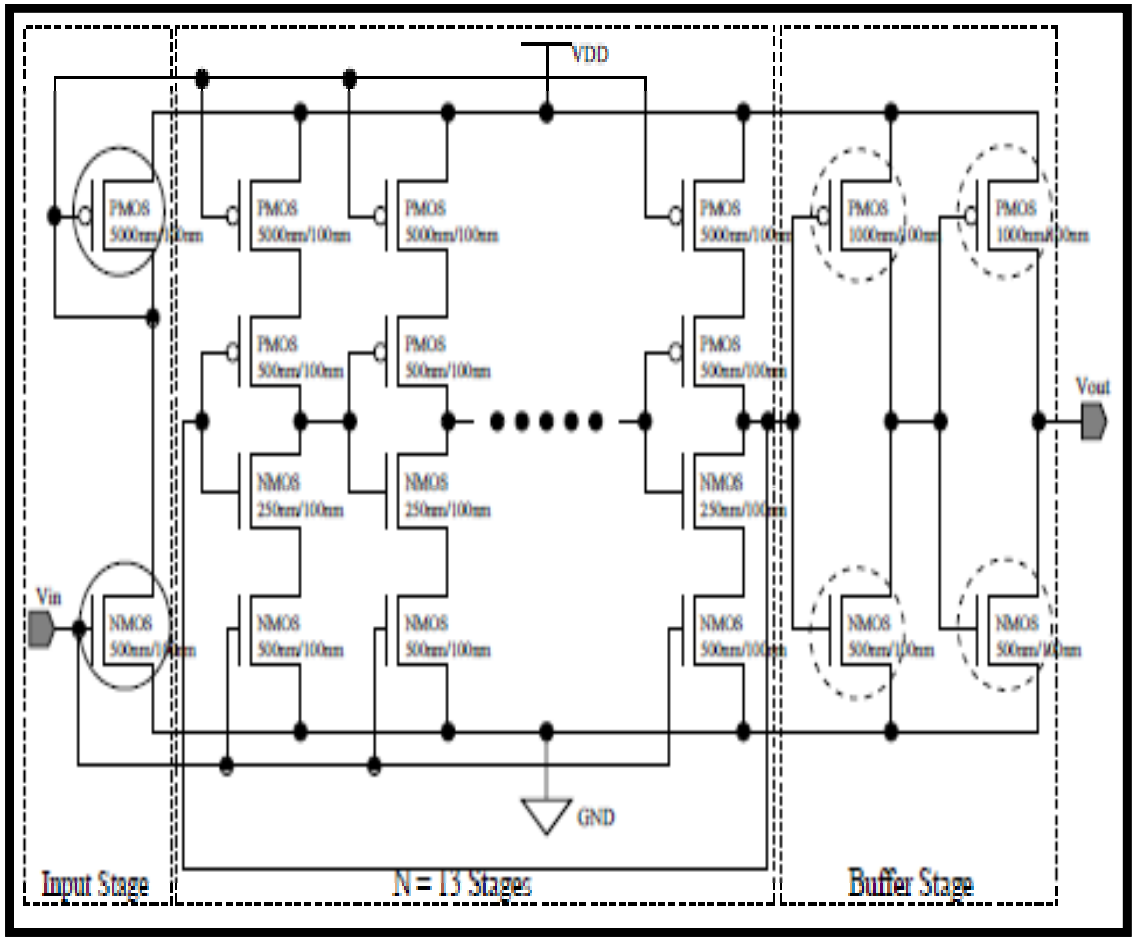
Dual-Threshold Assignment in VCO …

- Average power consumed by all the transistors is measured.
- Input stage transistors (shown by solid circles) consume 48% of total average power of the VCO circuit.
- Most suitable candidates for higher threshold voltage assignment (HV_{Thn}, HV_{Thp}).



Dual-Threshold Assignment in VCO

- The buffer stage transistors (shown by dashed circles) consume 11.5% of the total average power.
- May be treated to higher threshold voltage, for further power minimization.
- Input stage transistors follow *high threshold model file,* other transistors follow *baseline model file.*



Power-Performance Optimization in VCO …

- The parasitic aware netlist generated from the preliminary layout is parameterized with respect to the optimization parameter set D, which includes:
  - Widths of PMOS and NMOS devices in the inverter (Wn,Wp),
  - Widths of PMOS and NMOS devices in the current-starved circuitry (Wncs,Wpcs),
  - HV_{Thn}, HV_{Thp}.

Power-Performance Optimization

- The parameterized netlist is subjected to power-performance optimization using a conjugate gradient method.
- Our objective set are $f_0 \geq 2GHz$, and P_{VCO} = minimum.
- S is the stopping criteria for the optimization to stop when the objective set is within $\pm\varepsilon$.
- ε is a designer specified error percentage.

One Optimization Algorithm

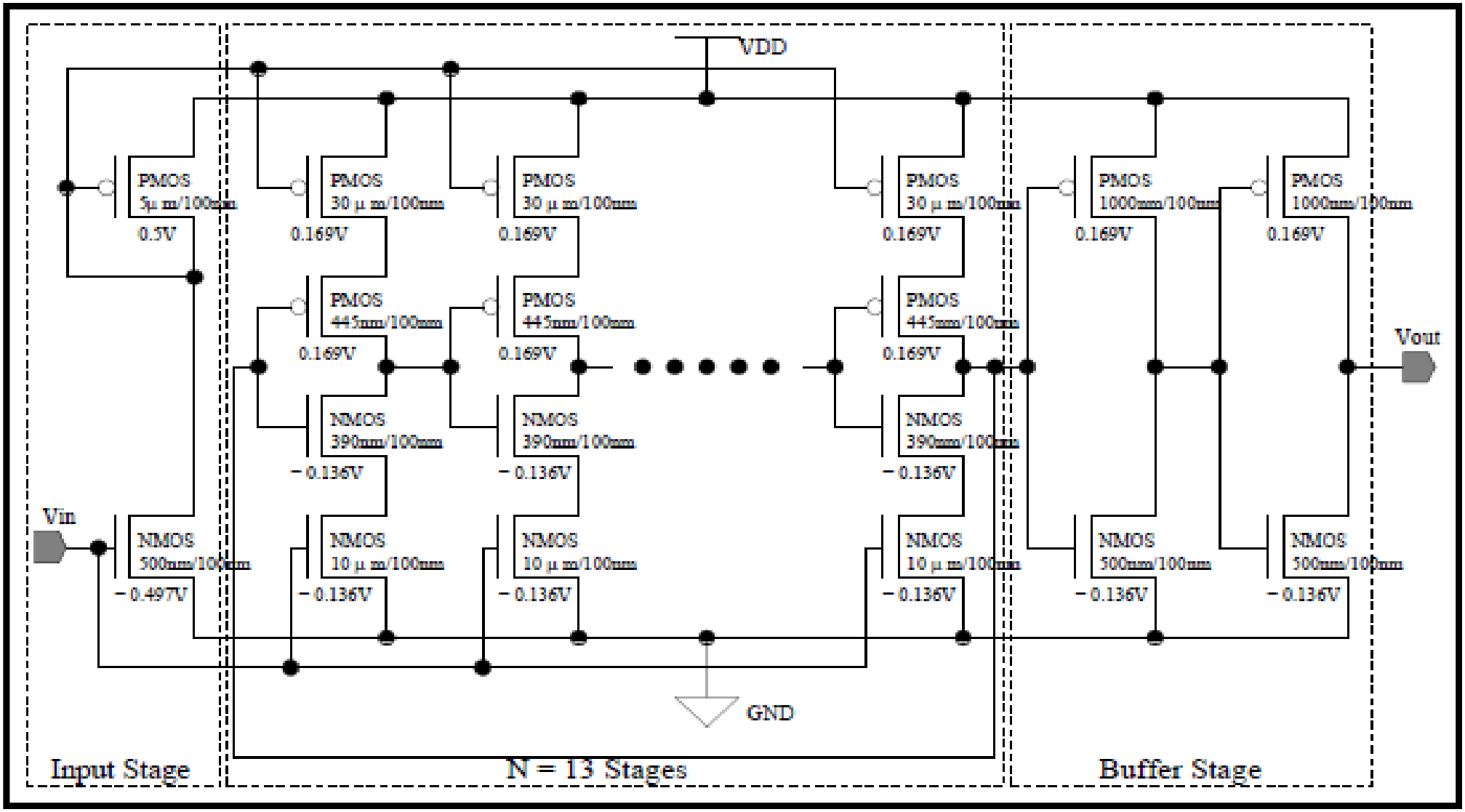
- **Input:** Parasitic aware netlist, Baseline model file, High threshold model file, Objective set $F = [f_0, P_{VCO}]$, Stopping criteria S, parameter set $D = [Wn, Wp, Wncs, Wpcs, HV_{Thn}, HV_{Thp}]$, Lower design constraint C_{low}, Upper design constraint C_{up}.
- **Output:** Optimized objective set F_{opt}, Optimal parameter set D_{opt} for $S \leq \pm\varepsilon$, {where ε=10%}.
- Perform first iteration with initial guess of D.
- **while** ($C_{low} < D < C_{up}$) **do**
  - Using conjugate gradient, generate $D' = D \pm \Delta D$ in the direction of travel of $F_{opt} \pm \varepsilon$.
  - Compute objective set $F(D') = [f_0, P_{VCO}]$.
  - Compute S as the difference of target objective set and current objective set.
  - **if** $S \leq \varepsilon$ **then**
    - {stopping criteria is within the error margin}
    - **return** $D_{opt} = D'$.
  - **end if**
- **end while**
- Using D_{opt}, construct final physical design and simulate.
- Record F_{opt} accounting the full-blown parasitics.

Optimization Results

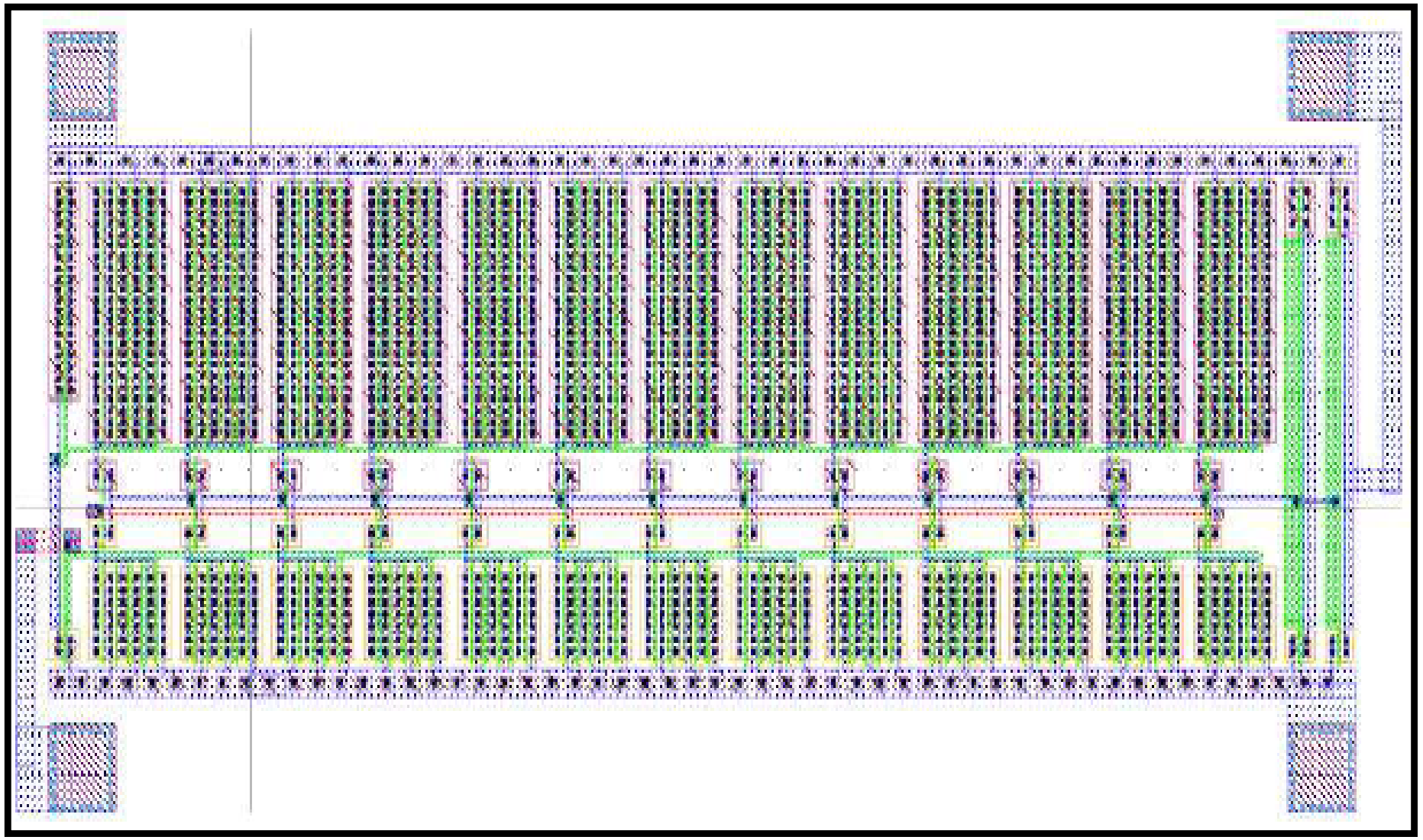
- Target center frequency $f_0 \geq 2GHz$.
- Final Physical design center frequency $f_{0p} = 2.4GHz$.
- Final Physical design center frequency in a worst case PVT conditions $f_{0pvt} = 1.8GHz$ (10% discrepancy).
- Final average power consumption (including leakage) (P_{VCO}) = 137.5µW (16.4% reduction).

D	C_{low}	C_{up}	D_{opt}
Wn	200nm	500nm	390nm
Wp	400nm	1µm	445nm
Wncs	1µm	50µm	10µm
Wpcs	5µm	50µm	30µm
Toxpth	0.1692662V	0.5V	0.5V
Toxnth	-0.5V	-0.1359511V	-0.4975V

P4VT Optimal Dual-Threshold VCO Circuit



P4VT Optimal Dual-Threshold VCO Layout



P4VT-Aware Performance of VCO

Parameter	Value
Technology	$90nm$ CMOS $1P$ $9M$
Supply Voltage (V_{DD})	$1.2V$
Center frequency (Nominal PVT)	$2.4GHz$
Worst case PVT	V_{Th} (+10%), T_{ox} (+10%), V_{DD} (−10%), $125°C$
Center frequency (worst case PVT)	$1.8GHz$
Parameter set	6 (W_n, W_p, W_{ncs}, W_{pcs}, HV_{Thn}, HV_{Thp})
Number of objectives	2 ($f_0 \geq 2GHz$, P_{VCO}=$minimum$)
Area occupied	$547.74\mu m^2$ (58.3% penalty)

Summary and Conclusions …

- Design of a Power-Performance-Parasitic-Process-Voltage-Temperature (P4VT) optimal nano-CMOS VCO is proposed.
- The presented design flow is used on top of existing physical design tools.
- The center frequency treated as the target specification.
- The degradation of the center frequency due to worst-case PVT effects narrowed down from 50% to 10%.

Summary and Conclusions

- 16.4% power minimization is achieved using dual-threshold technique.
- The end product of the proposed design flow is a P4VT optimal dual-threshold VCO physical design that meets the functional specifications across entire temperature range.
- For future research, we plan to incorporate additional performance criteria to the optimization set, such as phase noise.


Thank you !