# Single Ended Static Random Access Memory for Low-$V_{dd}$, High-Speed Embedded Systems

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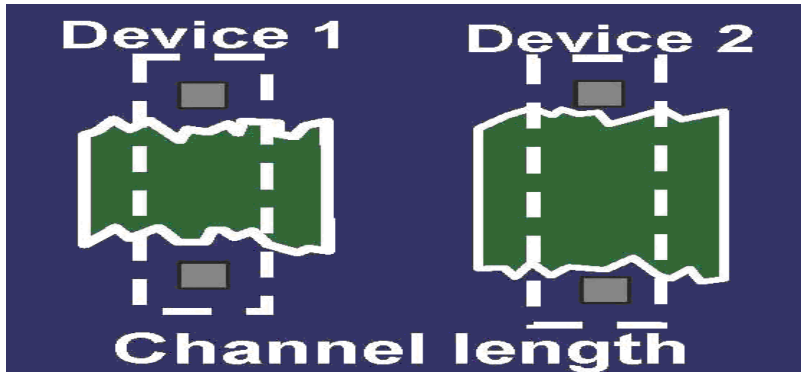
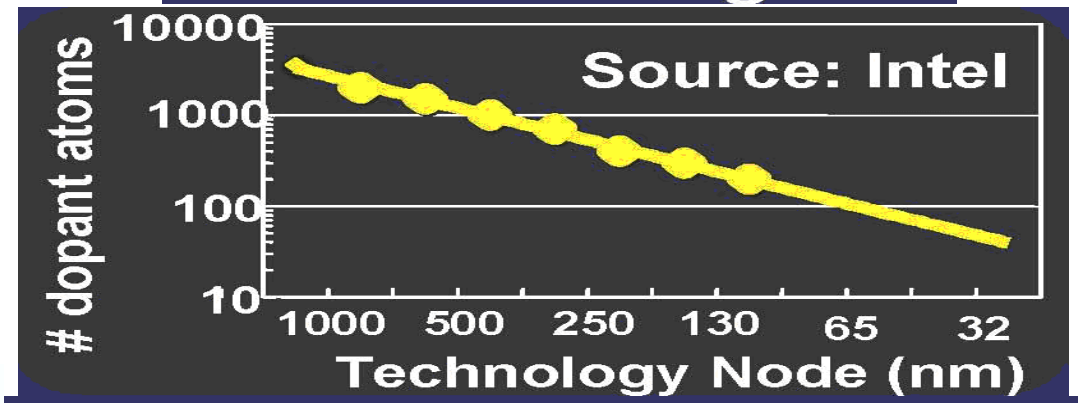
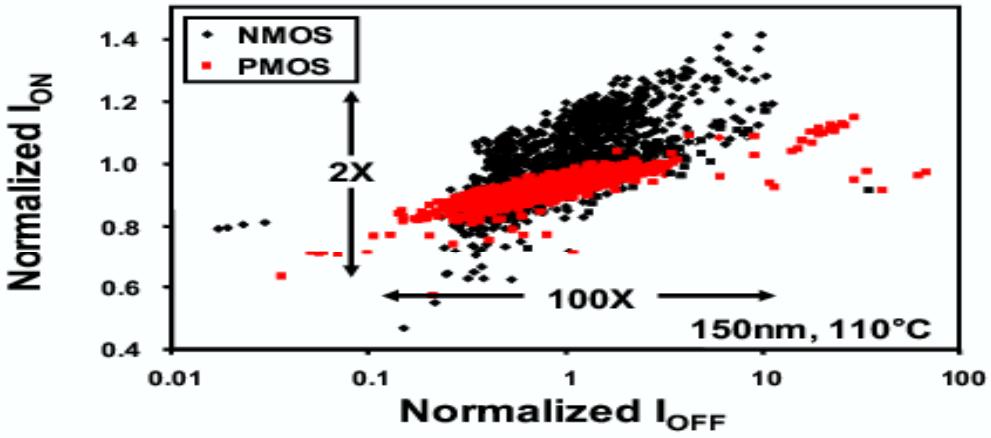
# Technology Scaling: Nano-Regime

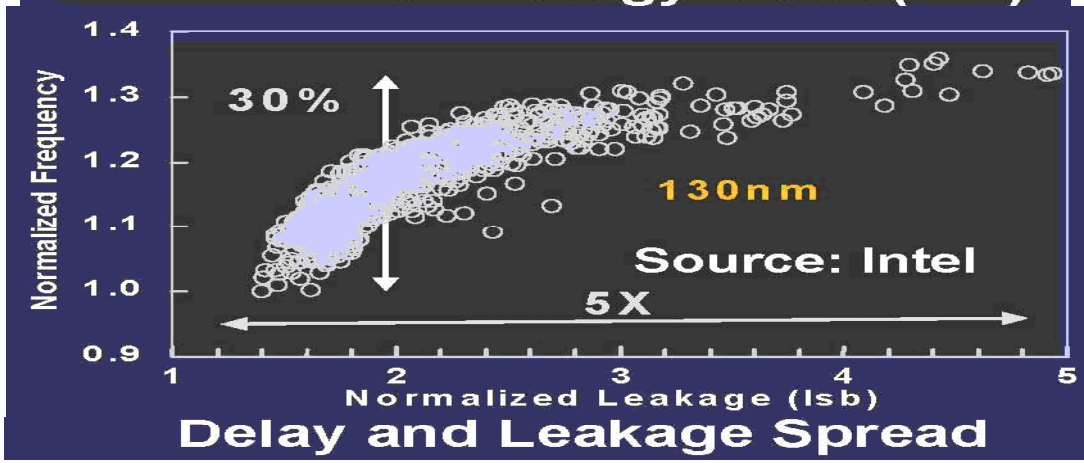
## Process variations affect:

- L: Channel Length
- $T_{ox}$: Gate Oxide Thickness
- $V_{th}$: Threshold Voltage
- # Dopant Atoms



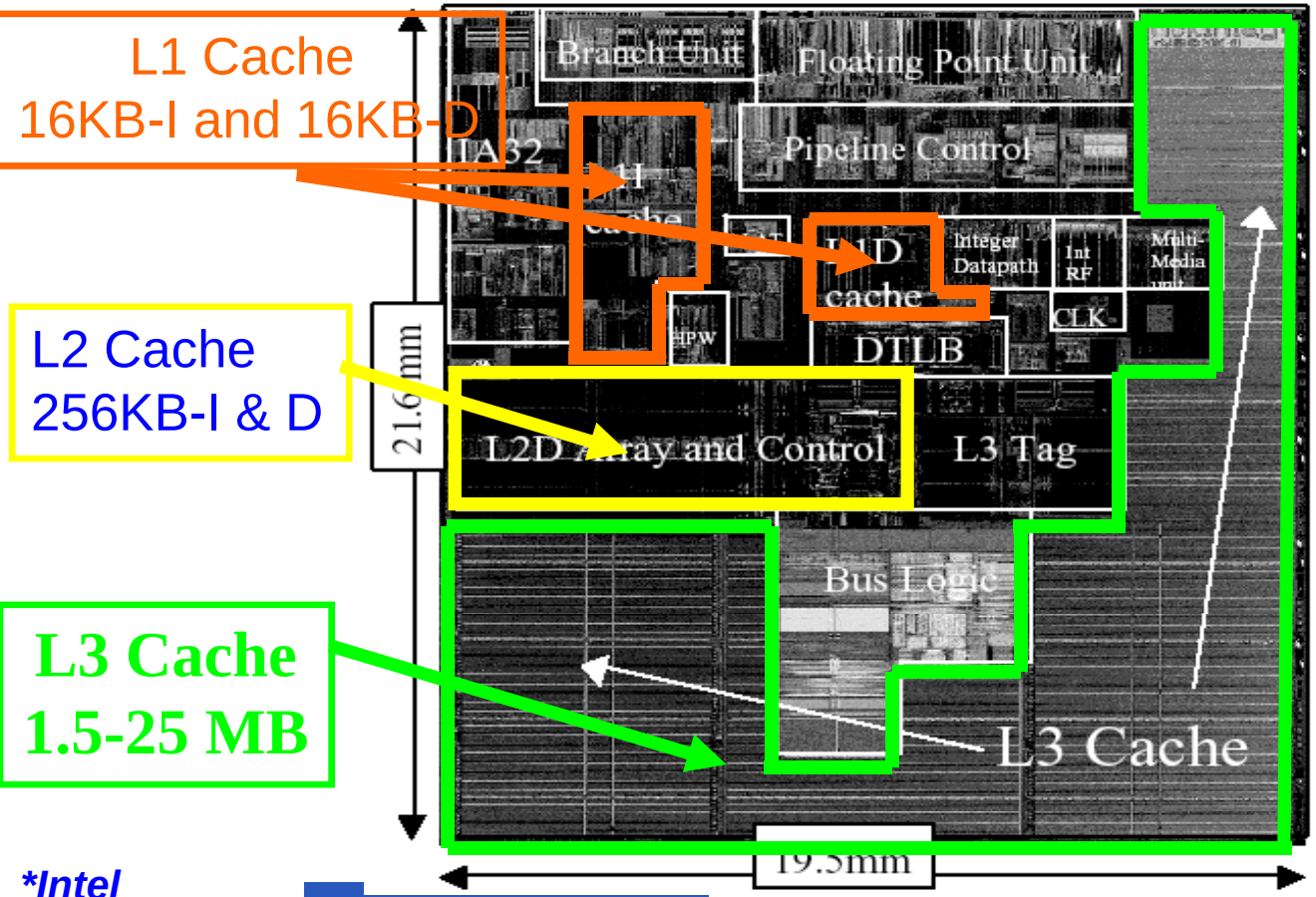



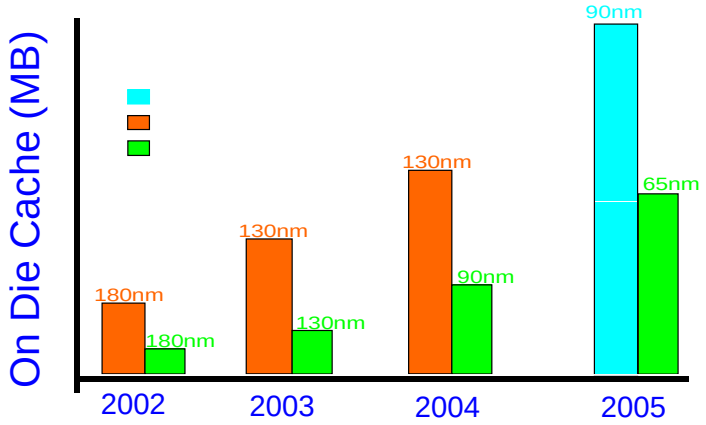
# Why Efficient SRAM Design?

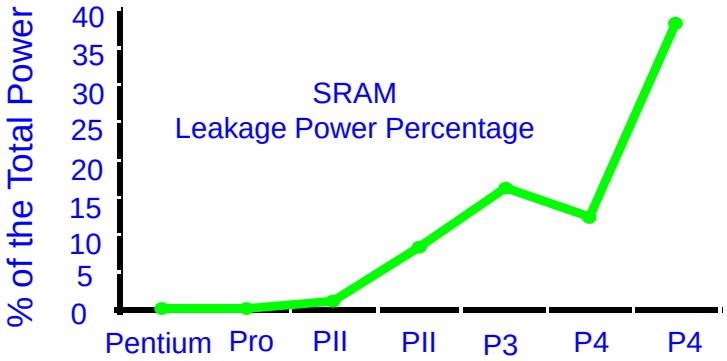
- Amount of on-die caches increases
- Up to 60% of the die area is devoted for caches in typical processor and embedded application.
- Largely contributes for leakage and power density.

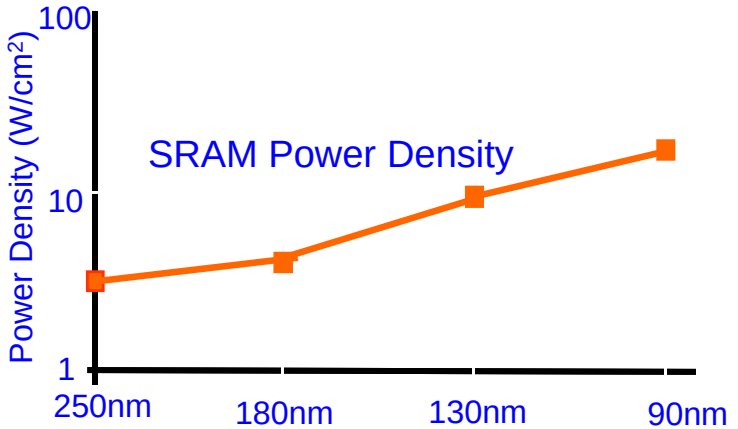
**Itanium 2* (L3-9MB) 130nm Technology**




*Intel




Single-Ended SRAM (SE-SRAM)



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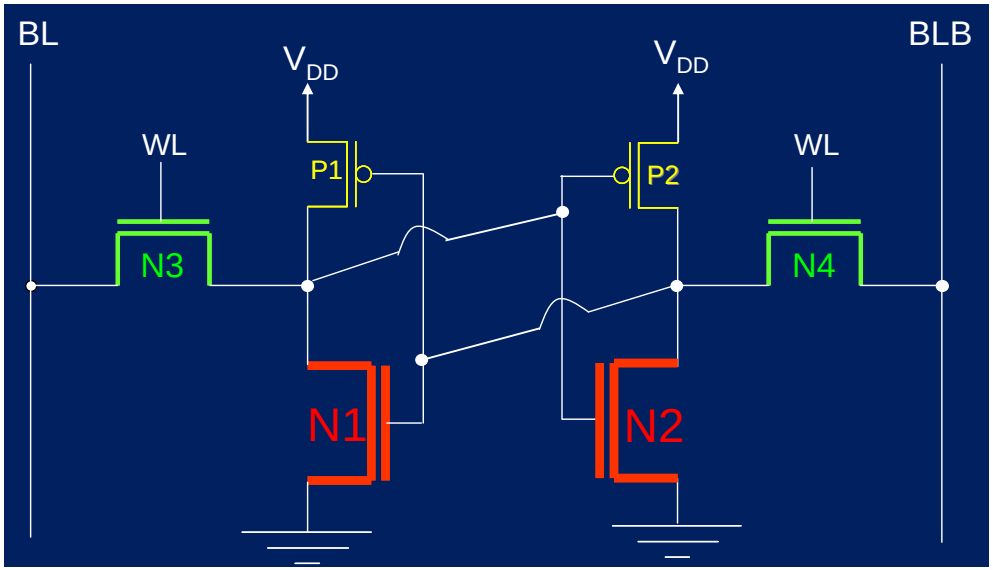
# Nano-CMOS SRAM Design Challenges ...

In nano-CMOS regime following are the major issues:

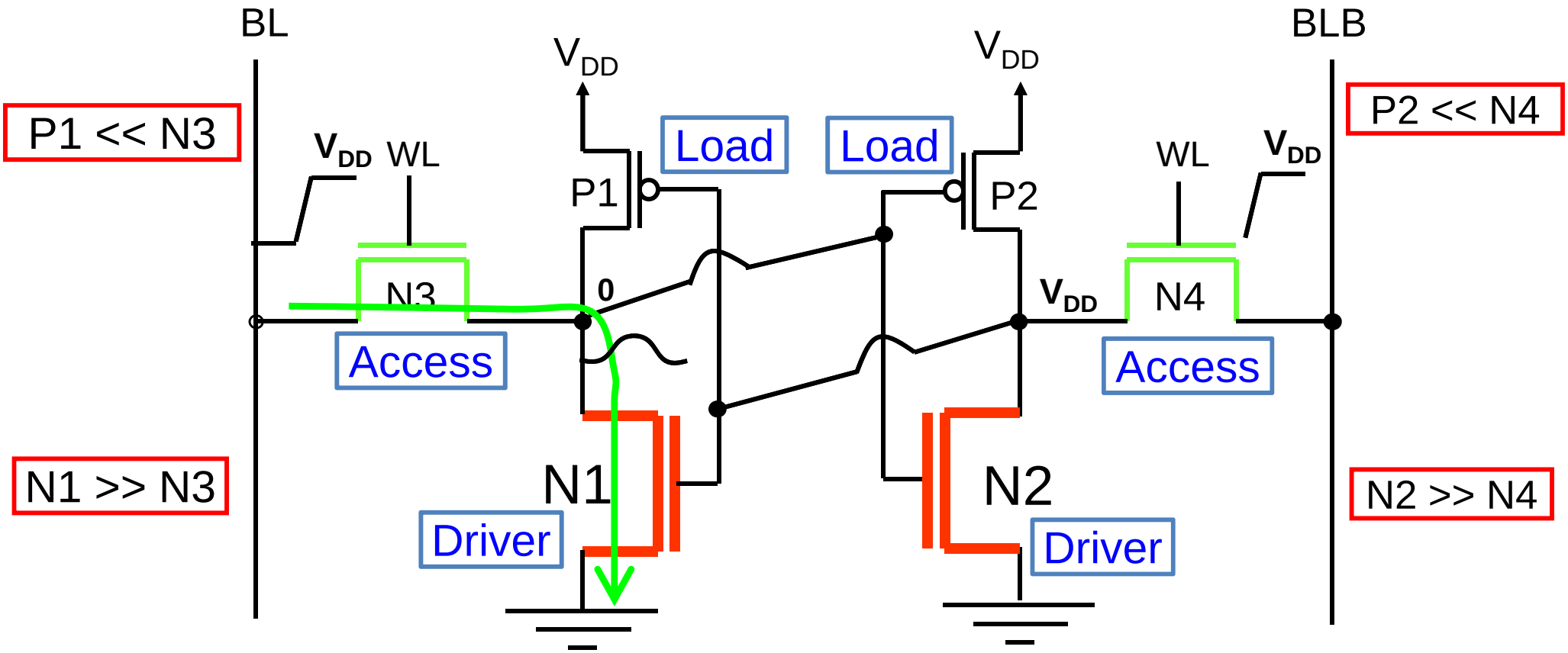
- Data stability and functionality
  - Non-destructive read
  - Successful write
  - Noise sensitivity
- Proper sizing of the transistors
  - To improve the write ability
  - To improve the read stability
  - To improve the data retention




6T-SRAM

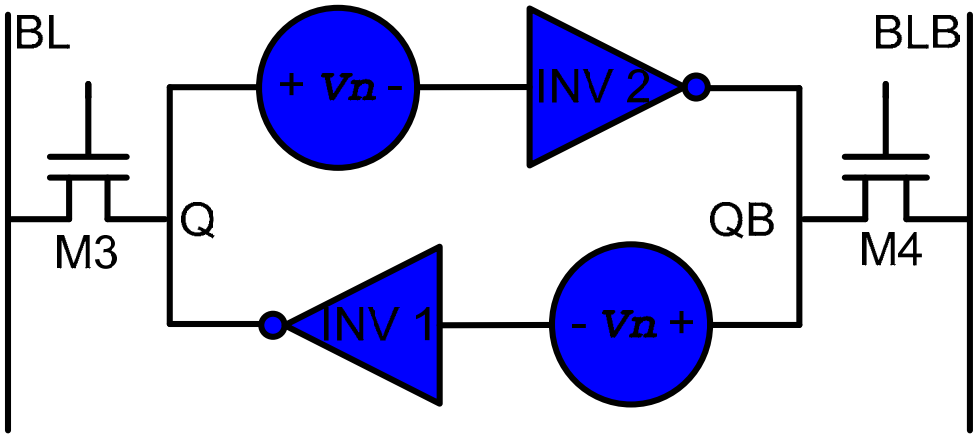
- Minimum size of transistors to maximize the memory density.
- Minimum leakage for low-power design.
- Minimum read access time to improve the performance.

# Nano-CMOS SRAM Design Challenges

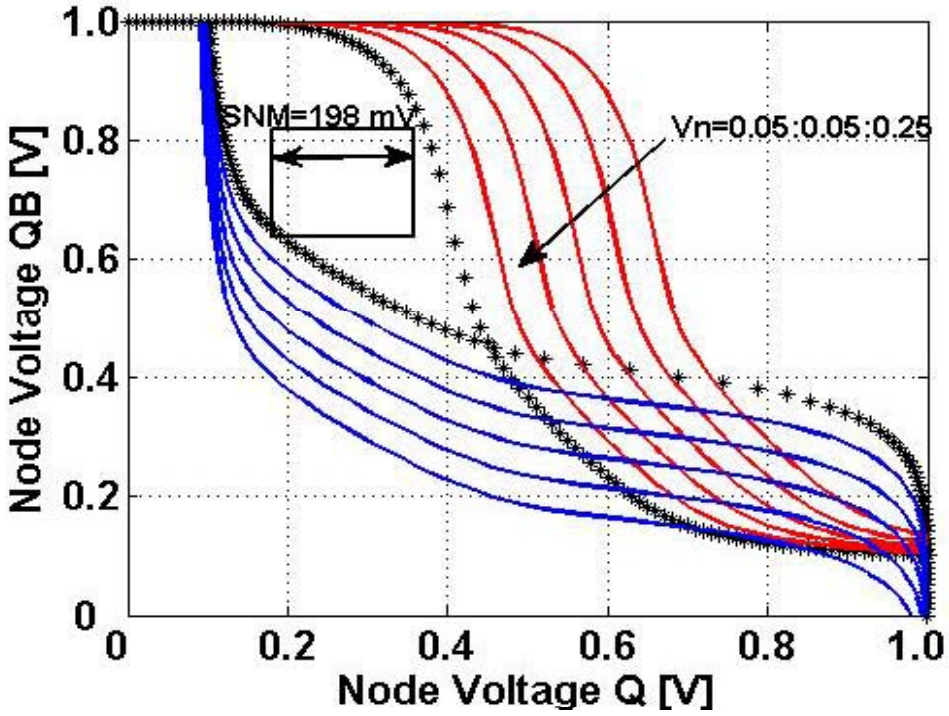



- For proper read stability: N1 and N2 are sized wider than N3 and N4.
- For successful write: N3 and N4 are sized wider than P1 and P2.
- Minimum sized transistors do not provide good stability and functionality.
- SRAM cell ratio ($\beta$): ratio of driver transistor's W/L to access transistor's W/L.

# Stability Analysis of SRAM ...



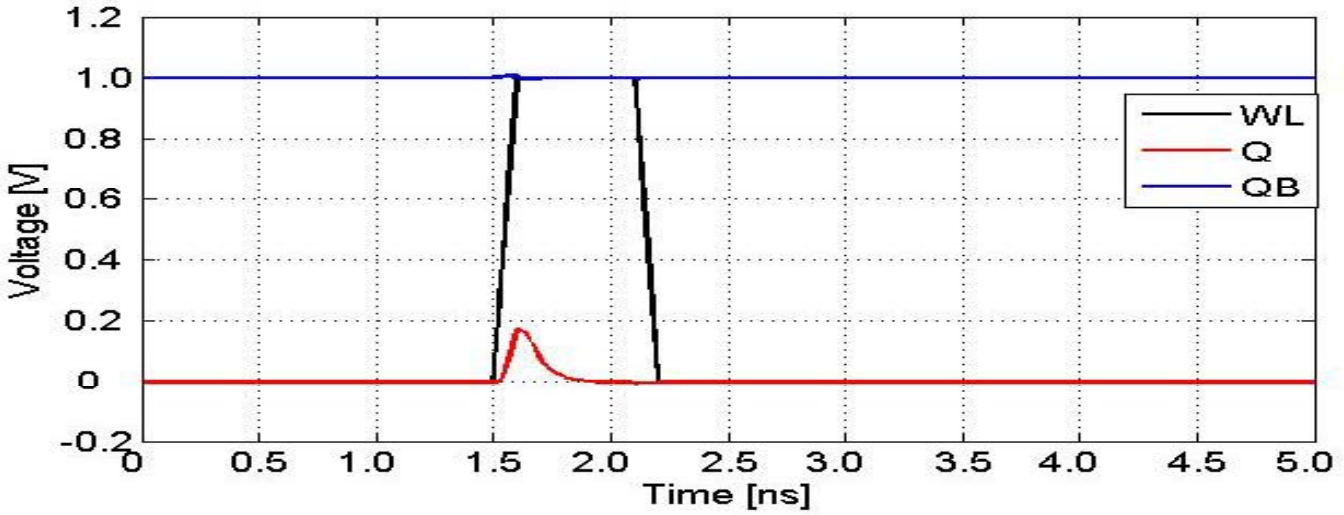

Noise model for stability analysis



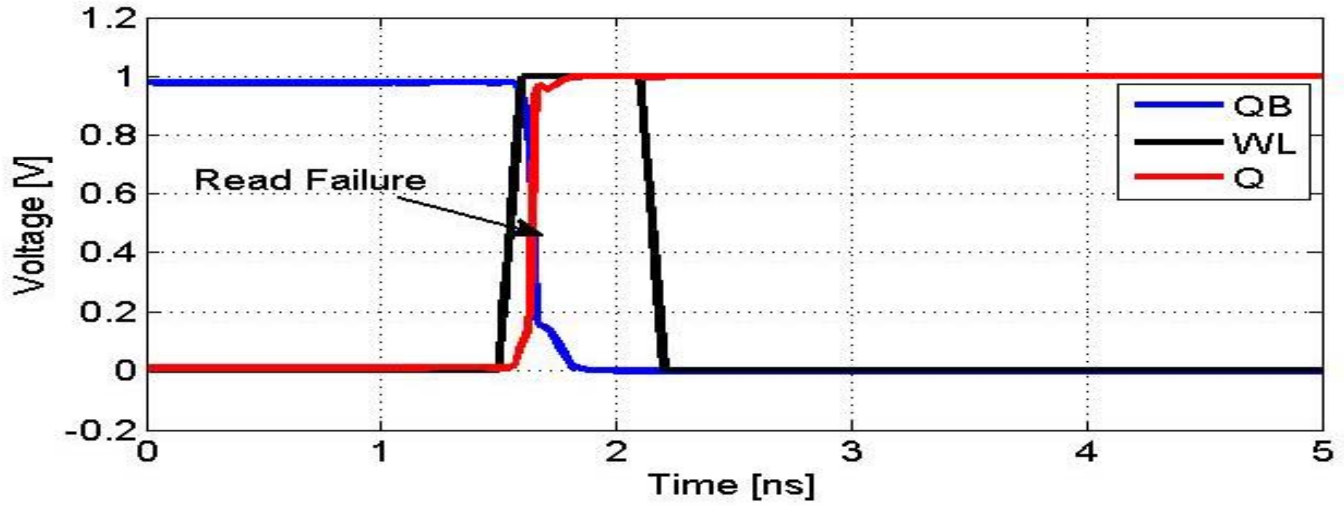

Voltage Transfer Characteristics (VTCs)

Static Noise Margin (SNM): The maximum DC noise voltage $V_n$ that can be tolerated by SRAM.

# Stability Analysis of SRAM



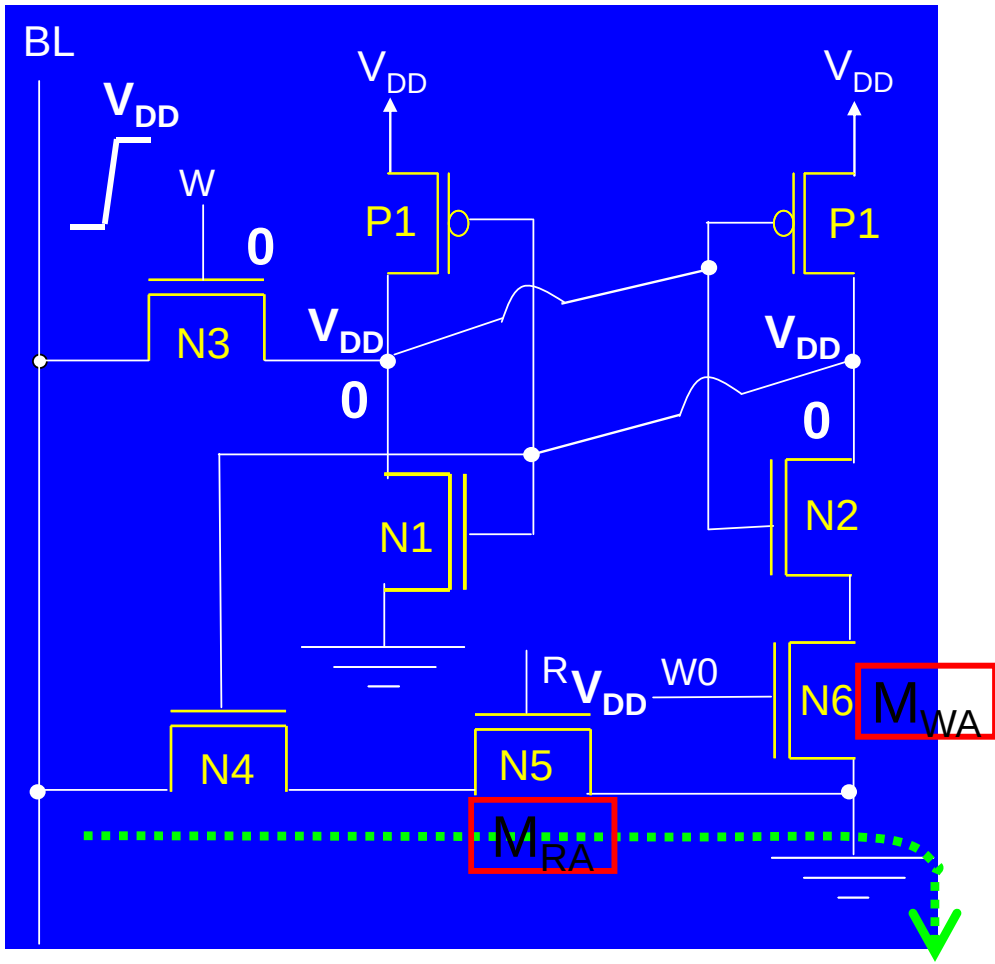

$V_n$ < 198mV: Successful Read




$V_n$ > 198mV: Destructive Read

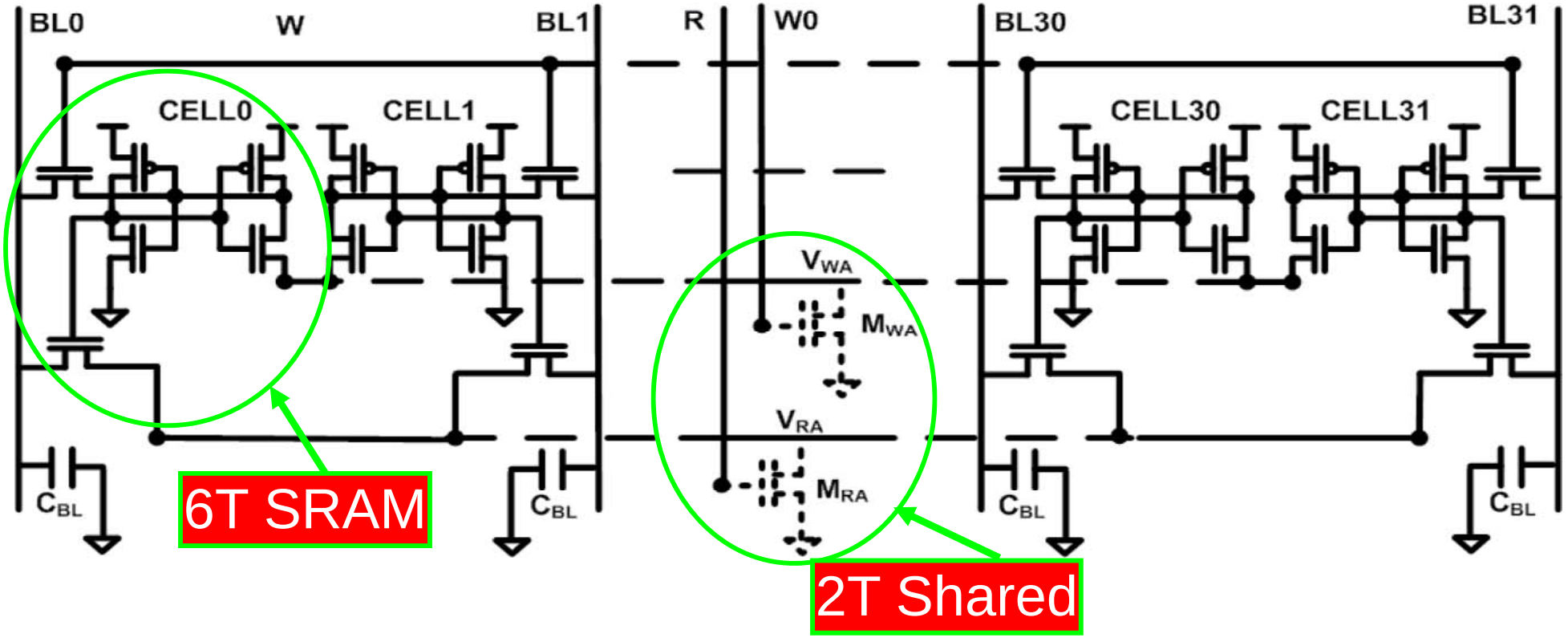
# The Proposed SE-SRAM

- Proposed single ended I/O 8T-SRAM cell design.
- In word oriented design it becomes 6T- SRAM design.
- Minimum size of transistors are used.
- Read Stability: For 0 and $V_{dd}$.
- No ratio contention.
- 3 signals: W, W0, R; W0 = $\overline{W}$. Read operation: R, Write operation: W and W0.



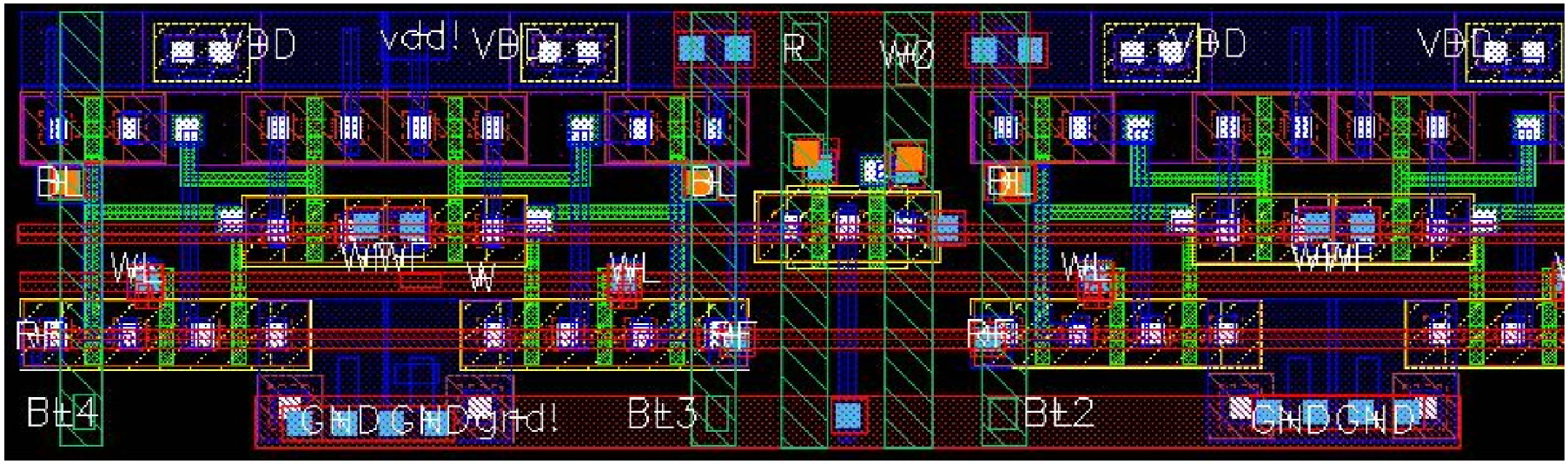

Reduction in dynamic power and leakage because of single ended input/output line and stacking of transistors, respectively.

# 32-Bit Word Organization Using SE-SRAM




- Word oriented design to reduce area and power overhead.
- 6T-SRAM cell with 2T shared among the word cells.
- Read/Write assist transistors are shared by all bits of a word as all 32 bits are accesses simultaneously.
- Wider word will provide better area saving.

# Physical Design of a Proposed 32-bit Word




4-bit array shown for clarity

- Bitcell Area: 0.68μm² (0.55μm x 1.22μm).
- 8% higher than standard 6T SRAM.
- Read/write assist transistors half roughly half of a bitcell area per a memory word.
- A 32-bit layout was designed and parasitics were extracted.

# Read/Write Assist Transistors Sizing

- The amount of current flowing through the read assist transistor:

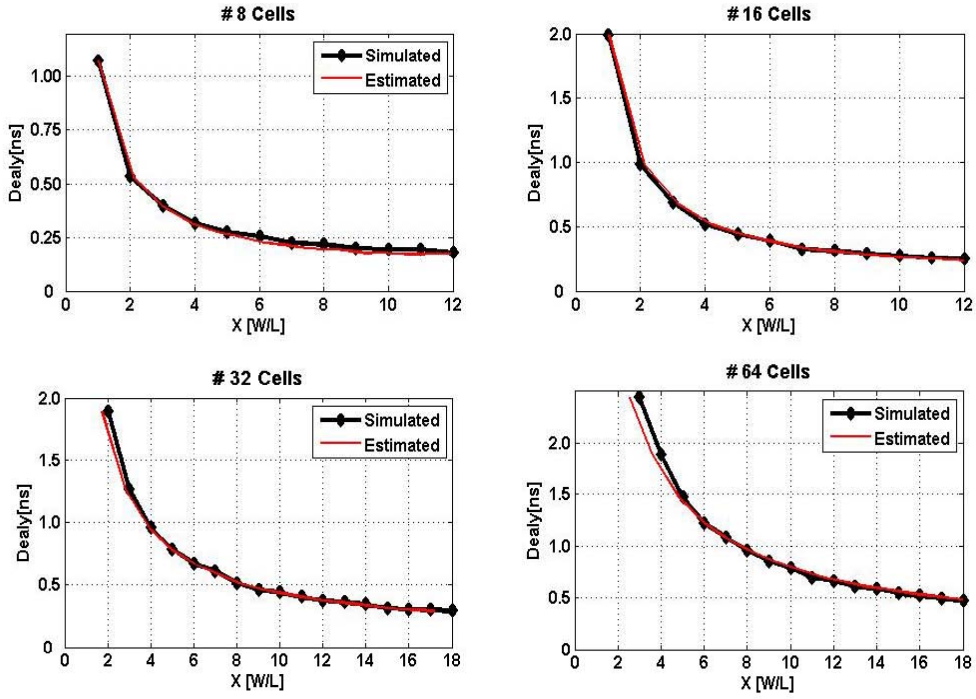
$$I_{RA} \approx \mu_n C_{ox} \left(\frac{W}{L}\right)_{RA} (V_{dd} - V_{th}) V_{RA}$$

- Voltage at the node $V_{RA}$ is

$$V_{RA} = V_{dd} \exp\left(\frac{-t}{\tau}\right)$$

Where, $\tau_d = R_{RA} C_{BL}$ and $\tau_d = \tau$

when voltage at node $V_{RA}$ is 0.36 $V_{dd}$



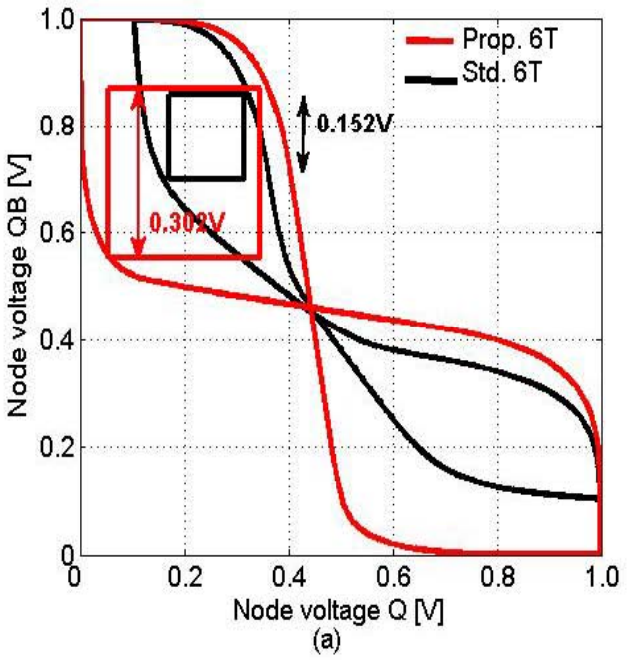

- Hence, size of the read assist $M_{RA}$

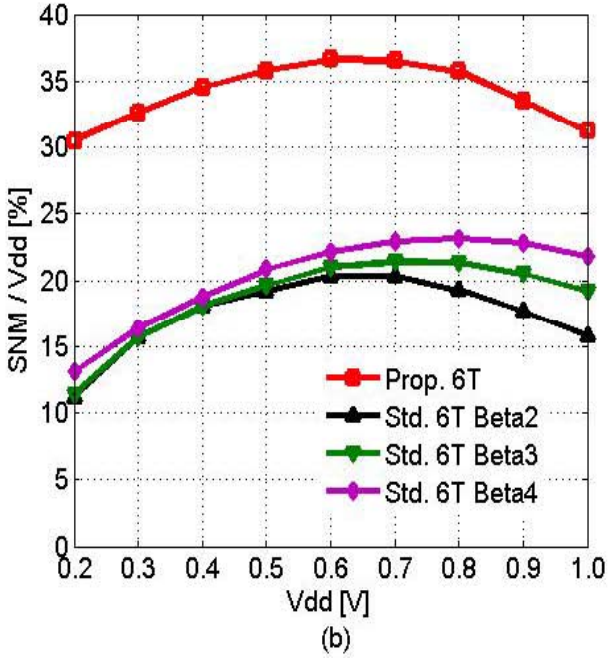
$$\left(\frac{W}{L}\right)_{RA} = \frac{1}{R_{RA}\mu_n C_{ox}(V_{dd} - V_{th})}$$

- Size of the write assist $M_{WA}$: A single equivalent minimum size transistor per word for minimum leakage and data retention.

# Stability Analysis of SE-SRAM ...

- SNM of traditional SRAM and proposed SE-SRAM.
- Under normal read operation.
- For traditional SRAM cell ratio = 2.
- For proposed SE-SRAM minimum size transistors.

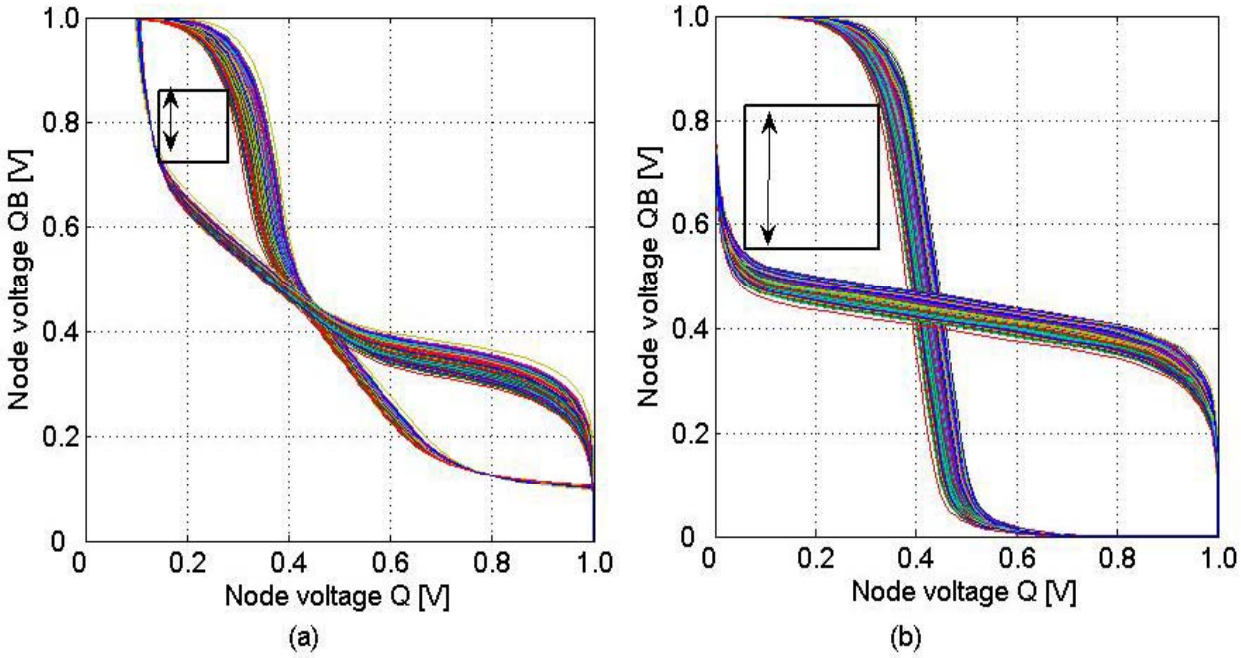



- Proposed cell has 2X higher SNM than the standard cell at beta = 2 and $V_{dd}$ =1.0V.
- For subthreshold operation proposed cell SNM is equal to stdard cell at beta=4 and $V_{dd}$ =0.5V.

# Stability Analysis of SE-SRAM

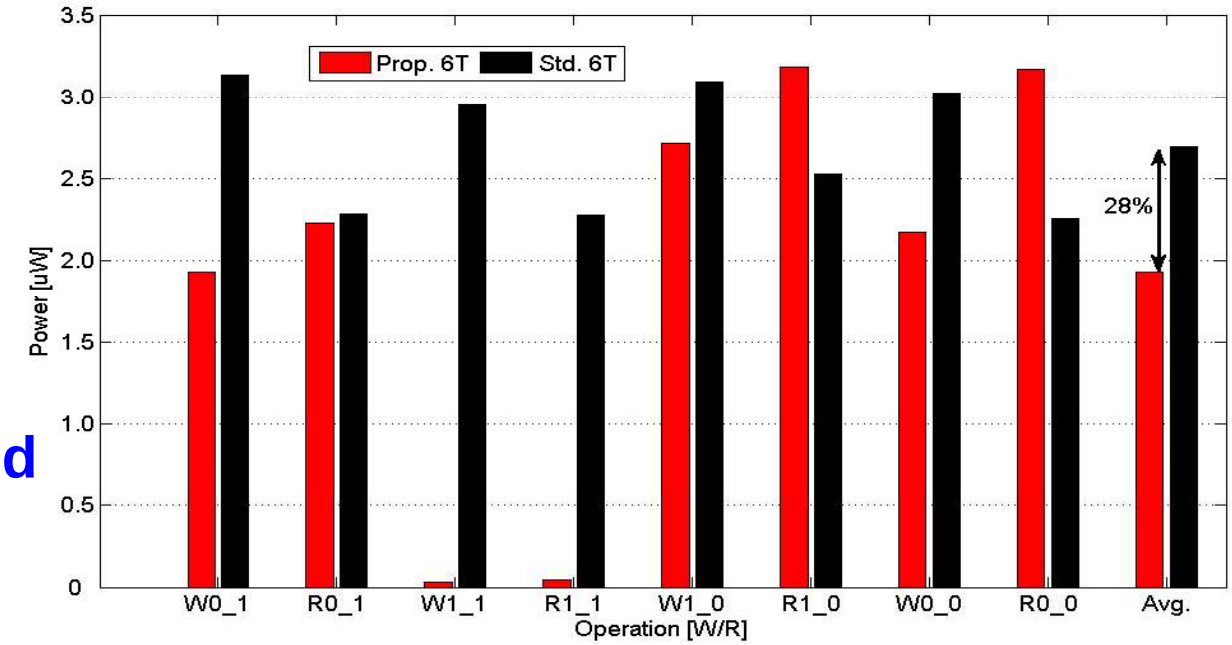
- SNM of standard SRAM and the proposed SE-SRAM.
- Read operation under process variations in $V_{th}$.
- For traditional SRAM, cell ratio =2.
- For prop. 6T minimum size transistors




- For the worst case prop. cell has 2.65X higher SNM than the standard cell at beta=2 and $V_{dd}$ =1.0V.
- The worst case standard deviation in the SNM for proposed cell is 11% higher than the standard cell at beta=2 and $V_{dd}$ =1.0V.

# Active Power Dissipation of SE-SRAM

- Active power of standard and proposed SRAMs.
- For all possible read and write operations at $V_{dd}$=1.0V.
- Power pattern is asymmetrical for proposed SE-SRAM, because of asymmetric r/w operation or its structure.




- If the upcoming datum is same either for read of write operation (W1_1 or R1_1) the proposed SRAM has low power consumptions compared standard.
- If the upcoming datum is zero during read operation (R1_0 or R0_0) proposed design has 21% and 29% higher power than the standard SRAM.
- Average active power in the proposed design is 28% lower than the standard.

# Conclusions

- The proposed SE-SRAM design achieves 2.65X better static noise margin compared to a standard 6T-SRAM.
- Improved write-ability of logic ‘1’.
- Minimum feature size devices.
- No radioed contention or tuning of cell ratio
- Saving of active and leakage power.
- One disadvantage: A marginally high standard deviation in the SNM and active and leakage power due to minimum sized device.

# Thank You