A Universal Level Converter Towards the Realization of Energy Efficient Implantable Drug Delivery Nano-Electro-Mechanical-Systems

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Outline of the Talk

- Introduction and Contributions
- Proposed Drug Delivery Nano-Electro-Mechanical Systems (DDNEMS)
- The Universal Voltage-Level Converter (ULC)
- Power and Delay Optimization of the ULC
- Related Research
- Characterization of the ULC
- Conclusions and Future Research

Introduction

- Nano-Electro-Mechanical Systems (NEMS) are a technological solution for building miniature systems which can be beneficial in terms of safety, efficacy, or convenience.
- NEMS based drug delivery (DDNEMS) is meant to administer drugs to pre-determined targets in the body through implantable chips, which are controlled or programmed externally through a radio frequency interface.
- DDNEMS should have the following attributes:
  - Low power consumption
  - Fault tolerance
  - Re-configurability and field upgradability

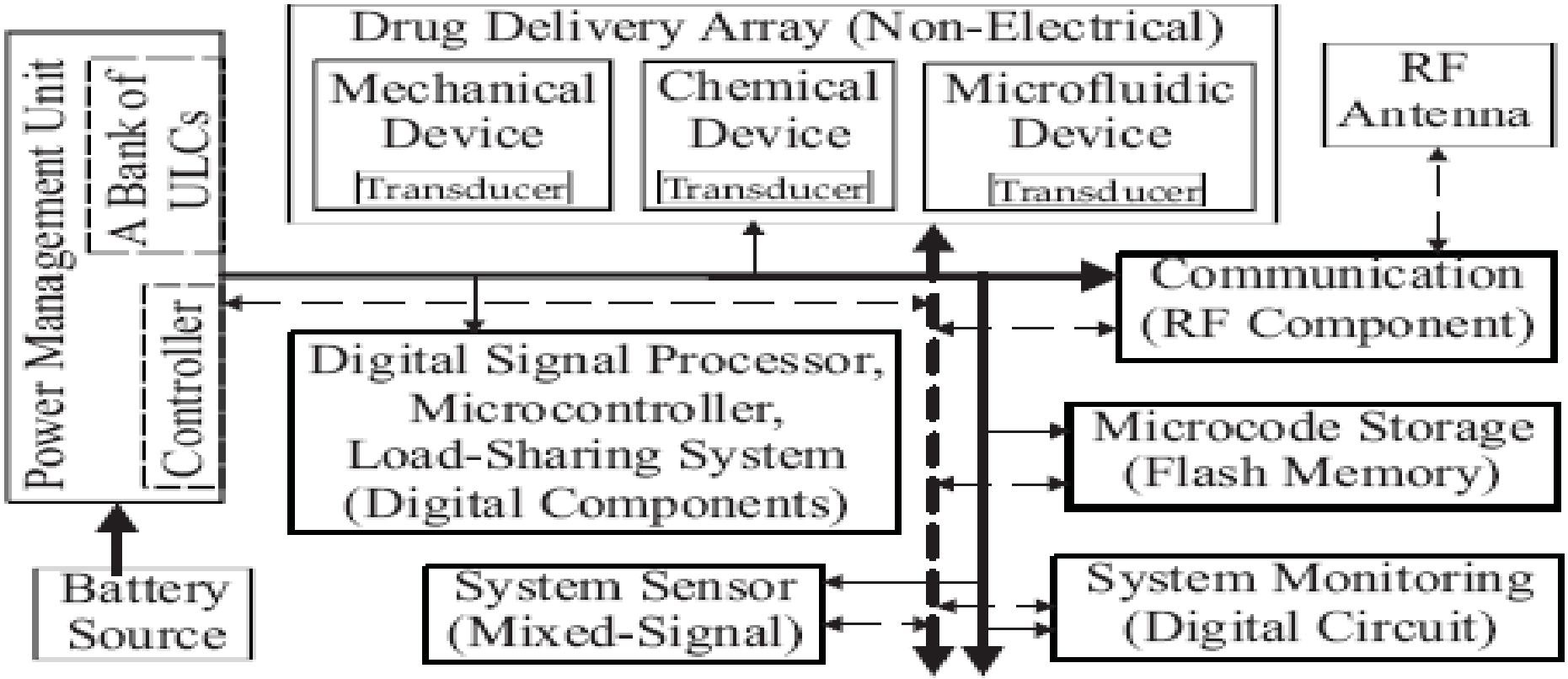
Introduction

- DDNEMS can be realized as system-on-chip (SoC) while supplied with power from a single battery source.
- There is need for devising integrated power management methods to reduce power consumption in DDNEMS.
- We propose a special type of level converter, called Universal Level Converter (ULC), suitable for power management and field programmability of DDNEMS.
- ULC designed using cutting-edge high-κ/ metal-gate Dual-V_{Th} nano-CMOS 32nm technology.
- High-κ is used to contain the gate leakage, and Dual-V_{Th} technology reduces the subthreshold leakage.

Contributions

- A novel implantable system called DDNEMS, which can be realized as a multicore analog/mixed-signal SoC (AMS-SoC) along with nonelectrical components for programmable drug delivery is introduced.
- The key components as well as challenges of DDNEMS design are identified.
- In order to serve the most pressing challenge, the power dissipation, we introduce the universal voltage-level converter (ULC).
- A novel design flow for energy efficient design of a ULC circuit is proposed.
- A 32nm high-κ/ metal-gate (HKMG) CMOS ULC has been implemented and thoroughly characterized.
- An algorithm is presented for the simultaneous power, leakage, and delay optimization of the 32nm ULC.
- A dual−V_{Th} technique has been applied to this HKMG ULC for power and delay optimization.

Proposed DDNEMS



- Solid-lines represent power bus.
- Dotted-lines represent data and control buses.

DDNEMS Components: PMU

- Power Management Unit (PMU):
  - Manages the power distribution to the various subsystems to optimize energy consumption.
  - Has built-in timers that put the system to "sleep" or "wake-up" mode and can be induced to activate the system via external signals received by the RF subsystem (to force an emergency drug delivery, for example).
  - *The heart of PMU is a bank of ULCs. ULC sends different* operating voltages to various subsystems of DDNEMS each of which operate at different voltages from a *single battery* and facilitates reconfigurability.

DDNEMS Components: DDA

- Drug Delivery Array (DDA):
  - Typically non-electrical in nature.
  - The sub-sytem is designed as an array to allow redundancy, fault tolerance, load sharing and multiple drugs.
  - The array could be homogeneous (all elements of the same kind) or heterogeneous.
  - Micropumps, microfluidic devices, stents, and microneedles to be designed in the design phase.
  - Appropriate transducers needed to allow control and interfacing array elements to the electronic portion of the DDNEMS.

DDNEMS Components: Electrical Components

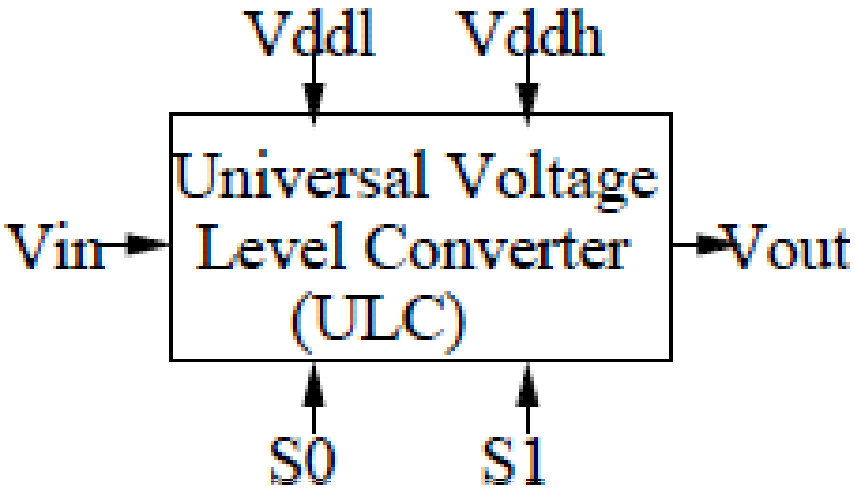
- Electrical Components (DSP, Sensors, Memory etc):
  - Sensor subsystem performs the monitoring and control of the drug array elements, which receives information from, and sends control signals to the transducers.
  - Front-end (transducer side) is analog but the back-end, interfacing to the DSP is digital.
  - The DSP subsystem analyzes the on-line data generated by the sensors and, under the control of the program stored in the flash memory subsystem, generates control signals to control drug delivery, facilitate fault tolerance, load sharing, and drug mixing.
  - The system monitoring subsystem continually polls the various electrical subsystems and transducers to obtain a snapshot of the overall system's health.
  - Upon the discovery of faults or errors, it alerts the DSP for appropriate action.

DDNEMS Components: RF Components

- Radio Frequency Components (RF):
  - Comprises of an antenna and transmitter/receiver.
  - Can be built using RFID principles for the shape and placement of the antenna and communication protocol.
  - Allows non-invasive maintenance of the system (modification of the microcode stored in the flash memory, for example),
  - Does remote collection of data (such as amount of drug remaining in the reservoir, drug array element failures, battery status etc.),
  - Facilitates emergency drug delivery or system deactivation.

The Universal Voltage-Level Converter (ULC)

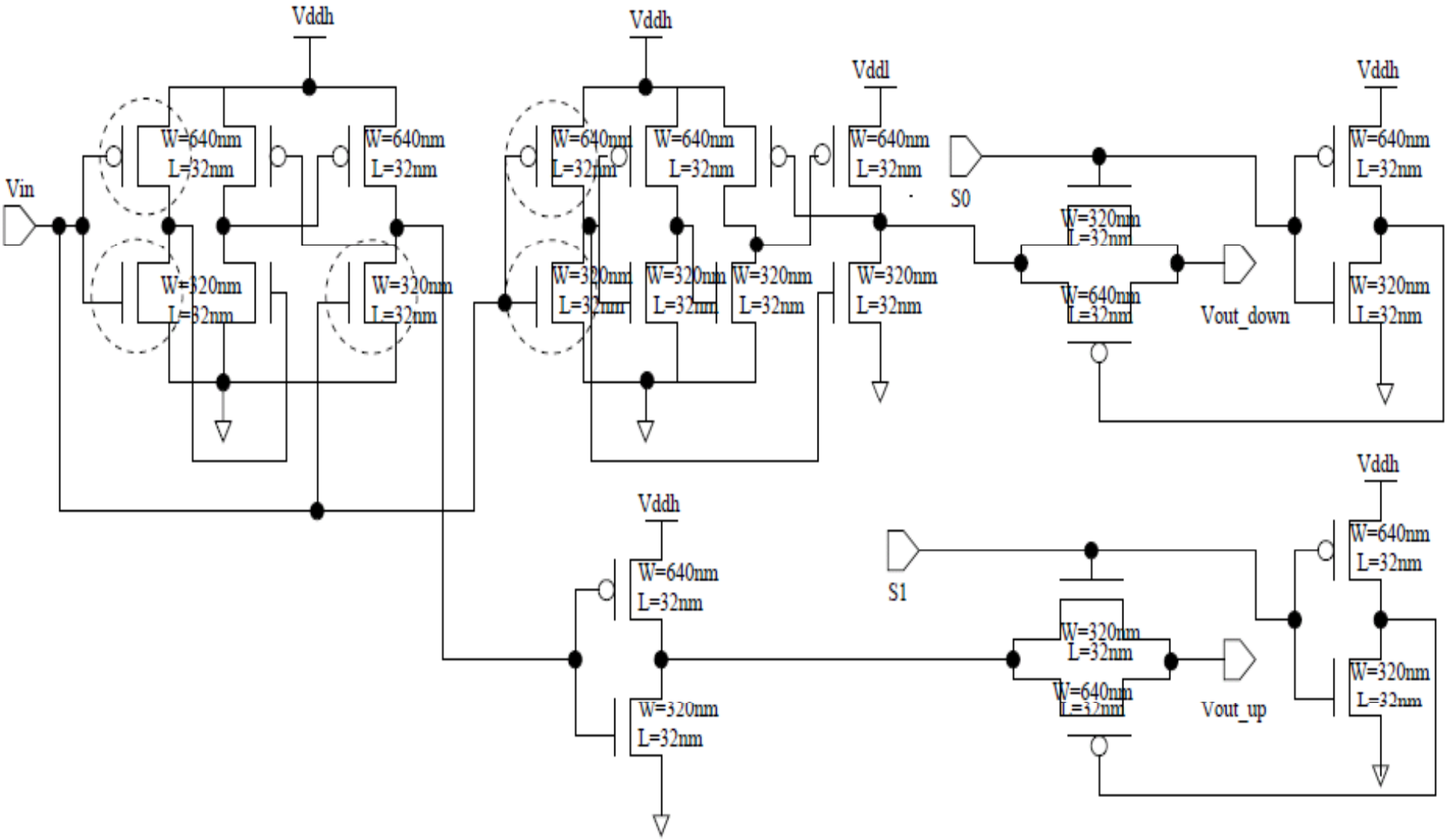
- The ULC consists of:
  - Input voltage signal V_{in}
  - Control signals S1 and S0
  - Supply voltages V_{ddl}, V_{ddh}
  - Output voltage signal V_{out}



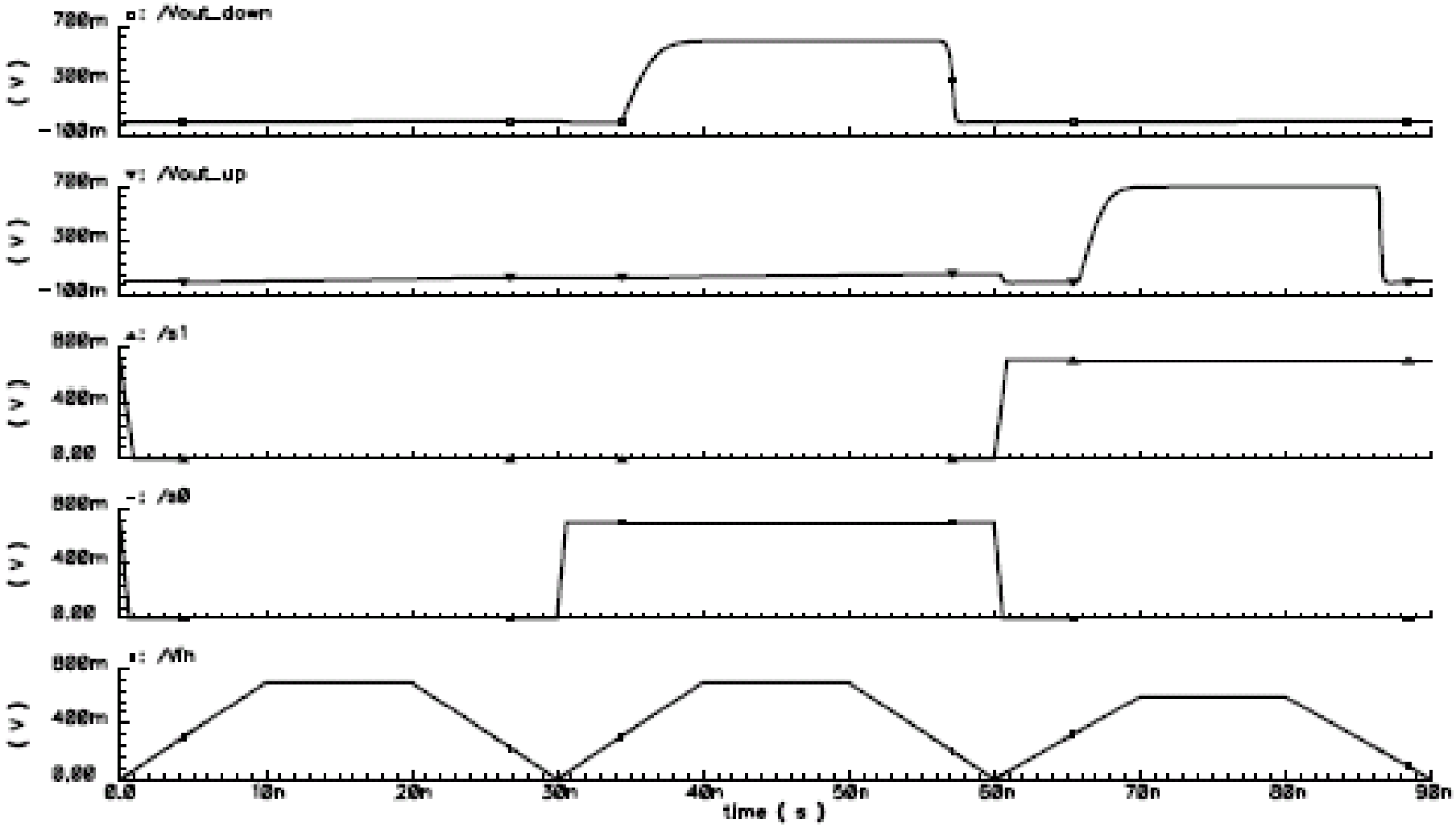
- Operations of the ULC:
  - Level-up conversion
  - Level-down conversion
  - Blocking of input signal

Select Signal		Type of Operation
0	0	Block Signal
0	1	Down Conversion
1	0	Up Conversion

The Universal Voltage-Level Converter (ULC)



The Universal Voltage-Level Converter (ULC)



High-κ Metal Gate Modeling of ULC

- 32 nm high-κ/ metal gate (HKMG) Predictive Technology Model (PTM) is used for modeling transistors of ULC (http://www.eas.asu.edu/~ptm/).
- Two methods are used: (1) The model parameter in the model card that denotes relative permittivity (EPSROX) is changed or (2) The equivalent oxide thickness (EOT) for the dielectric under consideration is calculated.
- The EOT is calculated by the formula:

$$EOT = \left(\frac{\kappa_{SiO_2}}{\kappa_{gate}} \right) * t_{gate}$$

- κ_{gate} is the relative permittivity and t_{gate} is the thickness of the gate dielectric material other than SiO_2.
- κ_{SiO2} is the dielectric constant of SiO_2 (= 3.9). We have taken κ_{gate}=21 and t_{gate}=5 nm to emulate a HfO_2 based dielectric. EOT is calculated to be 0.9 nm.

Power and Delay Optimization of ULC

- Power-hungry transistors are identified and are assigned higher V_{Th} values.
- Power-hungry NMOS are assigned 20% higher V_{Th} and power hungry PMOS are assigned 50% higher V_{Th} compared to the nominal values
- Design variable set for Optimization:
  - W_{PMOSup}: width of PMOS transistors in level-up converter
  - W_{NMOSup}: width of NMOS transistors in level-up converter
  - $W_{PMOSdown}$: width of PMOS transistors in level-down converter
  - $W_{NMOSdown}$: width of NMOS transistors in level-down converter

Power and Delay Optimization of ULC

1: **Input:** Circuit netlist, Objective set F, Stopping criteria S, design variable set D, Lower design constraint C_{lower}, Upper design constraint C_{upper}.

2: **Output:** Optimized objective set $F_{optimized}$, Optimal design variable set $D_{optimal}$ for $S = \pm \beta$, {where $1\% \leq \beta \leq 5\%$}.

3: Run initial simulation in order to obtain feasible values of design variables for the given specifications.

4: **while** ($C_{lower} < D < C_{upper}$) **do** {Loop outputs optimal design variable set $D_{optimal}$}

5: Using conjugate gradient method, generate new set of design variables

$D' = D \pm \delta D$.

6: Compute objective set $F(D') = [P_{ULC}, Delay_{ULC}]$.

7: **if** ($S == \pm \beta$) **then**

8: return $D_{optimal} = D'$.

9: **end if**

10: **end while**

11: Obtain optimal values for design variable set $D_{optimal}$, and simulate.

12: Record objective set $F_{optimized}$ for the ULC.

Power and Delay Optimization of ULC

Parameter	C_{lower}	C_{upper}	$D_{optimal}$
W_{PMOSup}	64 nm	640 nm	64 nm
W_{NMOSup}	64 nm	640 nm	640 nm
$W_{PMOSdown}$	64 nm	640 nm	64 nm
$W_{NMOSdown}$	64 nm	640 nm	640 nm

Objective	Value
P_{ULC}	5 μW
$Delay_{ULC}$	1.6 ns

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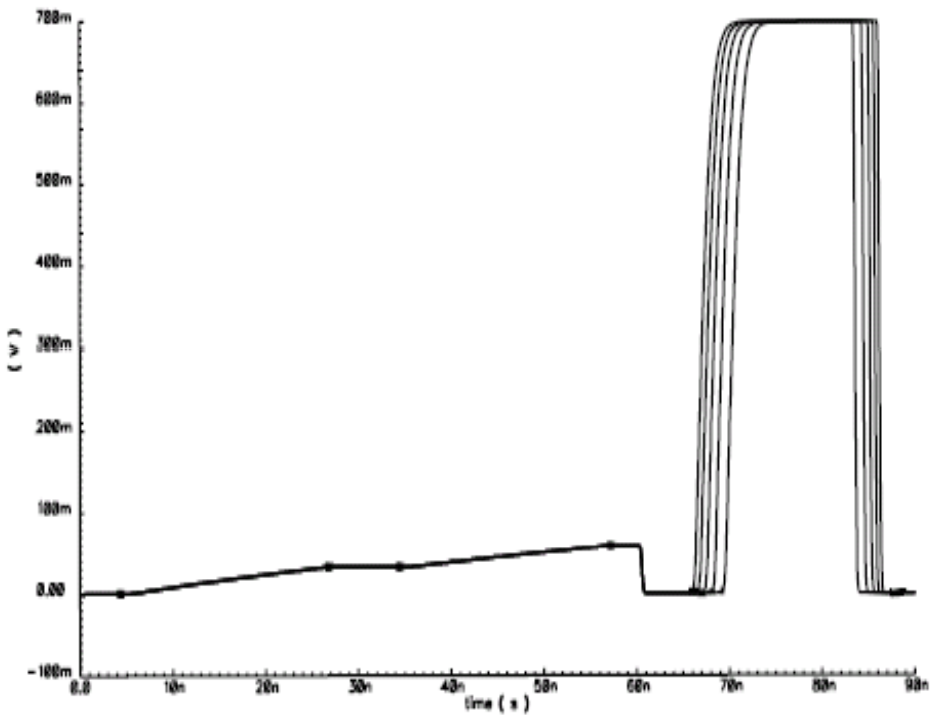
Related Research

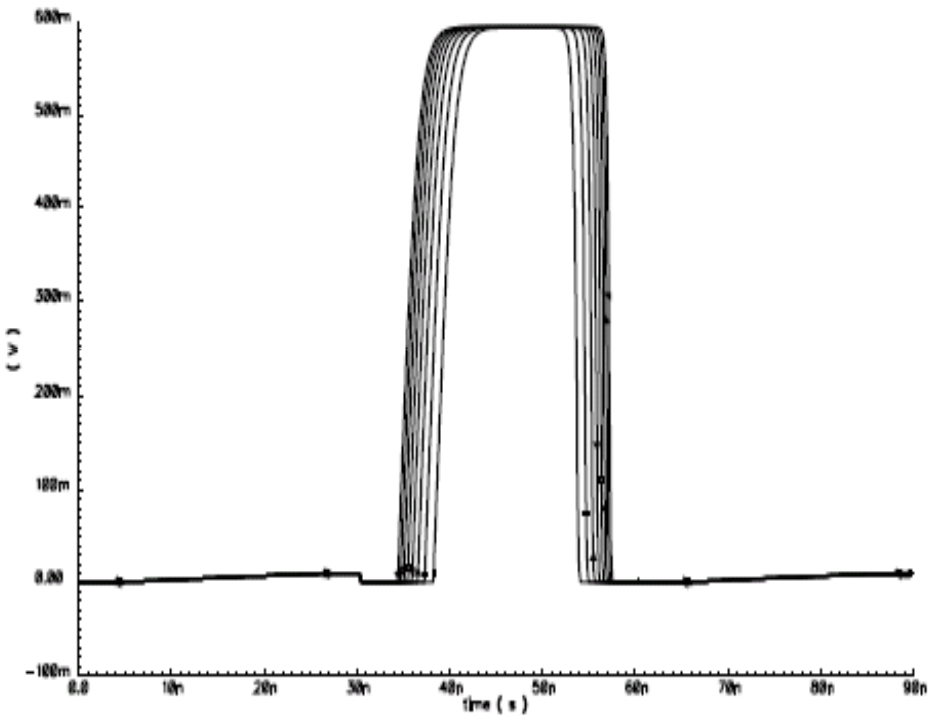
Works	Tech. (nm)	Power	Delay	Conversion
Ishihara	Bulk 130 nm	---	127ps	Level-up and down
Yu	Bulk 350 nm	220.57µW	---	Level-up
Sadeghi	Bulk 100 nm	10µW	1ns	Level-up
Kanno	Bulk 140 nm	---	5 ns	Level-down
This Work	**High-κ 32 nm**	**5 µW**	**1.6 ns**	**Level-up/down and block**

Characterization of the ULC

- Parametric Analysis:



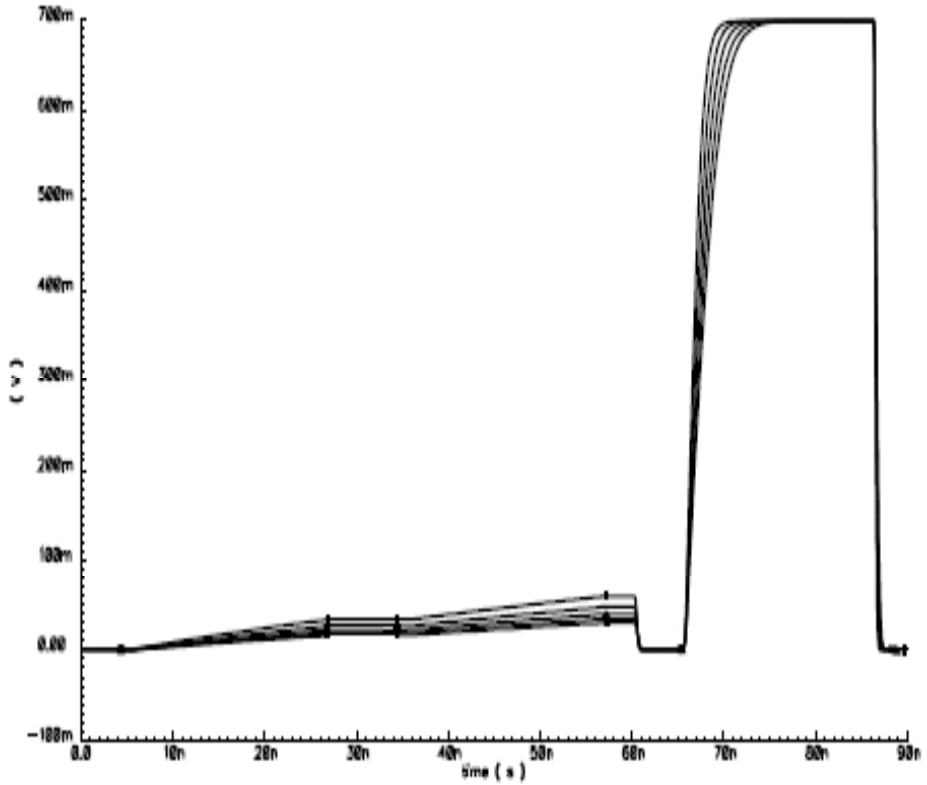
(a) For level-up conversion



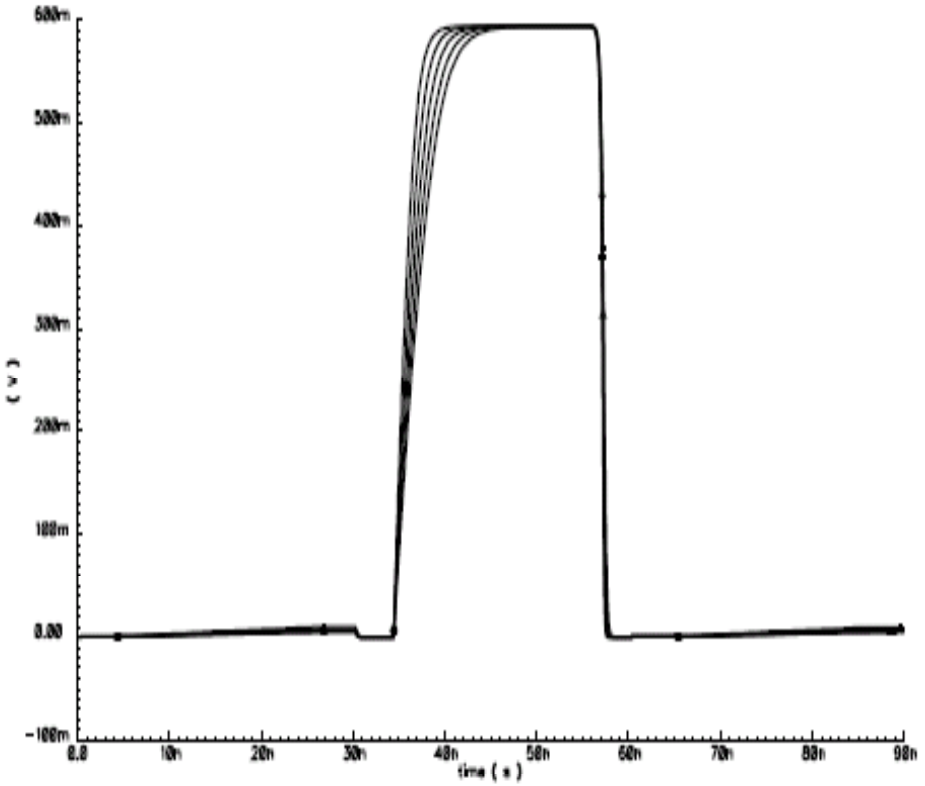
(b) For level-down conversion

Characterization of the ULC

- Load Analysis:



(a) For level-up conversion



(b) For level-down conversion

Characterization of the ULC

- Power Analysis:

Input Rise/Fall Time (ns)	Input Switching Freq. (MHz)	Capacitive Load (fF)	Avg. Power Consumption (μW)
10	33.33	50	4.988
10	33.33	82	5
10	33.33	120	5.8

Conclusions

- A novel design called ULC for is proposed for DDNEMS architecture.
- The ULC is capable of performing up-conversion, down-conversion and blocking.
- An HKMG design of the ULC is presented. This ULC is subjected to further power minimization by applying a dual-V_{Th} technique.
- An algorithm is discussed and adapted for the power and delay optimization of the entire ULC circuit.
- The robustness of the ULC is tested using parametric, load and power analysis.
- First ever reported level converter implementation using 32 nm HKMG nano-CMOS.

Future Research

- Future research will consider gate-induced junction leakage (GIDL) in the optimization process.
- Design of the ULC using other nanoscale technologies, such as double gate FET (DGFET), Carbon Nano-Tube FET (CNTFET) and analyze the effects on the performance metrics.


Thank you !!