A PVT-Aware Accurate Statistical Logic Library for High-κ Metal-Gate Nano-CMOS

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Acknowledgment: This work is partially supported by NSF award number 0702361.

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Outline of Talk

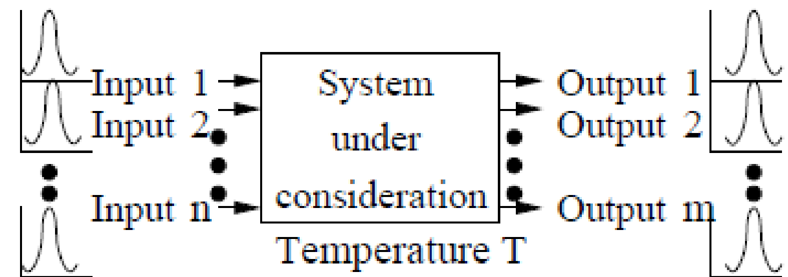
- Introduction and Contributions
- Related Prior Research
- Proposed Methodology for HKMG Logic Library
- Variation-Aware HKMG Device Characterization
- Variation-Aware State Dependent HKMG Logic Level Characterization
- PVT-Aware HKMG Logic Level Characterization
- Conclusions and Future Research

Introduction

- Success of the semiconductor industry relies on the continuous improvement of IC performance by device scaling.
- Scaling of SiO_2 gate-oxide thickness leads to tunneling gate leakage.
- A gate insulator with a higher dielectric constant κ than that of SiO_2 (=3.9) and metal gate (high-κ metal-gate (HKMG) nano-CMOS) reduces the gate leakage and improves the reliability of the gate.
- HKMG suffers from I_{sub}: subthreshold leakage and I_{GIDL}: gate-induced drain leakage.

Introduction

- Major sources of variability in nano-CMOS:
  - Process Variation (P)
  - Supply Voltage (V), and
  - Operating Temperature (T).
- It is necessary to express the effect of PVT variability on power, leakage and delay: $\hat{Y} = f\,(P, V, T)$ where $\hat{Y}$ is power, leakage or delay.
- We propose a Monte Carlo based technique to create a PVT aware library.



Contributions

- A methodology for HKMG logic library creation is presented.
- The effect of process variations has been considered during logic library creation.
- Device level characterization of HKMG NMOS and PMOS transistors is presented.
- A HKMG logic library with statistical characterization at room temperature (27 °C) is presented.
- A PVT aware HKMG statistical logic library is presented

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Related Prior Research

- Sundareswaran-ISQED2008,Mohanty-VLSID2007: Statistical characterization of logic gates as function of process parameter variations.
- Rastogi-JETTA2008:Rapid Library characterization for specific operating conditions.
- Basu-ISQED2008: Existing standard CMOS Logic Libraries.
- There is a need for characterized standard cells for non-classical CMOS technologies.

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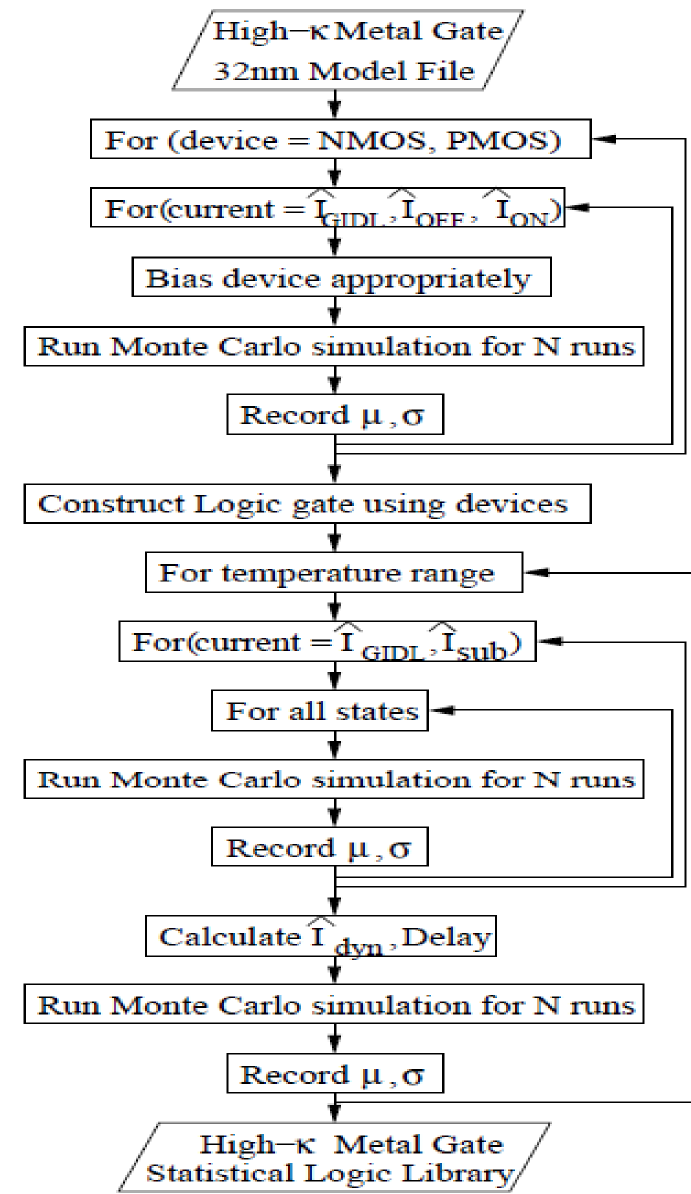
Proposed Methodology for HKMG Logic Library

- Variability: The 15 Device Parameters

(1) V_{dd}: supply voltage.
(2) V_{Thn}: NMOS threshold voltage.
(3) V_{Thp}: PMOS threshold voltage.
(4) t_{gaten}: NMOS gate dielectric thickness.
(5) t_{gatep}: PMOS gate dielectric thickness.
(6) L_{effn}: NMOS channel length.
(7) L_{effp}: PMOS channel length.
(8) W_{effn}: NMOS channel width.
(9) W_{effp}: PMOS channel width.
(10) N_{gaten}: NMOS gate doping concentration.
(11) N_{gatep}: PMOS gate doping concentration.
(12) N_{chn}: NMOS channel doping concentration.
(13) N_{chp}: PMOS channel doping concentration.
(14) N_{sdn}: NMOS source/ drain doping concentration.
(15) N_{sdp}: NMOS source/ drain doping concentration.

Proposed Methodology for HKMG Logic Library

- The input to the design flow is a 32 nm HKMG model file.
- First step: statistical characterization at device level i.e. NMOS and PMOS for $\hat{I}_{GIDL}$, $\hat{I}_{OFF}$ and $\hat{I}_{ON}$.
- Monte Carlo simulations are run to obtain statistical data (mean (μ), variance (σ)) for each device.
- Second step: PVT aware characterization of logic gates. At a given temperature, the logic gate under consideration is biased for each state and Monte Carlo simulations are performed.
- State dependent data for $\hat{I}_{GIDL}$ and $\hat{I}_{sub}$ is presented. This is followed by measurement of $\hat{I}_{dyn}$ and Propagation Delay.



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High-κ Modeling at Device Level

- 32nm Predictive Technology Model (PTM) is used for modeling HKMG transistors (http://www.eas.asu.edu/~ptm/).
- Two methods are used: (1) The model parameter in the model card that denotes relative permittivity (EPSROX) is changed or (2) The equivalent oxide thickness (EOT) for the dielectric under consideration is calculated.
- The EOT is calculated by the formula:

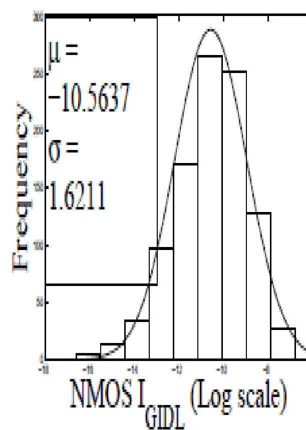
$$EOT = \left(\frac{\kappa_{SiO_2}}{\kappa_{gate}} \right) * t_{gate}$$

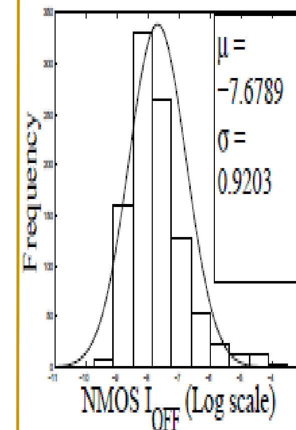
- κ_{gate} is the relative permittivity and t_{gate} is the thickness of the gate dielectric material other than SiO_2.
- κ_{SiO2} is the dielectric constant of SiO_2 (= 3.9). We have taken κ_{gate}=21 and t_{gate}=5 nm to emulate a HfO_2 based dielectric. EOT is calculated to be 0.9 nm.

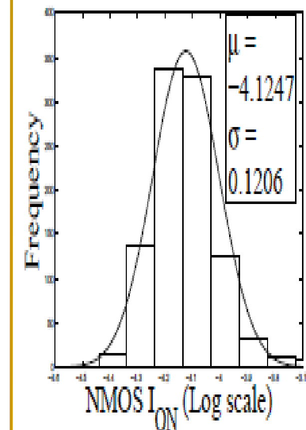
Variation-Aware HKMG Device Level Characterization

- Different biasing conditions are used for device level characterization of $\hat{I}_{GIDL}$, $\hat{I}_{OFF}$ and $\hat{I}_{ON}$.
- A Monte Carlo analysis is done with N=1000 runs, with the 15 process parameters. Each of these process parameters is assumed to have a Gaussian distribution with mean taken as the nominal values specified in the PTM and standard deviation as 10% of the mean.
- $\hat{I}_{GIDL}$, $\hat{I}_{OFF}$ and $\hat{I}_{ON}$ exhibit Lognormal distribution.

PDF of Currents		NMOS Device	PMOS Device
$\hat{I}_{GIDL}$	μ	-10.5637	-10.1050
	σ	1.6211	0.9927
$\hat{I}_{OFF}$	μ	-7.6789	-7.4682
	σ	0.9203	1.1446
$\hat{I}_{ON}$	μ	-4.1247	-4.1694
	σ	0.1206	0.1632







Variation-Aware State Dependent HKMG Logic Level Characterization

- Results for HKMG logic cells are presented at room temperature (27∘C).
- State dependent data for $\hat{I}_{GIDL}$ and $\hat{I}_{sub}$ as it leads to accurate leakage estimation.
- As $\hat{I}_{dyn}$ depends primarily on the switching of the logic gates, average data for $\hat{I}_{dyn}$ is presented.
- C_L is taken as 10 times C_{gg} (gate capacitance of PMOS).
- Logic cells characterized: Inverter, NAND, NOR and Buffer.
- Propagation Delay measured using formula:

$$Delay = \left(\frac{T_{PDLH} + T_{PDHL}}{2} \right)$$

PDF of Currents / Delay		"00"	"01"	"10"	"11"
$\hat{I}_{GIDL}$	μ	-10.5409	-10.5779	-13.3605	-10.0153
	σ	1.6280	1.6377	1.6670	1.6247
$\hat{I}_{sub}$	μ	-8.4793	-7.6933	-7.9148	-7.8814
	σ	0.6193	0.8815	0.7913	1.0967
$\hat{I}_{dyn}$	μ	-6.5458			
	σ	0.2203			
Delay	μ	126.37ps			
	σ	29.72ps			

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Variation-Aware State Dependent Logic Level Characterization: HKMG NAND

(a) State "00" (b) State "01" (c) State "10" (d) State "11"

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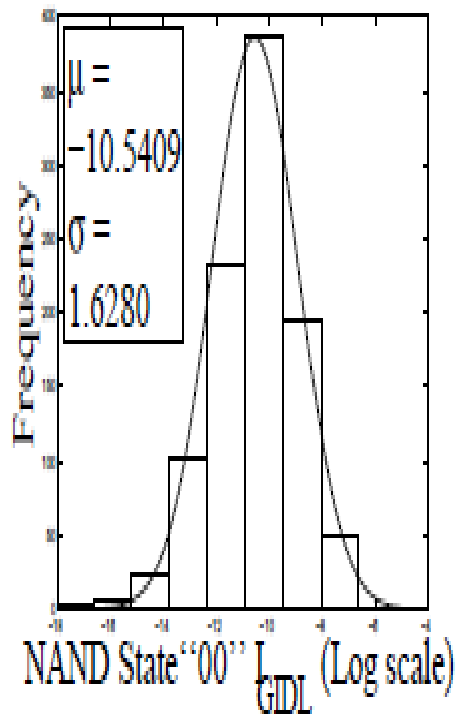
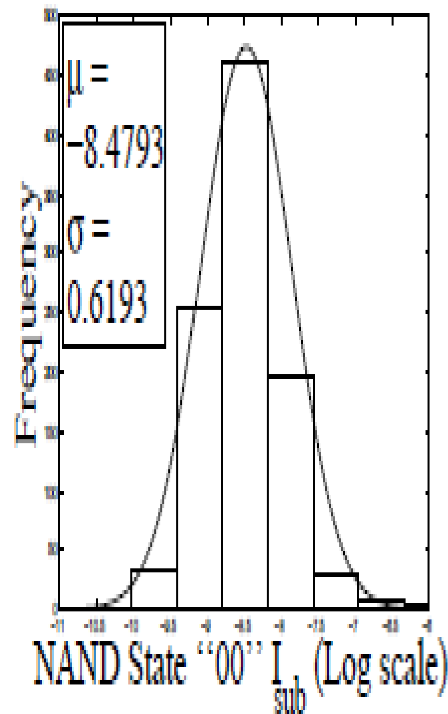
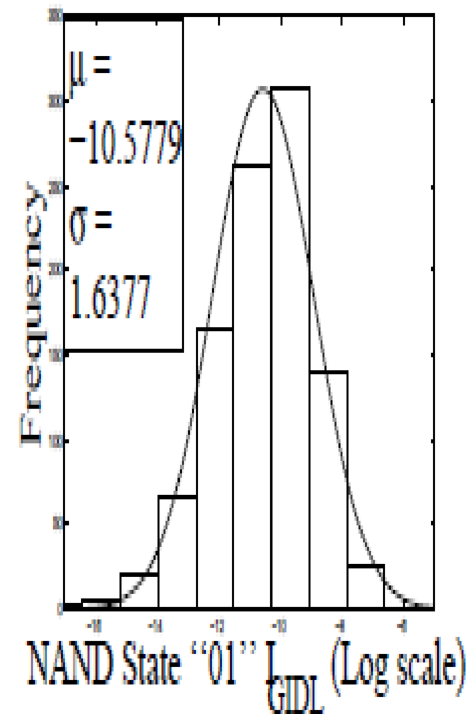
Variation-Aware State Dependent Logic Level Characterization: HKMG NAND



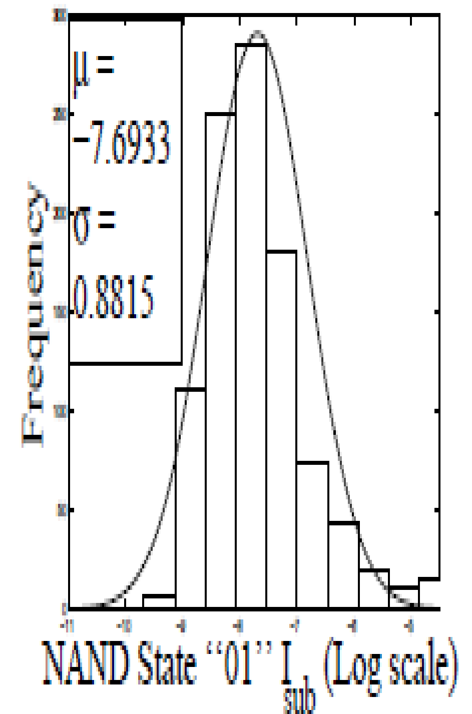
(a) state 00: GIDL



(b) state 00: Subthreshold

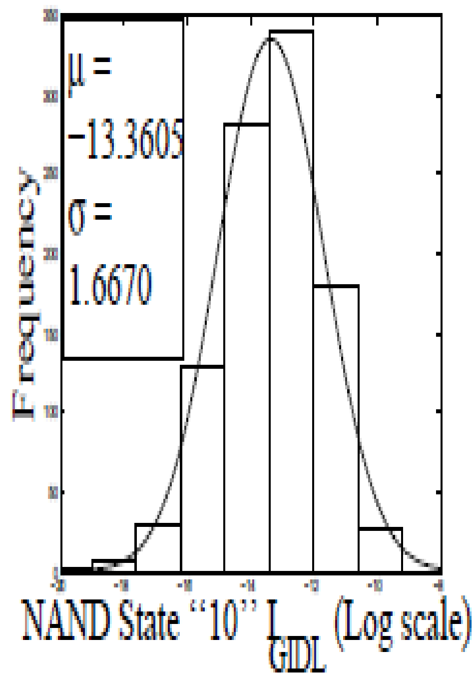


(c) state 01: GIDL

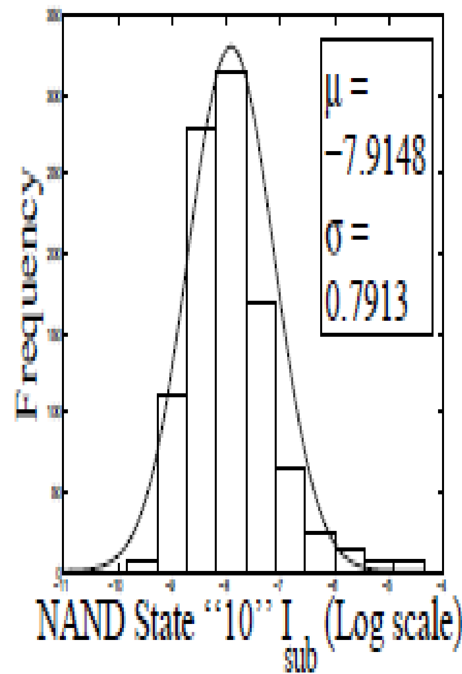


(d) state 01: Subthreshold

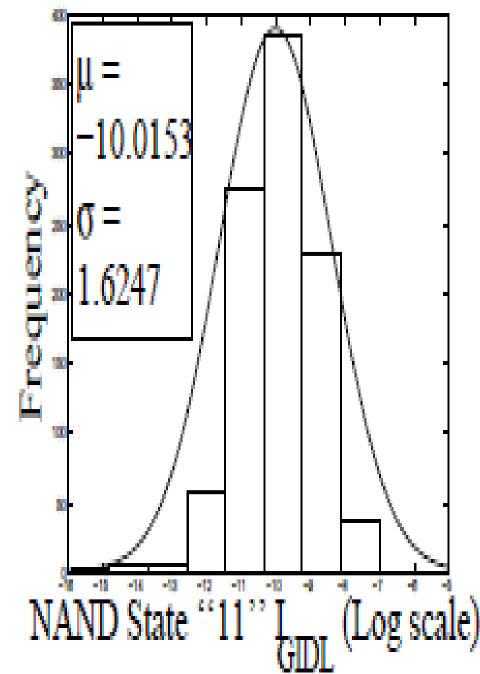
Variation-Aware State Dependent Logic Level Characterization: HKMG NAND



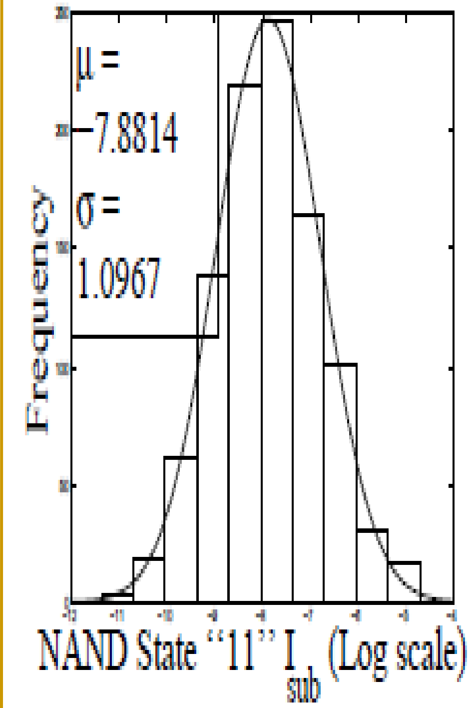
(e) state 10: GIDL



(f) state 10: Subthreshold



(g) state 11: GIDL



(h) state 11: Subthreshold

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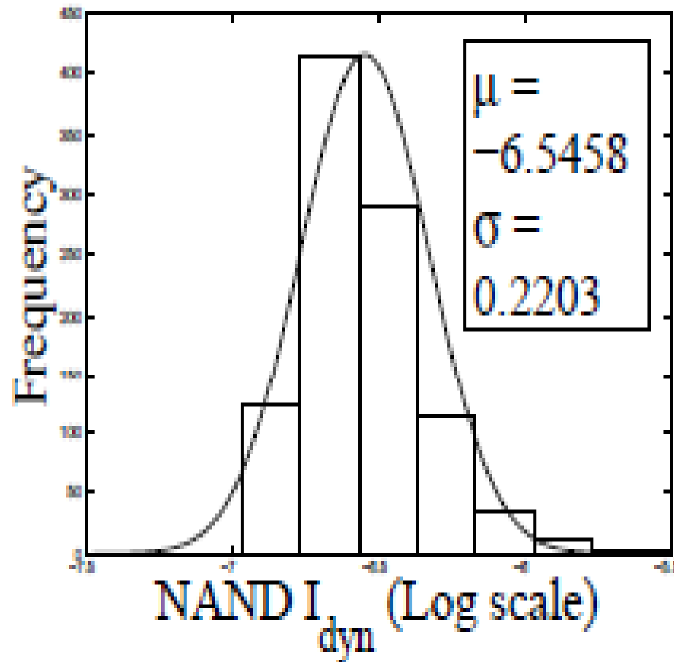
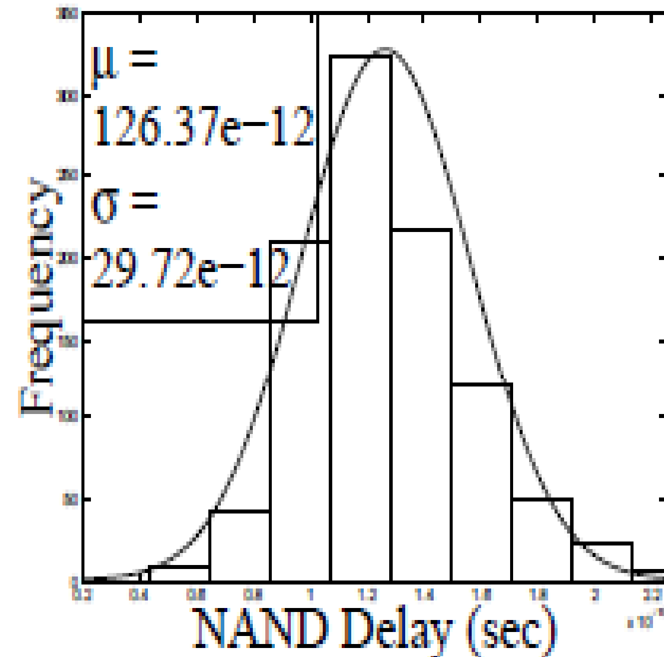
Variation-Aware State Dependent Logic Level Characterization: HKMG NAND



(i) Avg. : I_{dyn}



(j) Avg. : Delay

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PVT-Aware HKMG Logic Level Characterization

- Simulations at 0°C, +50°C, +100°C, +125°C are considered.
- It is observed that $\hat{I}_{GIDL}$ does not show strong dependence on temperature.
- $\hat{I}_{sub}$ shows an increase in the mean (μ) value with increasing temperature. This is due to dependence of $\hat{I}_{sub}$ on V_{Th}, which depends strongly upon temperature.
- Delay also shows an increasing trend with temperature.
- $\hat{I}_{dyn}$ is measured over one cycle of operation. It remains almost constant with temperature, because for one cycle theoretically, $\hat{I}_{dyn}$ does not depend on frequency (delay).

Temp	PDF of $\hat{I}_{GIDL}$			PDF of $\hat{I}_{sub}$			PDF of $\hat{I}_{dyn}$			PDF of Delay		
(° C)	μ	σ	$\frac{\sigma}{\mu}$ %	μ	σ	$\frac{\sigma}{\mu}$ %	μ	σ	$\frac{\sigma}{\mu}$ %	μ	σ	$\frac{\sigma}{\mu}$ %
0	-10.5398	1.6230	15.4	-8.9032	0.6763	7.6	-6.5504	0.2184	3.3	126.41 ps	29.61 ps	23.42
50	-10.5418	1.6325	15.5	-8.1738	0.5784	7.1	-6.5442	0.2210	3.4	127.19 ps	30.12 ps	23.68
100	-10.5443	1.6432	15.6	-7.6394	0.5070	6.6	-6.5441	0.2205	3.4	131.55 ps	31.52 ps	23.96
125	-10.5457	1.6490	15.6	-7.4228	0.4781	6.4	-6.5439	0.2197	3.4	134.8 ps	32.32 ps	23.98

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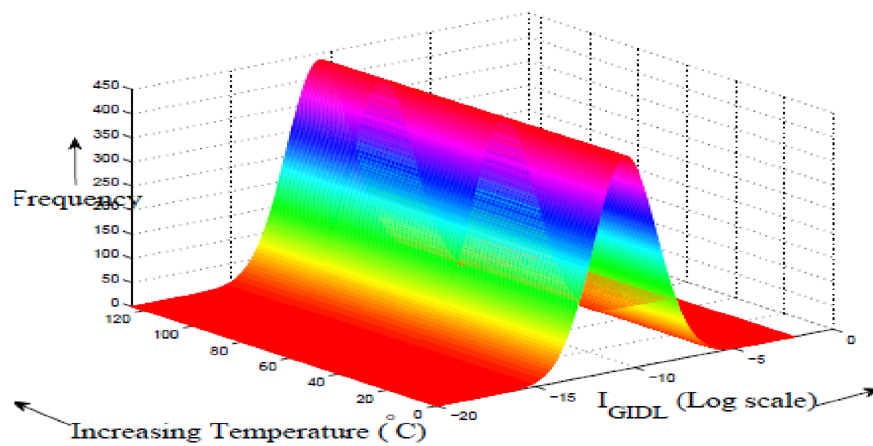
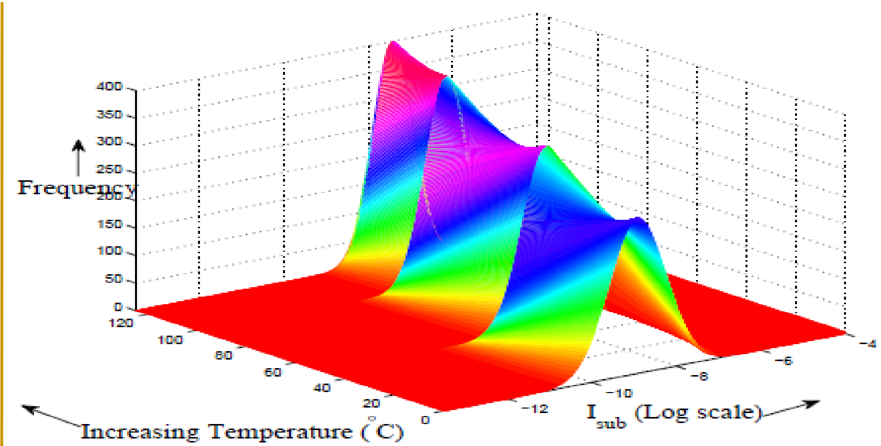
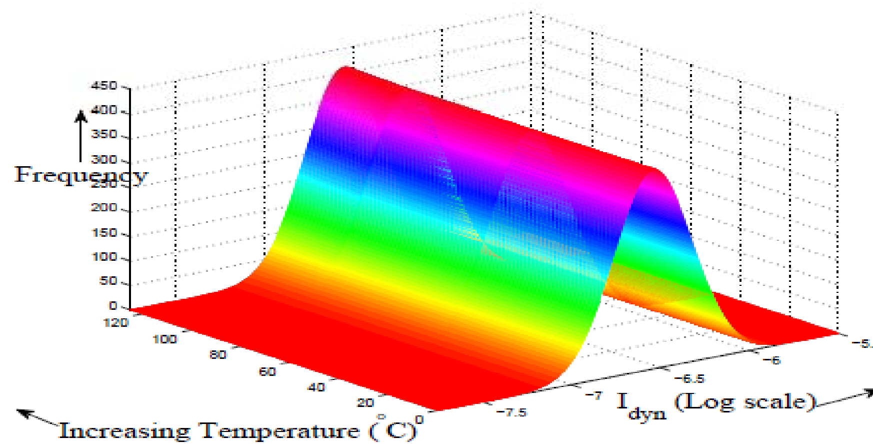
PVT-Aware Logic Level Characterization: HKMG NAND



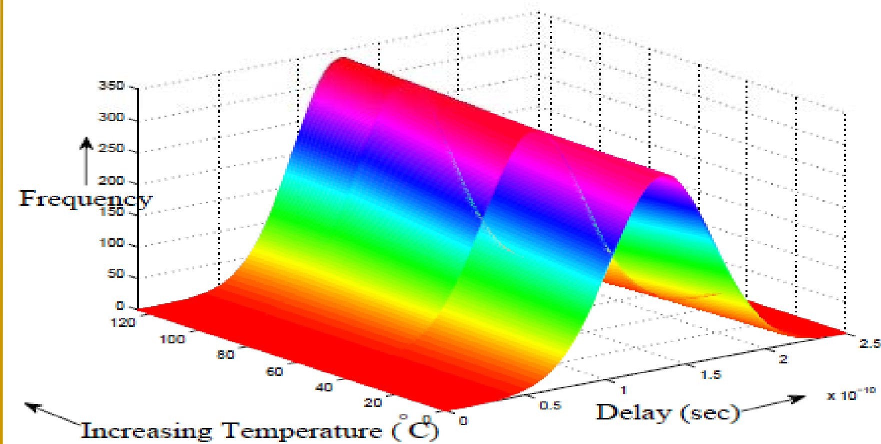
(a) I_{GIDL}



(b) I_{sub}



(c) I_{dyn}



(d) Delay

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Conclusions

- Methodology for a PVT aware HKMG standard cell library creation while considering the effect of process variations is presented.
- Device level characterization for HKMG NMOS and PMOS transistors for drive current ($\hat{I}_{ON}$), off-current ($\hat{I}_{OFF}$) and GIDL current ($\hat{I}_{GIDL}$) has been done, modeled using 32 nm PTM models.
- This is followed by PVT aware statistical characterization of standard cells. The state dependent data for $\hat{I}_{sub}$, $\hat{I}_{GIDL}$ and dynamic current ($\hat{I}_{dyn}$) are presented.

Future Research

- We plan to develop similar logic libraries for other non-classical CMOS technologies such as Double Gate FET and Carbon Nanotubes and analyze their performance.
- Applications for HKMG Library:
  - The data provided in the paper will be useful at the system level when a probabilistic analysis is carried out.
  - Useful for probabilistic-CMOS, where the analysis is done using probability distribution functions (PDFs), instead of working with actual values.

Thank you !!