A Combined Packet Classifier and Scheduler Towards Net-Centric Multimedia Processor Design

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Outline of Talk

- Introduction and Motivation
- Proposed Net-Centric Multimedia Processor (NMP)
- Classification-Scheduling Algorithm
- Classification-Scheduling Architecture
- Prototype Development
- Experimental Results
- Conclusion and Future Works

Introduction and Motivation

- IP-TV (Internet Protocol Television) supports more and more entertaining and educating applications such as commercial TV, video on demand, time-shifted TV, video phones, game portals, personal digital library, etc.
- Challenges for IP-TV include:
  - Scalability
  - High-quality of service
  - Cost-effective service deployment
  - Digital Rights Management (DRM) for security and copyright protection

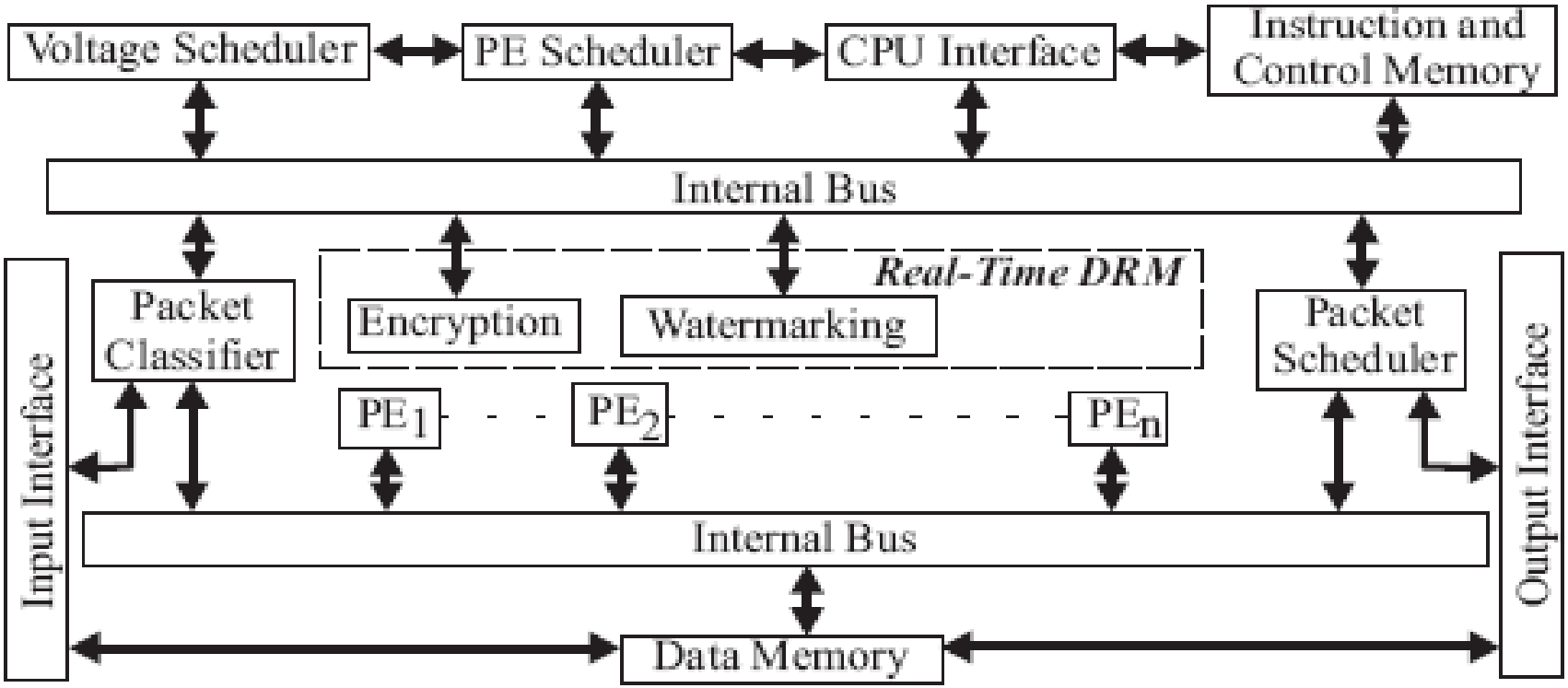
  To solve DRM problem, we propose a Net-Centric Multimedia Processor (NMP) with built-in DRM facilities.

Introduction and Motivation

- NMP possesses multimedia processing capabilities along with networking capabilities.
- NMP can completely offload multimedia processing and network packet processing from CPU thus making CPU available for other applications.
- NMP may be included as a part of line cards of common routers, network cards, set-top boxes, or other high-speed communications devices in the IP network cloud.

Proposed NMP Architecture

- NMP architecture proposed for System-on-Chip (SoC) implementation.



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Proposed NMP Architecture

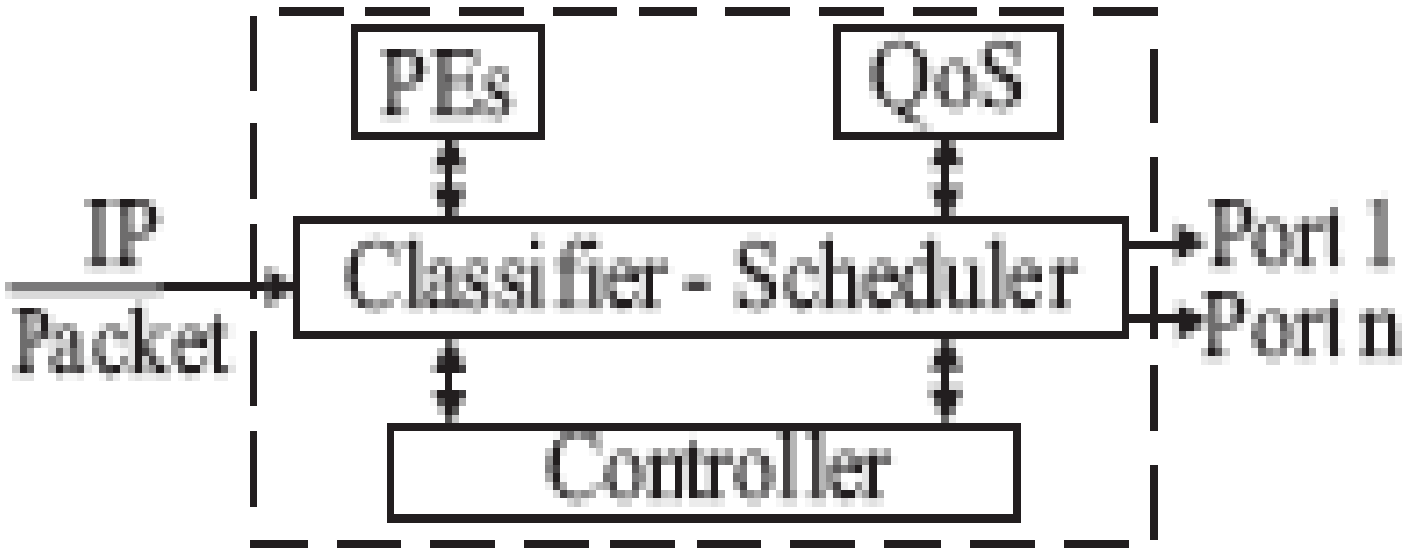
- Architecture consists of several processing elements (PEs) connected through internal bus.
- Packet classification carried out by packet classifier, which passes the packet to the appropriate PE for further processing.
- The outgoing packet is dynamically buffered by the packet scheduler until it is sent to the outgoing link.
- Instruction and control memory used to store the instructions corresponding to the program that is to be executed.
- Data memory used to store or buffer the (video/IP) data, and an appropriate mechanism is needed to avoid data conflict among the PEs.
- Input interface and output interface are two ports through which the proposed NMP communicates with the external environment.

High Level Classifier-Scheduler Architecture

- Need to develop the classification and scheduling for high-performance processing while reducing the operation latency, logic usage, and power dissipation.
- As IP packets arrive, they need to be processed directly without using the CPU.
- Proposed module differentiates between IP packets and video packets. Video packets are further processed for DRM using PEs. IP packets traverse as usual for further processing.
- Algorithm classifies and sends data to PEs and joins back the data with the header after the processing is performed.
- The scheduler collects them and using the updates from the controller schedules the packets based on Quality-of-Service (QoS) parameters.

High Level Classifier-Scheduler Architecture

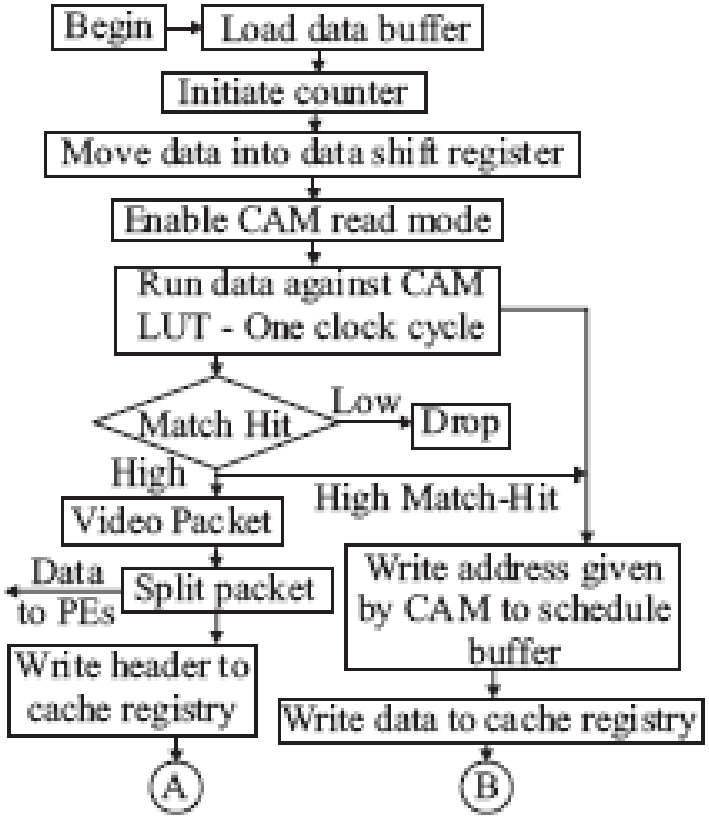
- The classifier-scheduler is tied to the controller through data buses and to the memory with address buses.



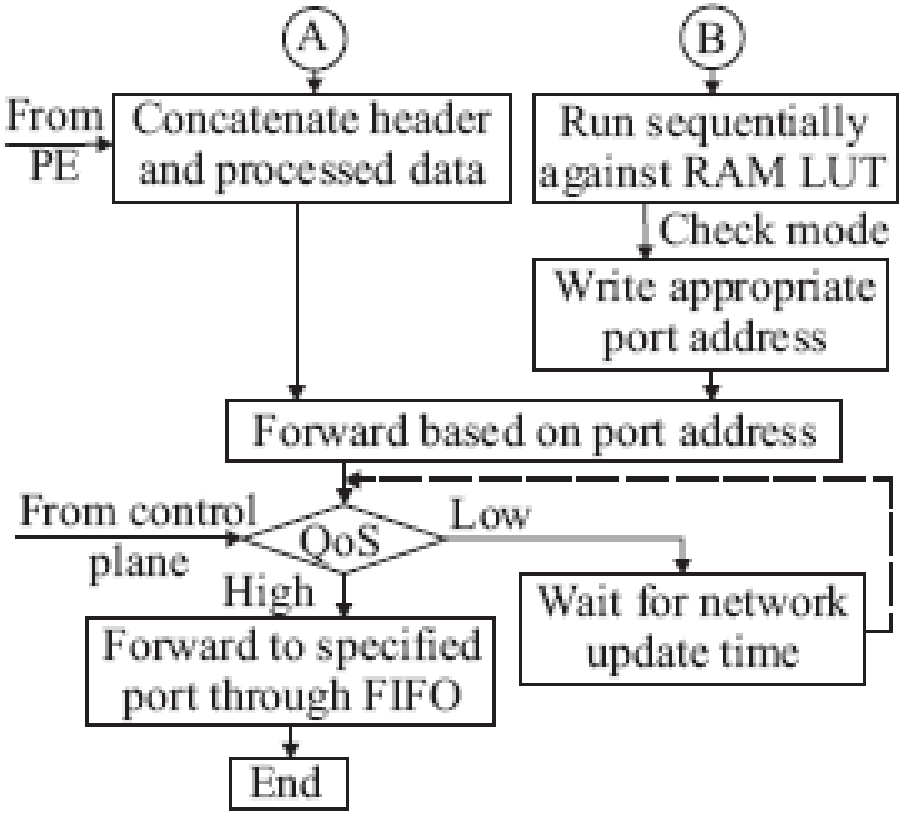
Classification-Scheduling Algorithm

- Once the string of data (the IP packet) flows in, the classifier checks the header against Content Addressable Memory (CAM) Look Up Tables (LUTs), strips the header and stores it in cache.
- The remaining of the packet is forwarded to PEs.
- After the PEs send the data back, the registry is updated and it is joined with the header.
- The schedulers registry is constantly updated by the QoS updater.
- Once a new packet comes in, it takes the update and schedules it or pushes the packet back in the queue.

Classification-Scheduling Algorithm



(a) Beginning phases, continued in (b)



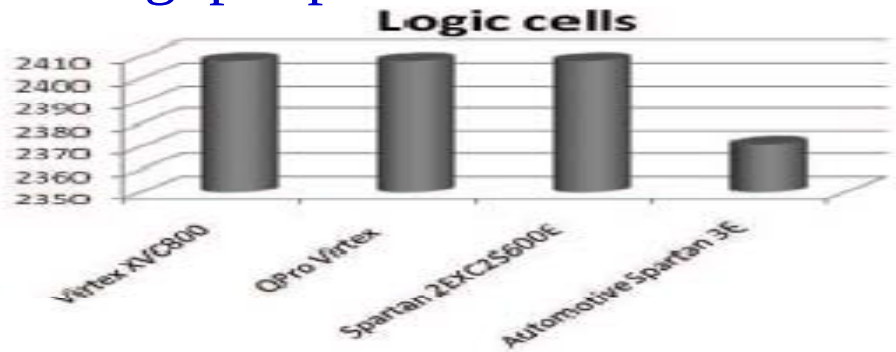
(b) Last phases, continued from (a)

Prototyping

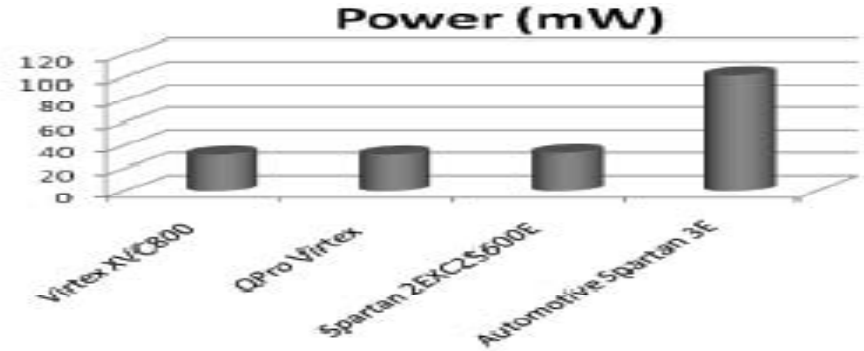
- Prototype modeled using VHDL and simulated through Xilinx.
- CAM architecture is used as the basis for the classifier-scheduler.
- A bit flag is added in the options field in the physical packet address, so that the classifier-scheduler can easily identify a video packet from a non-video packet.
- If the flag is high, the packet is considered a video packet else considered as an IP packet.
- Synthesis of the VHDL description of the module performed along with its mapping, placement and routing.
- The models are simulated for 4 different logic families. It is a designer's choice to select a particular logic family depending on a target application.
- The power dissipation is estimated under the ambient temperature of 25 °C and supply voltage of 2.5V .

Experimental Results

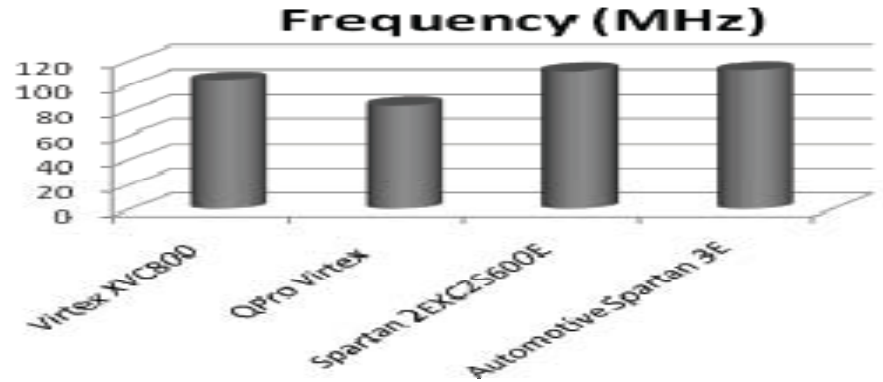
- The throughput is highest for Automotive-Spartan3, but the risk is high power dissipation.
- Virtex-XV and Spartan-2E is more appropriate for power and throughput point of view.

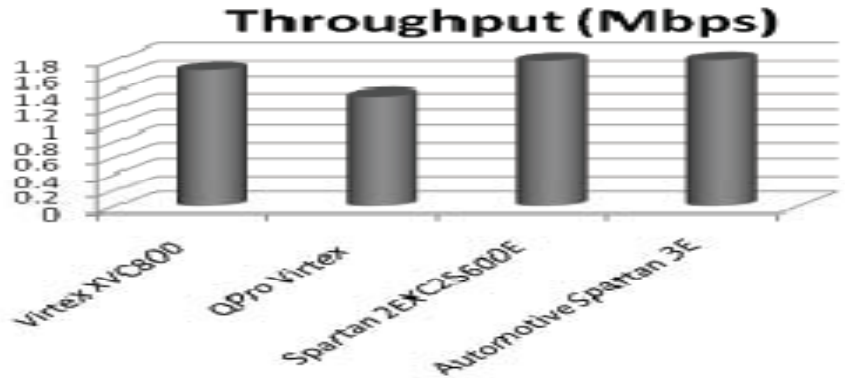


(a)



(b)





Conclusion and Future Works

- The classifier-scheduler has been implemented in structural and behavioral design.
- The classifier-scheduler can be used for NMP as well as network processors with appropriate modifications.
- We have introduced the architecture of NMP, and analyzed the complexities of developing NMP as a SoC design.
- We have also built other modules, such as watermarking and encryption.
- Many other modules are in the process of building.
- Further, we will use low-power techniques like power gating and voltage scaling to handle power issues.


Thank you !!!